

MITSUBISHI 1990 SEMICONDUCTORS

BIPOLAR DIGITAL IC LSTTL

UM PBOX



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★: New product



GUIDANCE 1

TYPE DESIGNATION TABLE INDEX BY FUNCTION SYMBOLOGY PACKAGE OUTLINES

MITSUBISHI LSTTLS TYPE DESIGNATION TABLE

TYPE DESIGNATION TABLE

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MITSUBISHI LSTTLS INDEX BY FUNCTION

INDEX BY FUNCTION (Recommended operating conditions, $V_{OC} = 5V \pm 5\%$, $T_{opr} = -20 \text{ } + 75 ^{\circ}\text{C}$)

INVERTERS, NAND GATES

	Type of	output		Турі	cal electric	al characte	eristics			
Circuit function	Active pull-up	Open collector	Type	Propa- gation time (ns)	Power dissipa- tion (mW)	output	High-level output current (mA)	Package Outlines	Interchangeable products	Page
Hex Inverter	0	_	M74LS04P	6	12	8	0.4	14P4	74LS04	2-15
nex mverter	_	0	M74LS05P	10	12	8		14P4	74LS05	2-17
Quadruple 2-Input Positive NAND Gate	0		M74LS00P	6	8	8	0.4	14P4	74LS00	2-9
Quadruple 2-Input Positive NAND Gate	_	0	M74LS03P	10	8	8		14P4	74LS03	2-13
Triple 3-Input Positive NAND Gate	0	_	M74LS10P	8	6	8	0.4	14P4	74LS10	2-23
Triple 3-Input Positive NAND Gate	_	0	M74LS12P	13	6.3	8	_	14P4	74LS12	2-27
Duel 4 leas & Decision NAND Con-	0		M74LS20P	10	4	8	0.4	14P4	74LS20	2-39
Dual 4-Input Positive NAND Gate	_	0	M74LS22P	18	4	8	_	14P4	74LS22	2-43
Single 8-Input Positive NAND Gate	0	_	M74LS30P	11	2.4	8	0.4	14P4	. 74LS30	2-49
Single 13-Input Positive NAND Gate	0	_	M74LS133P	11	2.4	8	0.4	16P4	74LS133	2-143

AND GATES

Quadruple 2-Input Positive AND Gate	0	_	M74LS08P	1.0	17 ·	8 .	0.4	14P4	74LS08	2-19
Quadruple 2-input Fositive AND Gate	_	0	M74LS09P	13	17	8		14P4	74L S09	2-21
Triple 3-Input Positive AND Gate	0	_	M74LS11P	10	12.8	8	0.4	14P4	74LS11	2-25
Thiple 3-rilput Positive AND Gate:		0	M74LS15P	13	12.8	8	_	14P4	74LS15	2-33
Dual 4-Input Positive AND Gate	0	_	M74LS21P	10	8.5	8	0.4	14P4	74LS21	2-41

NOR GATES

Quadruple 2-Input Positive NOR Gate	O	 M74 LS02P	6	10	8	0.4	14P4	74LS02	2-11
Triple 3-Input Positive NOR Gate	0	 M74LS27P	6	13.5	8	0.4	14P4	74LS27	2-47

OR GATE

Quadruple 2-Input Positive OR Gate		84741 C20D	7	20		140	741 0 00	0.51
accordance 2 mpdt 1 ositive Off date		M74LS32P	/	20	 I U.4	14P4	74LS32	2-51

EXCLUSIVE OR GATES

	0	-	M74LS86P	10	30.5	8	0.4	1.4P4	74LS86	2-90
Quadruple 2-Input Exclusive OR Gate	<u> </u>	0	M74LS136P	13	30.5	8	_	14P4	74LS 136	2-145
	0		M74LS386P	10	30.5	8	0.4	14P4	74LS386	2-366

EXCLUSIVE NOR GATE

Quadruple 2-Input Exclusive NOR Gate	_	C	M74LS266P	15	40	8	_	14P4	74LS266	2-302

AND-OR-INVERT GATE

2-Wide 2-Input AND-OR-INVERT) —	M74LS51P	7	5.5	8	0.4	14P4	74LS51	2-69
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MITSUBISHI LSTTLS INDEX BY FUNCTION

BUFFERS/LINE DRIVERS

	Туре	of out	put		Тур	ical elec	trical ch	aracteri		0) (0		
Circuit function	Active pull-up	Open collector	3-state	Туре	Propagation time (ns)	Power dissipa- tion (mW)		High- level output current (mA)	CHysteresis (VT+-VT-)	Package Outlines	Interchangeable products	Page
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Octal Buffer/Line Driver			N	M74LS244P	9	126.7	24	15	0.4	20P4	74LS244	2-269
		_	1	M74LS540P	10	111.7	24	15	0.4	20P4	74LS540	2-385
·	_	-	N	M74LS541P	10	133.3	24	15	0.4	20P4	74LS541	2-388
	_	_	N	M74LS245P	10	290	24	15	0.4	20P4	74LS245	2-272
·	_		ı	M74LS620P	10 .	290	24	15	0.4	20P4	74LS620	2-399
			- 1	M74LS640P	10	290	24	15	0.4	20P4	74LS640	2-402
	_	_)	M74LS640-1P	10	290	48	15	0.4	20P4	74LS640-1	2-405
	_	N	_	M74LS641P	18	290	24	_	0.4	20P4	74LS641	2-408
·	_	N	_	M74LS641-1P	18	290	48		0.4	20P4	74LS641-1	2-411
Octal Bus Transceiver	_		_	M74LS642P	15	290	24		0.4	20P4	74LS642	2-414
Octai bus fransceivei			_	M74LS642-1P	15	290	48	_	0.4	20P4	74LS642-1	2-417
		_	I·N	M74LS643P	10	290	24	15	0.4	20P4	74LS643	2-420
		_	I٠N	M74LS643-1P	10	290	48	15	0.4	20P4	74LS643-1	2-423
	_	I٠N		M74LS644P	16	290	24	_	0.4	20P4	74LS644	2-426
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Hex Bus Driver		_	N	M74LS367AP	9	67.5	24	2.6	_	16P4	74L S367A	2-347
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Outside B. B. W. Con		-1	N	M74LS125AP	9	51.8	24	2.6	_	14P4	74LS125A	2-137
Quadruple Bus Buffer Gate		-	N	M74LS126AP	9	59	24	2.6	_	14P4	74LS126A	2-139
Overden pla Dura Tarana		_	ı	M74LS242P	8	133.3	24	15	0.4	14P4	74LS242	2-263
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Dual 4-Input Positive NAND Buffer	ī	_		M74LS40P	14	8.6	24	1.2	_	14P4	74LS40	2-57

I: With inverted output N: With noninverted output I+N: With both inverted and noninverted output

SCHMITT TRIGGER NAND GATES/INVERTERS

	Туре о	f output		Typic	al electri	ical chara	cteristics			
Circuit function	Active pull-up	Open collector	Туре	Propaga- tion time (ns)	Power dissipa- tion (mW)	Positive- going threshold voltage (V)	Negative- going threshold voltage (V)	Package Outlines	Interchangeable products	Page
Hex Schmitt Trigger Inverter	1	_	M74LS14P	12	51.5	1.6	0.8	14P4	74LS14	2-31
	1		M74LS19P	13	67	1.9	1.0	14P4	74LS19	2-37
Quadruple 2-Input Positive NAND	.1		M74LS132P	13	35.3	1.6	0.8	14P4	74LS 132	2-141
Schmitt Trigger	1		M74LS24P	19	44	1.9	1.0	14P4	74LS24	2-45
Dual 4-Input Positive NAND Schmitt	I	_	M74LS13P	16	17.5	1.6	0.8	14P4	74LS13	2-29
Trigger	1 .	_	M74LS18P	25	22.5	1.9	1.0	14P4	74LS18	2-35

^{1 :} With inverted output



J-K FLIP-FLOPS

		Typic	al electrica	al characte	eristics				0) 10		
Circuit function	Type	Operating frequency (MHz)		Hold time (ns)	Power dissipation (mW)	Trigger	Preset	Reset	Package Outlines	Interchangeable products	Page
Dual J-K Negative Edge-Triggered Flip- Flop with Reset	M74LS73AP	0 ~ 45	20	0	20	Z	_	I	14P4	74LS73A	2-71
Dual J-K Negative Edge-Triggered Flip- Flop with Set and Reset	M74LS76AP	0~45	20	0	20	Z	U	IJ	16P4	74LS76A	2-80
Dual J-K Negative Edge-Triggered Flip- Flop with Reset	M74LS107AP	0~45	20	0	20	P	-	J	14P4	74LS107A	2-112
Dual J-K Positive Edge-Triggered Flip- Flop with Set and Reset	M74LS109AP	0~45	20	5	20	7	\mathbb{I}	J	16P4	7 4 LS109A	2-115
Dual J-K Negative Edge-Triggered Flip- Flop with Set and Reset	M74LS112AP	0 - 45	20	0	20	Z	J	I	16P4	7 4 LS112A	2-118
Dual J-K Negative Edge-Triggered Flip- Flop with Set	M74L S 113AP	0 ~ 45	20	0	20	Ł	L	_	14P4	74LS113A	2-121
Dual J-K Negative Edge-Triggered Flip-Flop with Set Common Reset and Common Clock	M74LS114AP	0 ~ 45	20	0	20	Ł	IJ	IJ	14P4	74LS114A	2-124

 $\underline{\mathbf{J}}$: Positive-going edge $\underline{\mathbf{V}}$: Negative-going edge $\underline{\mathbf{J}}$: Active low-level

D-Type FLIP FLOPS

		Typic	al electrica	al characte	ristics						
Circuit function	Туре	Operating frequency (MHz)		Hold time (ns)	Power dissipation (mW)	Trigger	Preset	Reset	Package Outlines	Interchangeable products	Page
Dual D-Type Edge-Triggered Flip-Flop with Set and Reset	M74LS74AP	0~50	20	5	20	F	T	V	14P4	74LS74A	2-74
Hex D-Type Flip-Flop with Reset	M74LS174P	0~47	20	5	- 80	1	_	٦٢	16P4	74LS174	2-214
Quadruple D-Type Flip-Flop with Reset	M74LS175P	0~50	20	5	55	<u></u>	-	٦٢	16P4	74LS175	2-217
Octal Positive Edge-Triggered D-Type Flip- Flop with Reset	M74LS273P	0~40	20	5	85	<u></u>	-	Ţ	20P4	74LS273	2-304
Octal Positive Edge-Triggered D-Type Flip- Flop with 3-State Outputs	M74LS374P	0~40	20	4	135	7	-	_	20P-4	74LS374	2-356
Octal Positive Edge-Triggered D-Type Flip- Flop with Enable	M74LS377P	0~40	25	5	85	Ţ	_	_	20P4	7 4 LS377	2-363

 \coprod : Active low-level

LATCHES, REGISTERS

		,Typic	al electrica	al characte	eristics					
Circuit function	Туре	Power dissipa- tion (ns)	Setup time (ns)	Hold time (ns)	Power dissipa- tion (mW)	Enable	Reset	Package Outlines	Interchangeable products	Page
10.0	M74LS75P	9	20	8	31.5	Л	-	16P4	74LS75	2-77
4-Bit Bistable Latch	M74LS375P	9	20	8	31.5	Л	-	16P4	74LS375	2-360
Dual 4-Bit Addresable Latch	M74LS256P	13	15	5	100	_	П	16P4	74LS256	2-288
8-Bit Addressable Latch	M74LS259P	13	. 15	5	100	_	U	16P4	74LS259	2-298
Quadruple R-S Latch	M74LS279P	10	_		19	_	-	16P4	74L S279	2-307
Octal D-Type Transparent Latch with 3-State Outputs	M74LS373P	12	5	20	120	Л	-	20P4	7 4 L\$373	2-353
4-Bit D-Type Register with 3-State Outputs	M74LS173AP	23	17	6	85	F	Л	16P4	74LS173A	2-210

☐ : Active high-level

 \coprod : Active low-level

MITSUBISHI LSTTLS INDEX BY FUNCTION

SHIFT REGISTERS

			electrical teristics			М	ode	-	4		
	T	Operating	Power	ب ا	¥		oad	Hold Do nothing)	ackage	Interchangeable	
Circuit function	Type	frequency	dissipation		Right shift	eft shift	arallel load	fold	ag =	products	Page
	[(MHz)	(mW)	oc.	Righ	Left	Para	100	a o		
8-Bit Universal Shift/Storage Register	M74LS299P	0~28	165	Α	0	0	0	0	20P4	74L S299	2-328
6-Bit Offiversal Stiff() Storage Register	M74LS323P	0~28	165	s	0	0	0	0	20P4	74LS323	2-332
4-Bit Bidirectional Universal Shift Register	M74LS194AP	0~45	75	Α	0	0	0	0	16P4	74LS194A	2-236
5-Bit Shift Register	M74LS96P	0~45	60	Α	0	_	0	-	16P4	74LS96	2-108
4-Bit Cascadable Shift Register with 3-State Outputs	M74LS395AP	0~40	83.8	Α	0	-	0	-	16P4	74LS395	2-374
4-Bit Parallel Access Shift Register	M74LS195AP	0~60	70	Α	0	_	0	-	16P4	74LS 195A	2-239
4-Bit Parallel Access Shift Register	M74LS95BP	0~50	65	-	0	-	0	-	14P4	74LS95B	2-105
4-Bit Shift Register with 3-State Outputs	M74LS295BP	0~40	72.5	_	0	_	0	_	14P4	74LS295B	2-322
8-Bit Serial-In Parallel-Out Shift Register	M74LS164P	0~50	80	Α	0	_	_	_	14P4	74LS164	2-196
8-Bit Shift Register	M74LS91P	0~60	60	-	0	-	_	_	14P4	74LS91	2-95
8-Bit Parallel-Load Shift Register	M74LS165AP	0~38	105	_	0	-	_	_	16P4	74LS165A	2-199
8-Bit Shift Register	M74LS166AP	0~38	100	Α	0	_	_	_	16P4	74LS166A	2-203
8-Bit Shift Register/Latch with 3-State Output	M74LS595P			Α	0	_	_	0	16P4	74LS595	2-391
8-Bit Shift Register/Latch with Open Collector Output	M74LS596P			Α	0	_	_	0	16P4	74LS596	2-395

A: Asynchronous S: Synchronous

ASYNCHRONOUS COUNTERS

	LO.	,	Typical e					o s		
Circuit function	Organization	Туре	Clock frequency (MHz)	Power	Trigger	Parallel load	Reset	Package Outlines	Interchangeable products	Page
Davida Carata	.2×5	M74LS90P	0~75 0~30	45	Ł	"9" set	几	14P4	74LS90	2-92
Decade Counter	2×5	M74LS290P	0~75 0~30	45	7	"9" set	Л	14P4	74LS290	2-316
Presettable Decade Counter/Latch	2×5	M74LS196P	0~80 0~25	80	7	Α	T	14P4	74LS196	2-242
	2×8	M74LS93P	0~60 0~35	45	Ł		Л	14P4	74LS93	2-101
4-Bit Binary Counter	2×8	M74LS293P	0~60 0~35	45	Ł	_	Л	14P4	74LS293	2-319
Presettable 4-Bit Binary Counter/Latch	2×8	M74LS197P	0~80 0~35	80	Ł	A	U	14P4	74LS197	2-246
Divide-by-Twelve Counter	2×6	M74LS92P	0~80 0~30	45	Ł	_	Л	14P4	74LS92	2-98
Dual Decade Counter	2×5	M74LS390P	0~80 0~35	100	Ł	_	几	16P4	74LS390	2-368
Dual 4-Bit Decade Counter	2×5	M74LS490P	0~35	75	P	_	Λ	16P4	74LS490	2-382
Dual 4-Bit Binary Counter	16	M74LS393P	0~75	100	Ł	_	几	14P4	74LS393	2-371

V: Negative-going edge

A : Asynchronous

"9" set: Output QA and QD can be set to high directly, and output QB and QC to low.



SYNCHRONOUS COUNTERS

Circuit function	Туре	Typical e charact Clock frequency (MHz)		Trigger	Parallel load	Reset	Package Outlines	Interchangeable products	Page
Synchronous Presettable Decade Counter with Direct Reset	M74LS160AP	0~55	92.5	7	s	Α	16P4	74LS160A	2-180
Fully Synchronous Presettable Decade Counter	M74LS162AP	0~55	92.5	1	s	s	16P4	74LS162A	2-188
Synchronous Presettable Up/Down Decade Counter with Mode Control	M74LS190P	0~38	100	7	A	-	16P4	74LS190	2-220
Synchronous Presettable Up/Down Decade Counter	M74LS192P	0~38	95	1	Α	Α	16P4	74LS192	2-228
Synchronous Presettable 4-Bit Binary Counter with Direct Reset	M74LS161AP	0~55	92 .5	7	s	A	16P4	74LS161A	2-184
Fully Synchronous Presettable 4-Bit Binary Counter	M74LS163AP	0~55	92.5		S	S	16P4	74LS163A	2-192
Synchronous Presettable Up/Down 4-Bit Binary Counter with Mode Control	M74LS191P	0~40	100	<u></u>	A	_	16P4	74LS191	2-224
Synchronous Presettable Up/Down 4-Bit Binary Counter	M74LS193P	0~38	95	玉	Α	Α	16P4	74LS193	2-232
Synchronous Up/Down Decade Counter	M74LS668P	0~45	100	<u>F</u>	s	_	16P4	74LS668	2-438
Synchronous Up/Down 4-Bit Binary Counter	M74LS669P	0~30	100		S	_	16P4	74LS669	2-444

A : Asynchronous
S : Synchronous

MONOSTABLE MULTIVIBRATORS

		Typic	al electi	rical characteristics	ge ss		
Circuit function	Туре	Output pulse width	Power dissipation (mW)	External timing resistor /capacitor for setting output pulse width	Package Outlines	Interchangeable products	Page
Retriggerable Monostable Multivibrator with Reset	M74LS122P	70ns~∞	30	5~260kΩ/No limit	14P4	74LS122	2-127
Dual Retriggerable Monostable Multivibrator with Reset	M74LS123P	70 ns~ ∞	60	5~260kΩ/Na limit	16P4	74LS123	2-132
Dual Retriggerable Monostable Multivibrator with Reset	M74LS423P	70ns~∞	60	5~260k Ω/No limit	16P4	74LS423	2-377
Dual Monostable Multivibrator	M74LS221P	33 ns ~ ∞	62.5	1.4~100kΩ/0~1000μF	16P4	74LS221	2-250

DATA SELECTORS/MULTIPLEXERS

		Typical	Typical prop	pagation t	ime (ns)	e s		
Circuit function	Туре	dissipa- tion (mW)	From strobe (enable) input to output	From data input to output	From data input to inverted output	Package Outlines	Interchangeable products	Page
8-Line to 1-Line Data Selector/Multiplexer with Strobe	M74LS151P	30	15	15	8	16P4	74LS151	2-165
8-Line to 1-Line Data Selector/Multiplexer with 3-State Output	M74LS251P	33	13	15	7	16P4	74LS251	2-281
Dual 4-Line to 1-Line Data Selector/ Multiplexer with Strobe	M74LS153P	31	12	10	_	16P4	74LS153	2-168
Dual 4-Line to 1-Line Data Selector/ Multiplexer with 3-State Output	M74LS253P	38.8	12	10	_	16P4	74L S253	2-285
Dual 4-Line to 1-Line Data Selector/ Multiplexer with Strobe(Inverted)	M74LS352P	31	11'	_	7	16P4	74L S352	2-336
Dual 4-Line to 1-Line Data Selector/ Multiplexer with 3-State Output (Inverted)	M74LS353P	38.8	13	_	8	16P4	74LS353	2-338
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer	M74LS157P	48.5	12	8		16P4	74LS157	2-176
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer (Inverted)	M74LS158P	24	8	_	5	16P4	74LS158	2-178
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer with 3-State Output	M74LS257AP	47	9	7	_	16P4	74LS257A	2-292
Quadruple 2-Line to 1-Line Data Selector/ Multiplexer with 3-State Output (Inverted)	M74LS258AP	42.2	10	_	7	1.6P4	74LS258A	2-295
Quadruple 2-Input Multiplexer with Storage	M74LS298P	65	12 From clock input		-	16P4	74LS298	2-325



MITSUBISHI LSTTLS INDEX BY FUNCTION

DISPLAY DECODERS/DRIVERS

Circuit function	Output active level	Type	Power	Low-level current	Output break-down voltage (V)	ıcka	Interchangeable products	Page
BCD-to-Decimal Decoder/Driver	"L"	M74LS145P	35	24	15	16P4	74LS145	2-156
BCD-to-7-Segment Decoder/Driver	"L"	M74LS47P	35	24	15	16P4	74LS47	2-62
BCD-to-7-Segment Decoder/Driver	"H"	M74LS48P	125	6	Vcc	16P4	74LS48	2-66
BCD-to-7-Segment Decoder/Driver	"L"	M74LS247P	35	24	15	16P4	74LS247	2-275
BCD-to-7-Segment Decoder/Driver	"H"	M74LS248P	125	6	Vcc	16P4	74LS248	2-278

Segment Identification of M74LS47P, M74LS48P

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Segment identification	0	!	2	3	Y	S	0	٦	8	ď	u	n	U	UI	υL	

Segment Identification of M74LS247P, M74LS248P

1	Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Segment identification	0	1	U	3	T	5	5	7	8	9	C	D	U	- C	۲	

DECODERS DEMULTIPLEXERS

		Typical	Typical propag	ation time (ns)	s e		
Circuit function	Туре	power dissipation (mW)	From strobe (enable) input to output	From data input to output	Package	Interchangeable products	Page
BCD-to-Decimal Decoder	M74LS42P	35	-	12	16P4	74LS42	2-59
3-Line to 8-Line Decoder/Demultiplexer with Address Latch	M74LS137P	55	10	12	16P4	74LS137	2-147
3-Line to 8-Line Decoder/Demultiplexer	M74LS138P	31.5	12	14	16P4	74LS138	2-151
Dual 2-Line to 4-Line Decoder/Demultiplexer	M74LS139P	34	10	13	16P4	74LS139	2-154
Dual 2-Bit Binary to 4-Line Decoder/ Demultiplexer with Strobe	M74LS155P	30.5	16	13	16P4	74LS155	2-170
Dual 2-Bit Binary to 4-Line Decoder/ Demultiplexer with Open Collector Outputs	M74LS156P	30.5	23	19	16P4	74LS156	2-173

ENCODER

		Typica	al electrica	al charact	eristics	s ae		
Circuit function	Туре	Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)	Packag Outline	Interchangeable products	Page
10-Line to 4-Line Priority Encoder	M74LS147P	16	55	. 8	0.4	16P4	74LS147	2-159
8-Line to 3-Line Priority Encoder	M74LS148P	15	55	8	0.4	16P4	74LS148	2-162

MITSUBISHI LSTTLS INDEX BY FUNCTION

COMPARATOR

		Typica	el electrica	al charact	eristics	oς		
Circuit function	Туре	Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)	Package Outlines	Interchangeable products	Page
4-Bit Magnitude Comparator	M74LS85P	13	55	8	0.4	16P4	74LS85	2-86
	M74LS682P	20	210	24	0.4	20P4	74LS682	2-452
	M74LS683P	24	210	24	_	20P4	74LS683	2-456
8-Bit Magnitude Comparator	M74LS684P	20	200	24	0.4	20P4	74LS684	2-459
o-Bit Magnitude Comparator	M74LS685P	24	200	24		20P4	74LS685	2-462
•	M74LS688P	14	200	24	0.4	20P4	74LS688	2-465
	M74LS689P	22	200	24		20P4	74LS689	2-468

PARITY GENERATOR/CHECKER

9-Bit Odd/Even parity Generator/Checker	M74LS280P	18	80	8	. 0.4	14P4	74LS280	2-310

ADDER

		Typical	Typical propag	ation time (ns)	age	Interchangeable	D
Circuit function	Туре	dissipation (mW)	Carry time	Add time	Package Outlines	products	Page
4-Bit Binary Full Adder with Fast Carry	M74LS83AP	102.5	8	12	16P4	74LS83A	2-83
4-Bit Binary Full Adder with Fast Carry	M74LS283P	102.5	- 8	12	16P4	74LS283	2-313

REGISTER FILES

Circuit fundament	Tuno	Typical power	'' ' '	ation time (ns)	age	Interchangeable	Page
Circuit function	Туре	(mW)	Write time	Read time	Pack	products	lage
4-By-4 Register File with Open Collector Outputs	M74LS170P	125	15	16	16P4	74LS170	2-207
4-By-4 Register File with 3-State Output	M74LS670P	150	12	13	16P4	74LS670	2-449
4-Bit D-Type Register with 3-State Output	M74LS173AP	85	_	_	16P4	74LS173A	2-210

Refer to LATCH and REGISTER sections for M74LS173AP specifications.



SYMBOLOGY

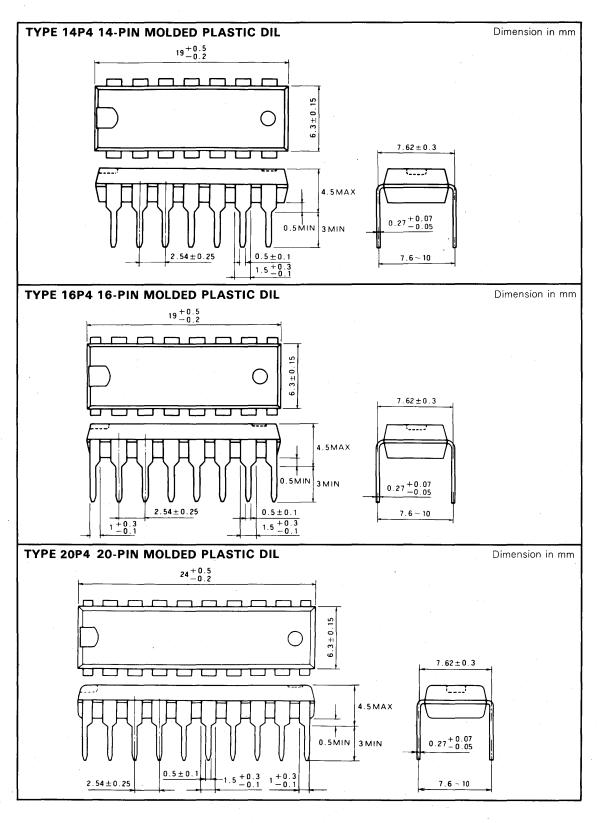
Symbol	ļ	Descriptions
CL	Load capacitance	Extenally connected load capacitance
fmax	Maximum clock frequency	Maximum input repetition frequency for normal IC operation.
۴ı	Fan-in	Number of similar inputs
Fo	Fan-out .	Number of similar ICs which can be driven by an output
Н	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level
I	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative
Icc	Supply current	The current flowing into the V _{CC} supply terminal of a circuit
ICCL	Low-level supply current	V _{CC} current when the inputs are such that the output is low.
Іссн	High-level supply current	V _{CC} current when the inputs are such that the output is high.
I _{CCZ}	High-impedance supply current	V _{CC} current when the inputs are such that the output is in the high-impedance state.
lF	Forward current	Forward diode current
l _t	Input current	Input current flowing into the IC pin when a voltage is applied.
l _{iH}	High-level input current	The current flowing into an input when a specified high voltage is applied.
I _{IL}	Low-level input current	The current flowing out of an input when a specified low voltage is applied.
1он	High-level output current	Current flowing in the load when the output is high or current flowing when a high level is applied
IoL	Low-level output current	The current flowing into an output which is in the low state
los	Short-circuit output current	The current flowing out of an output which is in the high state when that output is short circuit to group
lozh	Off-state high-level output current	The current flowing into a disabled 3-state output with a specified high output voltage applied
IozL	Off-state low-level output current	The current flowing out of a disabled 3-state output with a specified low output voltage applied
I _T	Threshold current	Current which flows when the threshold voltage is applied to the input
I _{T+}	Positive threshold current	Current which flows when the positive threshold voltage is applied to the input
Iτ _	Negative threshold current	Current which flows when the negative threshold voltage is applied to the input
Ĺ	Indicates the low logic level	Used in voltage and current suffixes to indicate the low potential level
0	Indicates output	
Pd	Power dissipation	Product of the supply voltage and the supply current
PRR	Pulse repetition rate	The rate of repetition of an applied pulse train
Ta	Operating free-air temperature	The temperature of the environment surrounding an IC
t _f	Falltime	Time required to fall from the high to the low logic level
t _h	Hold time	The required hold time for a specified input after an input has changed
t _{latch}	Latch time	The time from the latching action of input data until the data appears in the output
Topr	Operating temperature	The ambient temperature range for normal IC operation
t _{pd}	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output,
-pu	I spagation acidy time	expressed as the average propagation time.
t _{PHL}	Propagation delay time, high-to-low-level output	Amount of time required from a change of input signal until the output changes from high to low.
t _{PHZ}	Output disable time from High level	Amount of time required from a change of input signal until the output changes from high to
PHZ	Couput disable time from Fight level	
t _{PLH}	Propagation delay time, low-to-high-level output	high-impedance. Amount of time required from a change of input signal until the output changes from low to high.
t _{PLZ}	Output disable time from Low level	Amount of time required from a change of input signal until the output changes from low to high-impedance.
t _w	Pulse width	The time required for a pulse to change from one specified level to another.
t _{wo}	Output pulse width	The width of the pulse appearing in the output of a monostable multivibrator
t _{PZH}	Output enable time to a High level	Amount of time required from a change of input signal until the output changes from high-impedance to high.
t _{PZL}	Output enable time to a Low level	Amount of time required from a change of input signal until the output changes from high-impedance to low.
tr	Risetime	Time required to rise from the low to the high logic level
	Recovery time	Time from the point at which the input states are cancelled until the next clock pulse may be applied.
trec	Storage temperature	
Tstg •		The range of surrounding storage temperature for an IC.
t _{su}	Setup time	The required hold time for other inputs before a particular input may be changed.
Vcc	Supply voltage	The voltage of power supply voltage over which the device is guaranteed to operate within the specified limits.



Symbol		Descriptions
V _{BE}	Base-emitter voltage	
VF	Forward voltage	Forward voltage applied to a diode
V _I	Input voltage	Voltage applied to an input
Vic	Input clamp diode voltage	The forward voltage applied to an input clamping diode.
VIE	Input emitter-emitter voltage	The emitter-to-emitter voltage for a multi-emitter transistor input.
ViH	High-level input voltage	The range of input voltages that represents a logic high in the system.
VIL	Low-level input voltage	The range of input voltages that represents a logic low in the system.
Vo.	Output voltage	Voltage applied to or appearing at an output
VoH	High-level output voltage	Voltage at an output in the high state
VoL	Low-level output voltage	Voltage at an output in the low state
V _P	Pulse amplitude	The difference between the low level and high level of a pulse.
v _T	Threshold voltage	The input voltage beyond at which the output changes
V _{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to hig
V _T -	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changing from high to lo
Z	Indicates the off-state	Indicates that the output is in the high-impedance state.
	Output impedance	The load impedance which should be connected to such devices as pulse generators.



MITSUBISHI LSTTLS PACKAGE OUTLINES





2

DATA SHEETS

SCHEMATICS OF INPUTS AND OUTPUTS INDIVIDUAL DATA







Schematics of inputs and outputs of the M74LS00P series are shown in I-1 \sim I-11 and in 0-1 \sim 0-17, respectively, for devices whose circuit diagrams are not given in the individ-

ual data. Reference should be made when circuitry is being designed.

SCHEMATICS OF INPUTS AND OUTPUTS

Type designation		Schematics of inpu	ts	1	Schematics of ou	tputs		
r ype designation	Fig.	R (Ω)	Pin	Fig.	R (equivalent	resistance) Ω		
M74LS42P	I -1	17k	All inputs	0-1	120			
	I -1	25k	D _A ~D _D	0-2		_		
M74LS47P	I -1	20 k	LT, RBI	1 0 2		_		
	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20 k	BI/RBO		
	I -1	25k	D _A ~D _D	0-3	2k			
M74LS48P	I -1	20 k	LT, RBI] 0-3	2 K			
	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20 k	BI/RBO		
	I -1	26k	Ј, К					
M74LS73AP	I -1	9k	Ŧ	0-14	120			
	I -3	9k	, R _D	1				
	I -3	8k	SD, RD					
M74LS74AP	I -4	18k	Т	0-14	120			
	I -5	31k	D	1				
	I -1	18k	100					
M74LS75P	I -1	4.5k	E	0-15	120			
	I -1	26k	J,K					
M74LS76AP	I -1	9 k	Ŧ	0-14	120			
	I -3	9 k	S _D , R _D					
	I -1	18k	Co					
M74LS83AP	I -1	9 k	A ₁ ~A ₄ , B ₁ ~B ₄	0-1	120			
	I -6	17k	A <b, a="">B</b,>					
M74LS85P	I -7	R ₁ =15k, R ₂ =8.5k	I _{A=B}	0-1	120			
	I -7	R ₁ =8.5k, R ₂ =17k	A ₀ ~A ₃ , B ₀ ~B ₃	-				
· · · · · · · · · · · · · · · · · · ·	I -1	17k	S _{D(9)1} , S _{D(9)2} , R _{D1} , R _{D2}		R=120, R ₁ =17k			
M74LS90P	I -8	R ₁ =8.5k, R ₂ =8.5k, R ₃ =8.5k		0-13	R ₂ =17k, R ₃ =9k	Qв		
•	I -8	R ₁ =5.8k, R ₂ =5.8k, R ₃ =4.4k		0-15	120	QA,QC,QD		
	I -1	26k	D _{S1} , D _{S2}					
M74LS91P	I -1	19k	Т	0-15	120			
	I -1	17k	R _{D1} , R _{D2}	1	R=120, R ₁ =17k			
M74LS92P	I -8	R ₁ =8.5k, R ₂ =8.5k, R ₃ =8.5k	<u>T1</u>	0-13	R ₂ =17k, R ₃ =9k	Qc		
	I -8	R ₁ =5.8k, R ₂ =5.8k, R ₃ =4.4k	<u>T₂</u>	0-15	120	Q _A , Q _B , Q _D		
-	I -1	17k	R _{D1} , R _{D2}	0-15	120	QA, QD		
		R ₁ =8.5k, R ₂ =8.5k		-	R=120, R ₁ =17k			
M74LS93P	I -8	R ₃ =8.5k	<u>T</u> 1		R ₂ =17k, R ₃ =9k	Qв		
		R ₁ =13k, R ₂ =13k		0-13	R=120, R ₁ =10k			
	I -8	R ₃ =9k	T ₂		R ₂ =10k, R ₃ =9k	Qc		
	I -1	17k	TR, TL		,			
M74LS95BP	I -1	9 k	M/C	0-15	120			
, +_0,00	I -1	20k	D _S , D ₀ ~D ₃	" "				

Note: All resistances given are typical values.



Tura designation		Sc	hematics of inputs		Schematics of outputs
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω
	I -1	26k	Ds		
M74LS96P	I -1	18k	R _D , T, S _{D0} ~S _{D4}	0-15	120
	I -1	3.4k	LOAD		
	I -1	26k	J, K		
M74LS107AP	I -1	9 k	Ŧ	0-14	120
	1 -3	9 k	RD		
	I -3	8 k	S _D , R _D		
M74LS109AP	I -4	18k	Т	0-14	120
	I -5	31k	J, K		
	I -1	24k	J, K		
M74LS112AP	I -1	9 k	Ŧ	0-14	120
	I -3	9 k	S _D , R _D		
	I -1	24k	J, K		
M74LS113AP	I -1	9 k	Ŧ	0-14	120
	1 -3	9 k	S _D		
	I -1	24k	J, K		
	I -1	4.8k	T		
M74LS114AP	I -3	9 k	SD	0-14	120
	I -3	4.5k	RD		
M74LS122P	I -1	17k	All inputs	0-1	120
M74LS123P	I -1	17k	All inputs	0-1	120
WIT+E31201	1-9	15k	D ₀ ~D ₃		120
M74LS137P	I - 1	20k	E ₁ , E ₂ , E _L	0-5	120
	I - 9	10k	D ₀ ~D ₃	0-5	120
M74LS138P	I -1	20 k	$E_1, \overline{E_2}, \overline{E_3}$	0-5	120
M74LS139P	I -1	17k	All inputs	0-1	120
M74LS145P	I -1	17k	All inputs	0-6	_
M74LS147P	I -1	17k	All inputs	0-5	120
	I -1	-17k	D ₀ , Ē		
M74LS148P	I -1	9 k	$\overline{D_1} \sim \overline{D_7}$	0-5	120
M74LS151P	I -1	17k	All inputs	0-1	120
M74LS153P	I -1	17k	All inputs	0-1	120
M74LS155P	I -1	17k	All inputs	0-1	120
M74LS156P	I -1	17k	All inputs	0-7	<u></u>
	I -1	17k	1D ₀ ~4D ₀ , 1D ₁ ~4D ₁		
M74LS157P	I -1	8.5k	SA, G	0-1	120
	I -1	17k	1D ₀ ~4D ₀ , 1D ₁ ~4D ₁		
M74LS158P	I -1	8.5k	S _A , \overline{G}	0-1	120
	I -1	20 k	$D_A \sim D_D$, T, E _P , $\overline{R_D}$		
M74LS160AP	I -1	9 k	E _T , LOAD	0-15	120
	I -1	20 k	$D_A \sim D_D$, T, E_P , $\overline{R_D}$		
M74LS161AP	I -1	9 k	E _T , LOAD	0-15	120
	I -1	20 k	D _A ~D _D , T, E _P		
M74LS162AP	I -1	9 k	$E_T, \overline{R}, \overline{LOAD}$	0-15	120
M74LS163AP	I -1	2011	D _A ~D _D , T, E _P	0-15	120
	I -1	9 k	E _T , R, LOAD		



		Schematics of in	outs		Schen	natics of outputs
Type designation	Fig.	R (Ω)	Pin	Fig.	R	(equivalent resistance) Ω
M74LS164P	I -1	20 k	All inputs	0-15	120	
-	I -9	9 k	T, TINH, LOAD			
M74LS165AP	I -1	18k	D ₀ ~D ₇	0-8	120	
	I -1	22k	Ds	7		
-	I -9	9 k	RD, LOAD, T, TINH		100	
	I -1	18k	D ₀ ~D ₇	0-8	120	
M74LS166AP	I -9	12k	LOAD		100	
	I -1	22k	Ds	0-8	120	
	I -1	8.5k	E _R , E _W		-	
M74LS170P	I -1	17k	D ₀ ~D ₃ , R _A , R _B , W _A , W _B	0-2		- .
M74LS173AP	I -1	19k	All inputs	0-9	100	
	I -1	17k	T, RD	1		
M74LS174P	I -1	30 k	D ₀ ~D ₅	0-15	120	
	I -1	17k	T, RD			
M74LS175P	I -1	30 k	D ₀ ~D ₃	0-15	120	
	I -1	5.7k	Ē			· ·
M74LS190P	I -1	17k	All inputs except E	0-15	120	
	I -1	5.7k	Ē			
M74LS191P	I -1	17k	All inputs except \overline{E}	0-15	120	
	I -1	23 k	D _A ~D _D			·
M74LS192P	I -1	17k	T _U , T _D , R _D , LOAD	0-15	120	
	I -1	23 k	D _A ~D _D	0-15 120		
M74LS193P	I -1	17k	T _U , T _D , R _D , LOAD	0-15	120	
	I -1	25k	D _{SR} , D _{SL} , D ₀ ~D ₃			
M74LS194AP	I -1	17k	T, RD, M/C1, M/C2	0-15	120	
	I -1	20k	J, K, D ₀ ~D ₃ , M/C			4
M74LS195AP	I -1	17k	T, RD	0-15	120	
	I -1	17k	DA~DD, LOAD			
	I -1	8.5k	$\overline{R_D}$	1 .		
M74LS196P	I -8	R ₁ =5.7k, R ₂ =6.5k, R ₃ =7k	T ₁	0-15	120	
	I -8	R ₁ =5.7k, R ₂ =5.7k, R ₃ =5.7k	T ₂	1	-	
	I -1	17k	DA~DD, LOAD			
	I -1	8.5k	RD	1	1	
M74LS197P	I -8,	R ₁ =5.7k, R ₂ =6.5k, R ₃ =7k	T ₁	0-15	120	
	I -8	R ₁ =14k, R ₂ =13k, R ₃ =13k	T ₂	1		
	I -1	24k	Ā	1		
		R ₁ =45k, R ₂ =24k, R ₃ =9.5k		1		
M74LS221P	I -11	R ₄ =14k, R ₅ =1.7k	B	0-1	120	
		R ₁ =12k, R ₂ =9.5k		1		
	I -10	R ₃ =14k, R ₄ =1.7k	$\overline{R_D}$			
	I -1	25k	D _A ~D _D	<u> </u>	-	
M74LS247P	I -1	20k	LT, RBI	0-2		_
v ·	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20	ok BI/RBO
	I -1	25k	D _A ~D _D	· · · · · · · · · · · · · · · · · · ·	-	
M74LS248P	I -1	20k	LT, RBI	0-3		2k
	I -2	R _{IN} =10k	BI/RBO	I-2	R _{OUT} =20	ok BI/RBO



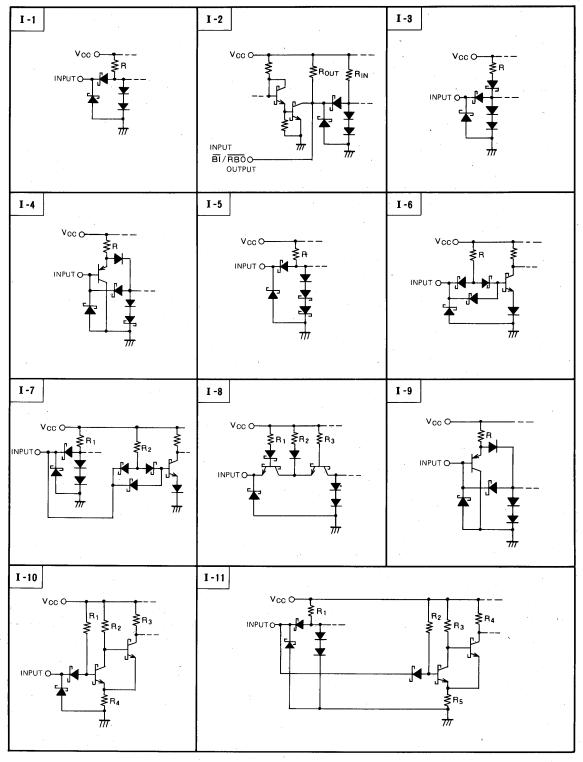
		Schematics of in	nputs	.,	Schematics of ou	tputs	
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivalent	resistance) Ω	
M74LS251P	I -1	17k	All inputs	0-11	100		
14741 00500	I -1	19k	SA, SB, 100, 200	0-4	100		
M74LS253P	I -1	17k	1D ₀ ~1D ₃ , 2D ₀ ~2D ₃	0-12	100		
	I -1	17k	SA, SB, 1D, 2D, R	0.10	100		
M74LS256P	I -9	9.5k	M/C	0-16	120		
M74LS257AP	I -1	8.5k	S _A	0-9	100		
M/4L525/AP	I -1	17k	OC, 1D ₀ ~4D ₀ , 1D ₁ ~4D ₁] "-3	100		
M74LS258AP	I -1	8.5k	SA	0-9	100		
	I -1	17k :	OC, 1D ₀ ~4D ₀ , 1D ₁ ~4D ₁				
M74LS259P	I -1	17k	S _A ~S _C , D, R	0-16	120		
	I -9	9.5k	M/C	1			
M74LS273P	I -1	17k	T, RD	0-15	120		
	I -5	28k	1D~8D				
M74LS280P	I -1	20 k	All inputs	0-1	120		
M74LS283P	I -1	18k	Co	0-1	120		
	I -1	9 k	A ₁ ~A ₄ , B ₁ ~B ₄				
	I -1	17k	S _{D(9)1} , S _{D(9)2} R _{D1} , R _{D2}	0-13	$R=120, R_1=17k$	Qв	
M74LS290P	I -8	$R_1 = 8.5 k, R_2 = 8.5 k, R_3 = 8.5 k$	· T ₁		R ₂ =17k, R ₃ =9k		
	I -8	R ₁ =5.8k, R ₂ =5.8k, R ₃ =4.4k	T ₂	0-15	120	QA, QC, QD	
	I -1	17k	R _{D1} , R _{D2}	0-15	120	QA, QD	
	I -8	R ₁ =8.5k, R ₂ =8.5k	T 1		R=120, R ₁ =17k	Qв	
M74LS293P		R ₃ =8.5k		0-13	R ₂ =17k, R ₃ =9k		
	I -8	$R_1 = 13k, R_2 = 13k$	T ₂		R=120, R ₁ =10k	Qc	
-		R ₃ =9k		ļ	R ₂ =10k, R ₃ =9k		
	I - 1	18k	T				
M74LS295BP	I -1	20k	0C, M/C	0-9	100		
	I -5	30k	Ds	-			
	I -5	20k	D ₀ ~D ₃			·.	
M74LS298P	I -1	17k	Ť	0-15	120		
	I -1	20 k	S _A , 1D ₀ ~4D ₀ , 1D ₁ ~4D ₁				
	I -1	10k	M/C ₁ , M/C ₂	0-9	100	Q ₀ ~Q ₇	
M74LS299P	I -1	20k	OC ₁ , OC ₂ , R _D , T	 	400	0' 0'	
	I -5	20 k	D _{SR} , D _{SL} , D ₀ ~D ₇	0-1	120	Q' ₀ , Q' ₇	
44741 00	I -1	10k	M/C ₁ , M/C ₂	0-9	100	Q ₀ ~Q ₇	
M74LS323P	I -1	20 k	OC ₁ , OC ₂ , R _D , T	-	100	0′ 0′	
-	I -5	20k	D _{SR} , D _{SL} , D ₀ ~D ₇	0-1	120	Q ₀ , Q ₇	
M74LS352P	I -1	1.9k	S _A , S _B , 1G, 2G	0-1	120		
	I -1	17k	1D ₀ ~1D ₃ , 2D ₀ ~2D ₃	ļ		•	
M74LS353P	I -1	19k	S _A , S _B , 100, 200	0-12	100		
	I -1	17k	1D ₀ ~1D ₃ , 2D ₀ ~2D ₃				
M74LS373P	I -1	17k	1D~8D	0-9	100		
	I -9	9 k	E, 00				
M74LS374P	I -1	30k	1D~8D	0-9	100		
· · · · · · · · · · · · · · · · · · ·	I -9	9 k	т, ос	<u> </u>			



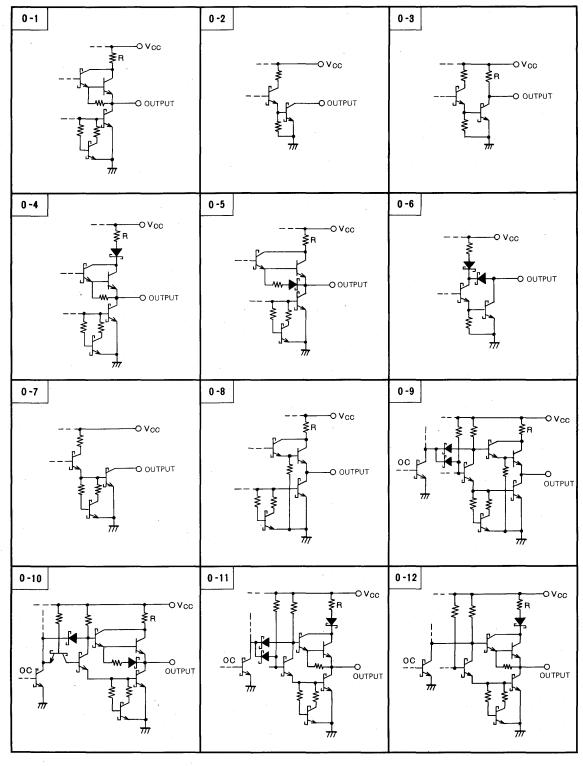
T a design still		Schematics of inp	outs		Schematics of o	outputs
Type designation	Fig.	R (Ω)	Pin	Fig.	R (equivaler	nt resistance) Ω
M741 C075D	I -1	18k	1D~4D	0.15	120	
M74LS375P	I -1	4.5k	1-2E, 3-4E	0-15	120	
	I -1	17k	T, Ē	2.45	100	
M74LS377P	I -5	28 k	1D~8D	0-15	120	
	I -1	17k	R _D			
M74LS390	I -8	R ₁ =14k, R ₂ =14k, R ₃ =14k	T ₁	0-17	120	
	I -8	R ₁ =8.5k, R ₂ =8.5k, R ₃ =8k	T ₂	7		
	I -1	17k	R _D	1	100	
M74LS393P	I -8	R ₁ =14k, R ₂ =14k, R ₃ =14k	Ŧ	0-17	120	
	I -1	18k	Ŧ	1		
	I -1	20k	OC, M/C, RD	0-9	100	Q ₀ ~Q ₃
M74LS395AP	I -5	30 k	Ds	7		
	I -5	20k	D ₀ ~D ₃	0-17	120	Q'3
M74LS423P	I - 1	17k	All inputs	0-1	120	
	I -1	17k	S _{D(9)} , R _D			
M74LS490P	I -8	R ₁ =14k, R ₂ =14k, R ₃ =14k	Ŧ	0-17	120	
	I - 1	19k	Ds	0-9	Q0~Q7	
M74LS595P	I -9	13k	その他	0-8	Q7′	
	I - 1	19k	Ds	0-2	Q0~Q7	
M74LS596P	I - 9	13k ⁽	その他	0-8	Q7′	
	I -1	8.5k	LOAD			
M74LS668P	I -1	17k	U/\overline{D} , T, \overline{E}_{P} , \overline{E}_{T}	0-15	120	QA,QB QC,QD
	I -5	20k	D _A ~D _D	0-1	120	RCO
	I -1	8.5k	LOAD			
M74LS669P	I -1	17k	U/D, T, EP, ET	0-15	120	QA,QB,QC,QD
	I -5	20 k	D _A ~D _D	0-1	120	RCO
	I -1	8.5k	Ew			
M74LS670P	I -7	R ₁ =8.5k, R ₂ =17k	ŌĊ	0-10	120	
	I -1	17k	R _A , R _B , W _A , W _B , D ₀ ~D ₃	7	1	
	I - 9	14k	P0~P7			
M74LS682P	I - 12	R ₁ =14k, R ₂ =24k	Q0~Q7	0-5	100	
	I - 9	14k	P0~P7	1.		
M74LS683P	I - 12	R ₁ =14k, R ₂ =24k	Q0~Q7	0-7	-	
M74LS684P	I - 9	14k	全入力	0-5	100	
M74LS685P	I - 9	14k	全入力	0-7	_	_
M74LS688P	I - 9	14k	全入力	0-5	100	
M74LS689P	I - 9	14k	全入力	0-7		

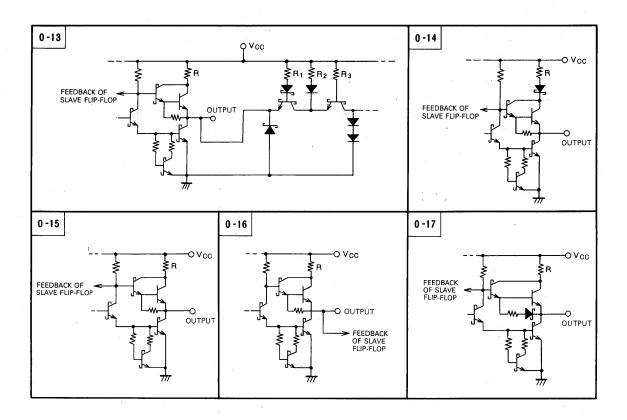


Schematics of inputs



Schematics of outputs





QUADRUPLE 2-INPUT POSITIVE NAND GATES

DESCRIPTION

The M74LS00P is semiconductor integrated circuit containing four dual-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 8mW typical)
- High speed (tpd = 6ns typical)
- · Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATIONS

General purpose, for use in industrial and consumer equipment.

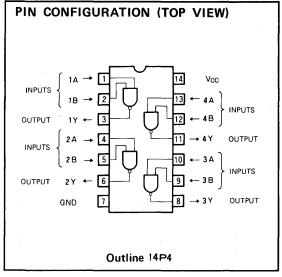
FUNCTIONAL DESCRIPTION

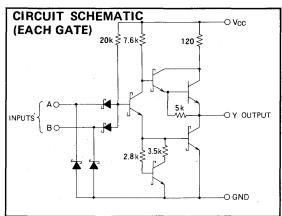
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, and low power consumption as well as high fan-out.

When both A and B inputs are high the output Y is low. When either A or B input is low the output Y is high.

FUNCTION TABLE

Α	В	Y
L ·	٦	H
Н	L	Н
L	I	Н.
н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5∼+15	V
Vo	Output voltage	High-level state	-0.5 ~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20 ∼ + 75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NAND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Cb.al	mbol Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Voc	Supply voltage		4.75	5	5.25	·V		
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА		
	1 - 1 - 1 - 1 - 1 - 1	V _{OL} ≤0.4V	0		4	mA		
loL	Low-level output current	V ₀ L≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

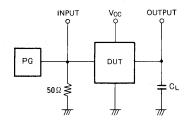
	B	T		Limits			11-14
Symbol	Parameter	Test o	Test conditions		Тур*	Max	Unit
VIH	High-level input voltage			2			. V
V _{IL}	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	= — 18mA			-1.5	٧
Voн	High-level output voltage	V _{CC} =4.75V, V _I =	0.8V, I _{OH} =-400µA	2.7	3.4		٧
	Lauriani anti-trans	V _{CC} =4.75V	I _{OL} = 4mA	7111111111111	0.25	0.4	٧
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	٧
	High to all in our annual	V _{CC} =5.25V, V _I =	2.7V			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
h∟	Low-level input current	V _{CC} =5.25V, V ₁ =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	0V	- 20		- 100	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	0∨		0.8	1.6	mΑ
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		2.4	4.4	mA

^{* :} All typical values are at $V_{CC} = 5V$, Ta = 25° C.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

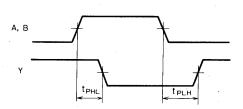
Symbol	Parameter	Test conditions		Limits		
Symbol	Symbol Farameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF	-	6	· 15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		6	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P.P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE NOR GATES

DESCRIPTION

The M74LS02P is a semiconductor integrated circuit containing 4 dual-input positive NOR and negative NAND gates.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 10mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment,

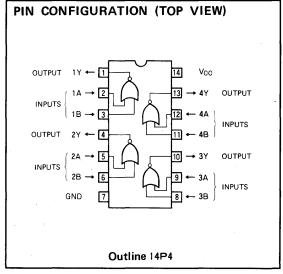
FUNCTIONAL DESCRIPTION

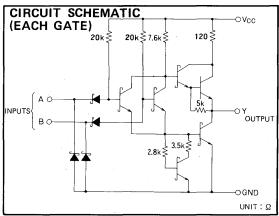
The use of Schottky TTL technology, enables the achievement of high input voltage, high speed, low power dissipation, and high fan-out.

When at least input A or input B is high, output Y is low, and when both A and B are low, Y is high.

FUNCTION TABLE

- Α	В	Υ
L	Г	Н
н	L	L
L	I	L
Ξ	Η	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		- 20~ + 75	°C
Tstg	Storage temperature range	·	- 65~ + 150	°C

QUADRUPLE 2-INPUT POSITIVE NOR GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Unit			
Symbol	rarameter	Laranne ret		Тур	Max	Unit
. Voc	Supply voltage		4.75	5	5.25	٧
I _{OH}	High-level output current	V _{OH} ≧2.7V	0		- 400	μА
		V ₀ L≦0.4V	0		4	mA.
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

		_			Limits		11-1
Symbol	Parameter	Test	conditions	Min	Тур*	Max	Unit
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	= — 18mA	,		-1.5	V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =	$V_{CC} = 4.75V, V_1 = 0.8V, I_{OH} = -400 \mu A$		3.4		V
	Law law law and a selection	V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
V _{OL} .	Low-level output voltage	V ₁ =2V	I _{OL} = 8mA		0.35	0.5	V
	High level input ourront	V _{OC} =5.25V, V _I =	2.7V			20	μΑ
ЙН	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	, mA
los	Short-circuit output current (Note 1)	V _{OC} =5.25V, V _O =	=0V	-20		-100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =	= 0V		1.6	3.2	mA
Icol	Supply current, all outputs low	V _{CC} =5.25V, V _I =	= 4.5V		2.8	5.4	mA

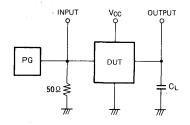
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		11-14
Symbol Parameter		rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		6	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		6	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_{P-P} , Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.



tpLH

TIMING DIAGRAM (Reference level = 1.3V)

MT4LSO3P

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS03P is a semiconductor integrated circuit containing four dual-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in AND-Tie connection
- High breakdown input voltage (V_I ≥ 15V)
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (P_d = 8mW typical)
- High speed (tpd = 10ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

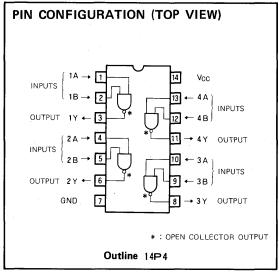
FUNCTIONAL DESCRIPTION

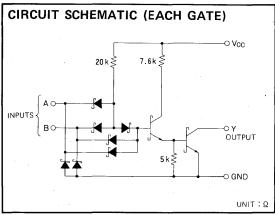
With use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

When inputs A and B are high, output Y is low and when one or both inputs are low, the output Y is high.

FUNCTION TABLE

Α	В	Υ
[·, L	٦	H .
Н	L	н
L	Н	н
Н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		- 65~ + 150	°C

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Combat	Parameter			Unit		
Symbol			Min	Тур	Max	Omit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		100	μА
loL	Low-level output current	V _{OL} ≦0.4V	0		4	mA
		V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

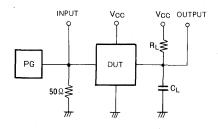
0	Parameter				Limits		
Symbol		l est co	onditions	Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18 mA				-1.5	V
Іон	High-level output current	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{O}=5.5V$				100	μΑ
VoL	Low-level output voltage	V _{CC} =4.75V V _I =2V	I _{OL} =4mA		0.25	0.4	V
L	III de la constanta de la cons	V _{CC} =5.25V, V _I =	2.7V			20	μΑ
Iн	High-level input current	V _{CC} =5.25V, V ₁ =	10V ·			0.1	mA
lı.	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
Іссн	Supply current, all inputs high	V _{CC} =5.25V, V _I =0V			0.8	1.6	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		2.4	4.4	mA

^{* :} All typical values are at V_{CC}=5V, Ta=25°C

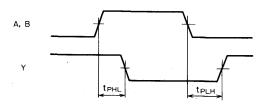
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol Parameter	Test conditions					
			Min	Тур	Max	Unit
tpLH	Low-to-high-level/high-to-low-level	R _L = 2 kΩ		- 10	32	ns
tpHL	Output propagation time	$C_L = 15 pF$ (Note 1)		10	28	ns

Note 1: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_{P-P} , Z_Q = 50 Ω
- (2) CL includes probe and jig capacitance.



M74LS04P

HEX INVERTERS

DESCRIPTION

The M74LS04P is a semiconductor integrated circuit containing 6 inverter circuits.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 12mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

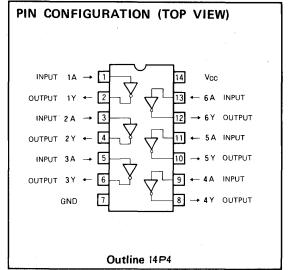
FUNCTIONAL DESCRIPTION

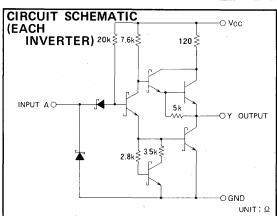
The use of Schottky TTL technology enables the achievement of high input voltage, high speed, low power dissipation and high fan-out.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

Α	Y
L	Н
Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter					
			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μА
		V _{OL} ≤0.4V	0	***************************************	4	mΑ
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	Parameter	T	Test conditions		Limits		
Symbol		lest			· Typ*	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
VoH	High-level output voltage	$V_{OC} = 4.75V$, $V_1 = 0.8V$, $I_{OH} = -400 \mu A$		2.7	3.4		V
		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output voltage	V₁= 2V	I _{OL} =8mA		0.35	0.5	V
1	Mich I and in a second	V _{CC} =5.25V, V _I =	2.7V			20	μА
Ин	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
IccH	Supply current, all outputs high	V _{CC} =5.25V, V _I =	=0V		1.2	2.4	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	=4.5V		3.6	6.6	mA

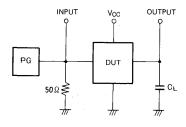
All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

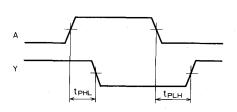
SWITCHING CHARACTERISTICS ($V_{CO}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Symbol Parameter	D	Total and distinct	Limits			Unit
	rarameter	Test conditions			Max	Offic
t _{PLH}	High-to-low-level output propagation time	C _L =15pF		6	15	ns
t _{PHL}	Low-to-high-level output propagation time	(Note 2)		6	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- (2) C_L includes probe and jig capacitance.



HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS05P is a semiconductor integrated circuit containing 6 open collector output inverter circuits.

FEATURES

- Usable in AND-Tie connection.
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 12mW typical)
- High speed (tpd = 10ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

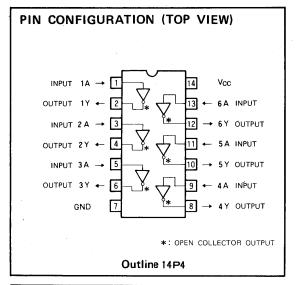
FUNCTIONAL DESCRIPTION

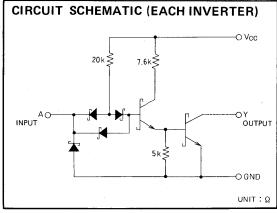
With the use of Schottky barrier diodes for the inputs and open-collector outputs, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection, which has been impossible with conventional gates.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

Α	Υ
L	н
Ι	Ŀ





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Unit		
Symbol Parameter		er	Min	Тур	Max	Offic
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		100	μА
		V _{OL} ≦0.4V	0 -		4	mA
IOL Low-level out	Low-level output current	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

	Parameter	T			Limits		
Symbol	Parameter	Test con	ditions	Min	Typ*	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
Гон	High-level output current	$V_{CC} = 4.75V, V_1 = 0.$	$V_{CC} = 4.75V, V_1 = 0.8V, V_0 = 5.5V$			100	μA
.,,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V .
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
1	High-level input current	V _{CC} =5.25V, V _I =2.7	7 V		,	20	μА
Ιн	High-level input corrent	V _{CC} =5.25V, V _I =10	V .			0.1	mA
I _I L .	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V	1	1	1.2	2.4	mΑ
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I = op	en	1	3.6	6.6	mA

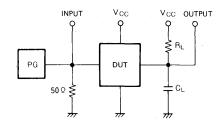
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

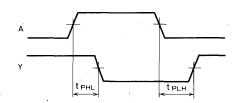
SWITCHING CHARACTERISTICS ($V_{OC} = 5V$, $Ta \approx 25^{\circ}C$, unless otherwise noted)

Combal	Symbol Parameter	Test and fishing		Limits		1 India
Symbol	Farameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	$R_L = 2 k\Omega$		10	32	ns
t _{PHL}	High-to-low-level output propagation time	C _L = 15pF (Note 1)		10	28	ns

Note 1: 'Measurement circuit

TIMING DIAGRAM (Reference level = 1.3V)





- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

M74LS08P

QUADRUPLE 2-INPUT POSITIVE AND GATES

DESCRIPTION

The M74LS08P is a semiconductor integrated circuit containing 4 dual input-positive AND and negative OR gates.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 17mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

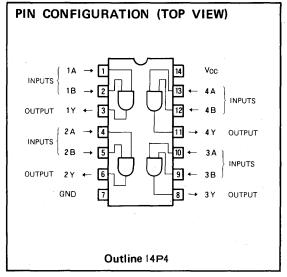
FUNCTIONAL DESCRIPTION

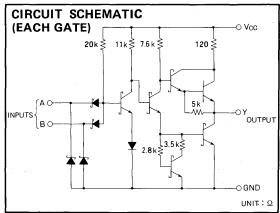
The use of Schottky TTL technology, enables the achievement of high input voltage, high speed, low power dissipation, and high fan-out.

When both inputs A and B are high, output Y is high, and when either or both of the inputs are low, Y is low.

FUNCTION TABLE

Α	В	Y
L	Ĺ	L
н	L	L
L	н	L
Н	Н	н





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage	No.	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5-+'V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE AND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

			Limits			Unit	
Symbol	Paramete	er	Min	Тур	Max	Oill	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
		V ₀ L≦0.4V	0		4	mA	
lor re	Low-level output current V ₀ L≤0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

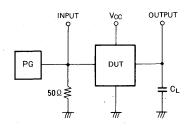
	Parameter	Took		Limits			
Symbol		rest	conditions	Min	Тур*	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	- — 18mA			-1.5	V
Voн	High-level output voltage	$V_{CC} = 4.75V, V_1 = 2V, I_{OH} = -400 \mu A$		2.7	3.4		٧
		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧
VoL	Low-level output voltage	V ₁ =0.8V	I _{OL} = 8mA		0.35	0.5	V
		V _{CC} =5.25V, V _I =	2.7V			20	μА
ин	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _C =	0V	- 20		- 100	mA
Toch	Supply current, all outputs high	V _{CC} =5.25V, V _I =	4.5V		2.4	4.8	mA
ICCL	Supply current, all outputs low	V _{OO} =5.25V, V _I =	0V		4.4	8.8	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

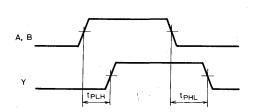
Cumbal	Symbol Parameter	Total or district		Limits		11.5
Syriboi	rarameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		9	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω

(2) C_L includes probe and jig capacitance.



Note 1: All measurement should be done quickly, and not more than one output should be shorted at a time.

M74LS09P

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS09P is a semiconductor integrated circuit containing 4 dual-input positive AND and negative OR gates with open collector output.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage (V₁ ≥ 15V)
- High breakdown output voltage (V_O ≥ 7V)
- Low power consumption (P_d = 17mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

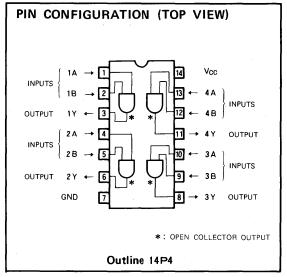
FUNCTIONAL DESCRIPTION

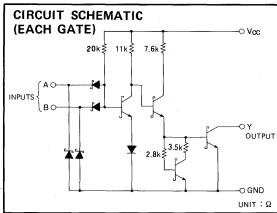
With the use of open collector output, the high-level output impedance can be freely selected by means of an external load resistor. This enables use in wire-AND, which has been impossible with conventional gates.

When both inputs A and B are high, output Y is high and when either or both of them are low, Y is low.

FUNCTION TABLE

Α	В	Υ
L	L	L
н	L	L
L	н	L
н	Н	Ħ





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5∼+15	v
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range	· ·	-20~+75	°C
Tstg	Storage temperature range		-65~+150	ో

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

				Limits			
Symbol	Parame	eter	Min	Тур	Max	Unit	
Voc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V ₀ =5.5V	0		100	μΑ	
		V _{OL} ≤0.4V	0		4	mA	
loL	Low-level output current	V _{0L} ≤0.5V	0	1	8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

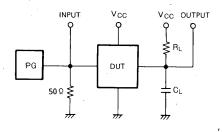
		T			Limits		11.24
Symbol	Parameter	l est c	Test conditions		Тур*	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
Гон	High-level output current	$V_{CC} = 4.75V$, $V_1 = 2V$, $V_0 = 5.5V$				100	μA
.,	Laurence and a service release	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =0.8V	I _{OL} =8mA		0.35	0.5	V
		V _{CC} =5.25V, V _I =3	2.7V			20	μА
ин .	High-level input current V _{CC} =5.25V, V _I =10V			0.1	mA		
l _I L	Low-level input current	V _{CC} =5.25V, V _I =1	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			2.4	4.8	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	V _{CC} =5.25V, V _I =4.5V		4.4	8.8	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

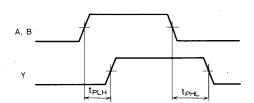
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol Parameter		T		Limits		
Symbol	i arameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	High-to-low-level output propagation time	$R_L = 2 k\Omega$		15	35	ns
t _{PHL}	Low-to-high-level output propagation time	C _L =15pF (Note 1)		10	35	ns

Note 1: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_0 = 50Ω
- (2) C_L includes probe and jig capacitance.



TRIPLE 3-INPUT POSITIVE NAND GATES

DESCRIPTION

The M74LS10P is a semiconductor integrated circuit containing three triple-input positive NAND and negative NOR gates.

FEATURES

- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (Pd = 8mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

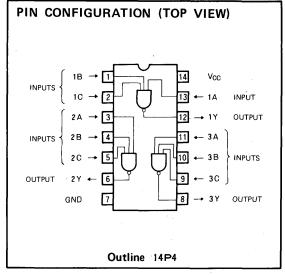
The use Schottky TTL technology has enabled the achievement of high input voltage, high speed, low power dissipation and high fan-out.

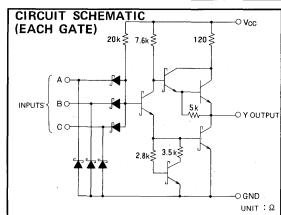
When all inputs A, B and C are high, output Y is low, and when one or more of the inputs is low, Y is high.

FUNCTION TABLE

Α	N	Y
L	L	н
Н	L	н
L ·	н	н
н	Н	L

N=B·C





ABSOLUTE MAXIMUM RATINGS ($T_a \approx -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		-65~+150	°C

TRIPLE 3-INPUT POSITIVE NAND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0				Limits		11-14
Symbol	Symbol Parameter		Min	Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mA
IOL	Low-level output current VoL≤0.5V		0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		Test conditions			Limits	7.	11.24
Symbol	Parameter	lest condi	tions	Min	Тур*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	٧
VoH	High-level output voltage	V _{CC} =4.75V, V ₁ =0.8	V, I _{0H} = -400μA	2.7	3.4		V
	Law law law and	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	V _{OL} Low-level output voltage	V ₁ = 2V	I _{OL} =8mA		0.35	0.5	V
l	IP-b I	V _{CC} =5.25V, V _I =2.7	/			20	μА
Іін	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
ИL	Low-level input current	V _{CC} =5.25V, V _I =0.4	/			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		– 20		100	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V		30.0	0.6	1.2	mA
FCCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5	V		1.8	3.3	mA

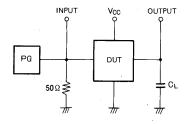
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

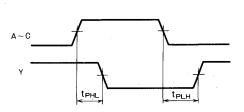
SWITCHING CHARACTERISTICS ($V_{OC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Pornantes	Test conditions	Limits '			Unit
Symbol	Parameter	(est conditions	Min	Тур	Max	Oilit
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		6	15	ns
tpHL	High-to-low-level output propagation time	(Note 2)		9	15	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω
- (2) C_L includes probe and jig capacitance,



M74LS11P

TRIPLE 3-INPUT POSITIVE AND GATE

DESCRIPTION

The M74LS11P is a semiconductor integrated circuit containing three triple-input positive AND and negative OR gates.

FEATURES

- High breakdown input voltage ($V_1 \ge 15V$)
- Low power dissipation (P_d = 13mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

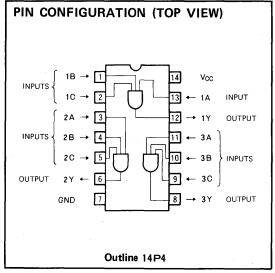
The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, lower power dissipation and high fanout.

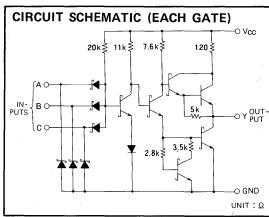
When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

Α	N	Y
L	L	L
Н	L	· L
L	н	L
Н	н	Н

 $N = B \cdot C$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit	
Voc	Supply voltage		-0.5~+7	V	
Vi	Input voltage		−0.5~+15	V	
V ₀	Output voltage	High-level state	-0.5~V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°C	

TRIPLE 3-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

	0			Limits		11-14
Symbol	nbol Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	- 5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
. 1	I _{OL} Low-level output current	V _O L≦0.4V	0		4	mA
IOL		V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Constant:	Parameter	Toot on	Test conditions		Limits		
Symbol	raraneter	rest co	nuttions	Min	Тур 🛊	Max	Unit
VIH	High-level input voltage			2			٧
VIL	Low-level input voltage				i.	0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =2	V, I _{OH} = - 400μA	2.7	3.4		V
	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	· V
¹ V _{OL}	Low-level output voltage	V ₁ =0.8V	I _{OL} =8mA		0.35	0.5	V
t	High-level input current	V _{CC} =5.25V, V _I =2	.7V			20	μΑ
ин	High-lever input current	$V_{CC} = 5.25V, V_I = 10$	0V .			0.1	mA
lıL .	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Icon	Supply current, all outputs high	V _{OC} =5.25V, V _I =4.5V			1.8	3.6	mΑ
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =0)V	1	3.3	6.6	mA

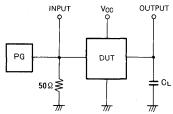
 $[\]star$: All typical values are at $\,V_{CC}\!=\!5V,\,\,T_a\!=\!25^\circ\!C.$

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

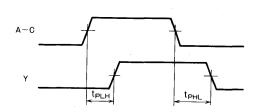
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter Test conditions		Limits			Unia
Yarameter	i di arrie (e)	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high output level propagation time	C _L =15pF		9	15	ns
t _{PHL}	High-to-low output level propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.



TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS12P is a semiconductor integrated circuit containing three triple-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage (V_i ≥ 15V)
- Low power dissipation (P_d = 6mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

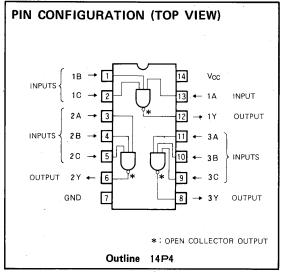
With the use of Schottky barrier diodes for the inputs and open-collector outputs, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

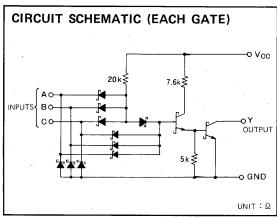
When inputs A, B and C are high, output Y is low and when one or more of the inputs is low, the output Y is high.

FUNCTION TABLE

A	N	Υ
L	L	Н
Н	L	H
L	Н	н .
Н	Н	L

 $N = B \cdot C$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	, Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~ + 75	°C
Tstg	Storage temperature range		-65 · +150	°C

TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter					
			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Юн	High-level output current	V ₀ =5.5V	0		100	μА
		V _{OL} ≦0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Total	anditions.	Limits			Unit
Symbol		Test ci	Test conditions			Max	Onit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
Гон	High-level output current	V _{CC} =4.75V, V ₁ =0.8V, V ₀ =5.5V				100	μА
	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL		V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
liн	High-level input current	V _{CC} =5.25V, V _I =	2.7V			20	μА
"H	riightiever input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
ItL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
t _{COH}	Supply current, all inputs high	V _{CC} =5.25V, V _I =0V			0.7	1.4	mA
ICOL	Supply current, all inputs low	V _{CC} =5.25V, V _I =	4.5V		1.8	3.3	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

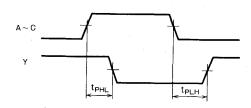
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			t testa in
		rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level/high-to-low level	$R_L = 2 k\Omega$		10	32	ns
tpHL	output propagation time	C _L =15pF (Note)		15	28	ns

Note: Measurement circuit

PG DUT VCC VCC OUTPUT

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.



DUAL 4-INPUT NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS13P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates having a Schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin
- High breakdown input voltage (V₁ ≥ 15V) (V₁ ≥ 15V, V_O ≥ 7V)
- Low power dissipation (P_d = 17.5mW typical)
- High speed (t_{pd} = 16ns typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

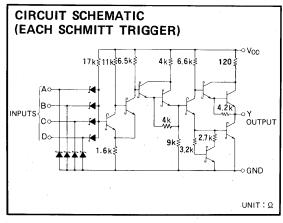
FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.8V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in a shaped waveform output without causing oscillation.

When inputs A, B, C and D are high, output Y is low, and when one or more of the inputs are low, Y is high.

Refer to M74LS14P for the typical characteristics.

PIN CONFIGURATION (TOP VIEW) INPUTS 1B → 2 NC 3 INPUTS 1C → 4 ID → 5 OUTPUT 1Y ← 6 GND 7 Outline 14P4 NC: NO CONNECTION



FUNCTION TABLE

Α	Ν	Υ
L	L	H
Н	L	Ι
L	н	Н
н	н	L

 $N = B \cdot C \cdot D$

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		- 65 ~ + 150	°C

DUAL 4-INPUT NAND SCHMITT TRIGGER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim \pm 75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits			
			Min	Тур	Max	Unit	
V _C C	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≧2.7V	0 .		-400	μА	
	Low-level output current	V _{OL} ≦0.4V	0		4	mA	
IOL		V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Cumbal	Parameter	Tost condi	tions	Limits			Unit
Symbol		rest condi	Test conditions		Typ *	Max	Offic
V _{T+}	Positive-going threshold voltage	V _{CC} =5V		1.4	1.6	1.9	V
V _T	Negative-going threshold voltage	V _{CC} =5V		0.5	0.8	1	٧
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =5V		0.4	0.8		V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =0.5V		2.7	3.4		V
	Low-level output voltage	$I_{OH} = -400 \mu A$ $V_{CC} = 4.75 V$	I _{OL} = 4mA	-	0.25	0.4	V
V _{OL}	Low-level output vortage	V ₁ =1.9∨	I _{OL} =8mA		0.35	0.5	٧ .
I _{T+}	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			-0.14		mA
I _T _	Input current at negative-going threshold	V _{CC} =5V, V _I =V _T -			-0.18		mA
I	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μА
I _{IH}	mign-leves imput current	V _{CC} =5.25V, V _I =10V	V _{CC} =5.25V, V _I =10V			0.1	mA
h_	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Icch ,	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			2.9	6	- mA
ICCL	Supply current, all outputs low	V _{CC} =5,25V, V _I =4.5	V		4.1	7	mΑ

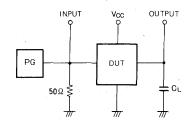
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

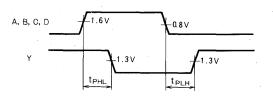
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Тур	Max	1 0///
tpLH	Low-to-high-level output propagation time	C _L =15 pF (Note 2)		12	22	ns
tpHL	High-to-low-level output propagation time			20	27	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM



M74LS14P

HEX SCHMITT TRIGGER INVERTERS

DESCRIPTION

The M74LS14P is a semiconductor integrated circuit containing 6 Schmitt trigger inverter circuits.

FEATURES

- Suitable for waveform shaping applications
- Wide hysterisis width (0.8V typical) and high noise margin
- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 51mW typical)
- High speed (tpd = 12ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

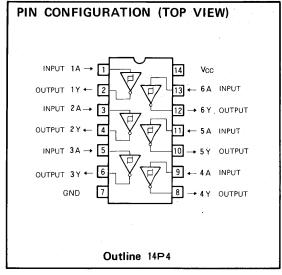
FUNCTIONAL DESCRIPTION

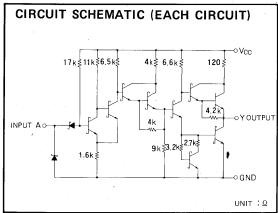
The use Schottly TTL technology has enabled the achievement of high input voltage, high speed, low power dissipation, and high fan-out. With positive feedback applied in the circuit, the hysterisis width is 0.8V (typical). Accordingly, noise margin is high. Even slow changing input signals result in a shaped waveform output without casing oscillation.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

Α	Y
L	н
н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter Conditions		Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		− 65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter						
Symbol			Min	Nom	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μА	
	Low-level output current	Low level output ourront	V _{OL} ≦0.4V	0		4	mΑ
loL		V _{OL} ≤0.5V	0		8	mA	



HEX SCHMITT TRIGGER INVERTERS

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

C		Tont	andisions :		Limits		Unit
Symbol	Parameter	lest	conditions	Min	Typ*	Max	Unit
V _{T+}	Positive-going threshold voltage	V _{CC} =5V		1.4	1.6	1.9	V
V _T	Negative-going threshold voltage	V _{CC} =5V		0.5	0.8	1	- V
V _{T+} -V _{T-}	Hysteresis	V _{CC} =5V		0.4	0.8		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
Voн	High-level output voltage	$V_{OC} = 4.75V$, $V_{I} = 0.5V$ $I_{OH} = -400 \mu A$		2.7	3.4		٧
.,		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =1,9V	I _{OL} =8mA		0.35	0.5	V
1 _T +	Input current at positive-going threshold	V _{CC} =5V, V _I =V _T	+ .		-0.14		mA
Iτ.	Input current at negative-going threshold	V _{CC} =5V, V _I =V _T			-0.18		mA
	High-level input current	V _{CC} =5.25V, V _I =	2.7V			20	μА
ин	nigh-lever input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
h_	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	=0V	-20		- 100	mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	0V		8.6	16	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		12	21	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

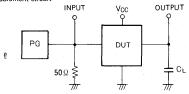
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

Symbol	Symbol Parameter	Test conditions		Limits		Unit
Gymbo.	T drameter	Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level output propagation time	O - 15 - F (New 2)		12	22	ns
t _{PHL}	High-to-low-level output propagation time	C _L =15pF (Note 2)		12	22	ns

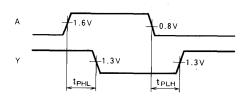
Note 2: Measurement circuit

OUTPUT VOLTAGE Vo (V)



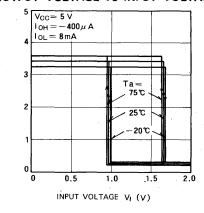
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM

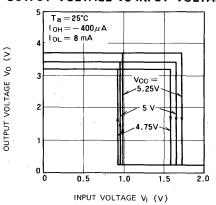


TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS INPUT VOLTAGE



OUTPUT VOLTAGE VS INPUT VOLTAGE



TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS15P is a semiconductor integrated circuit containing 3 triple-input positive AND and negative OR gates with open collector outputs.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage (V_I ≥ 15V)
- High breakdown output voltage ($V_O \ge 7V$)
- Low power dissipation (P_d = 13mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

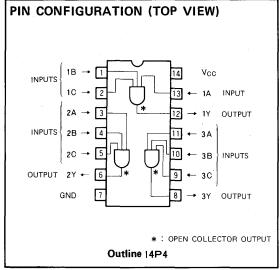
With the use of Schottky TTL Technology and open collector outputs with a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

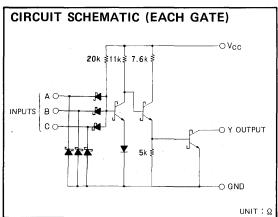
When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

Α	N	Y
L	L _i	L
Н	L	L
L	Ι	. L .
н	I	I

 $N = B \cdot C$





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter Parameter		tions	Limits	Unit
Vcc	Supply voltage			-0.5∼+7	V
VI	Input voltage			-0.5∼ + 15	V
Vo	Output voltage	High-level state		-0.5∼+7	V
Topr	Operating free-air ambient temperature range			- 20∼ + 75 ·	°C
Tstg	Storage temperature range			- 65~ + 150	°C

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Danamasa	Parameter		Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Гон	High-level output current	V _O =5.5V	0		100	. μΑ		
la.	Low-level output current	V ₀ L≦0.4V	0		4	mA		
I OL Low-level output current	V _{OL} ≦0.5V	0		8	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

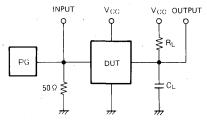
Combal	B	Ç	ditions	Limits			Unit
Symbol	Parameter	Conc	Conditions		Typ *	Max	Onit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
Гон	High-level output current	V _{CC} =4.75V, V _I =2	V, V ₀ =5.5V			100	μΑ
1/2.	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	٧
VoL	Low-rever output vortage	V ₁ =0.8V	IOL= 8mA		0.35	0.5	٧
l _{iH}	High-lèvel input current	V _{CC} =5.25V,V _I =2	2.7V			20	μА
чH	Trigriever input current	V _{CC} =5.25V,V _I =1	10V			0.1	mΑ
l _{IL}	Low-level input current	V _{CC} =5.25V,V ₁ =0).4V			0.4	mΑ
Ісен	Supply current, all outputs high	V _{CC} =5.25V,V ₁ =4	1.5V		1.8	3.6	mA
Iccl	Supply current, all outputs low	V _{CC} =5.25V,V₁=	0		3.3	6.6	mA

^{* :} All typical values are at $V_{CC} = 5 V$, $T_a = 25 ^{\circ}C$.

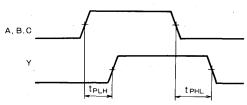
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter Test conditions			Limits		Unit
Symbol	i arameter	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level output propagation time	R _L =2KΩ		15	35	ns
t _{PHL}	High-to-low-level output propagation time	C _L =15pF (Note)		10	35	ns

Note: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_Q = 50Ω .
- (2) C_L includes probe and jig capacitance.



DUAL 4-INPUT NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS18P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates having a schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 22mW typical)
- High speed (t_{pd} = 24ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

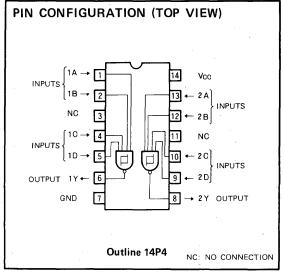
FUNCTIONAL DESCRIPTION

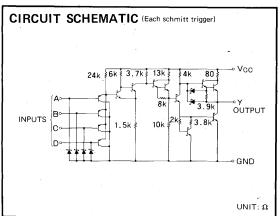
It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When A, B, C and D inputs are high, output Y is low, and when more than one is low. Y is high.

M74LS13P can be replaced with M74LS18P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.

For typical characteristics see M74LS19P.





FUNCTION TABLE

Α	N	Y
L	L	Н
н	L	Η
L	н	н
Н	Н	L

 $N = B \cdot C \cdot D$

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
· VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5 - V _{CC}	V
Topr	Operating free-air ambient temperature range '		-20~+75·	°C
Tstg	· Storage temperature range		-65~+150	°C

DUAL 4-INPUT NAND SCHMITT TRIGGER

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

	Parameter			Limits				
Symbol Parameter			Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА		
		V ₀ L≦0.4V	0		4	mA		
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 ^{\circ}C$, unless otherwise noted)

		-			Limits		
Symbol	Parameter	Test cond	litions	Min	Typ *	Max	Unit
V _T +	Positive-going threshold voltage	V _{CC} =5V		1.65	1.9	2.15	V
VT-	Negative-going threshold voltage	V _{CC} =5V		0.75	1.0	1.25	٧ .
VT+VT-	Hysteresis width	V _{CC} =5V		0.4	0.9		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
	High-level output voltage	V _{CC} =4.75V, V _I =0.5V		2.7	3,4		V
Voн	High-level output voltage	I _{OH} = 400 μA	400μA		3.4		V
.,		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output voltage	V _I =1.9V	I _{OL} = 8mA		0.35	0.5	V
I _{T+}	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			-2		μΑ
I _T	Input current at negative-going threshold	V _{CC} =5V, V _I =V _T -			-5		μΑ
	Lieb Is al in the second	V _{CC} =5.25V, V _I =2.7	'V			20	μΑ
ін	High-level input current	V _{CC} =5.25V, V _I =10\				0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _J =0.4	V			-0.05	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0\	,	- 20		-100	mΑ
Госн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			3.3	6	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5	V	1.	5.7	10	mA

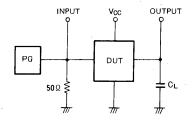
^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

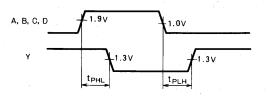
Symbol	Symbol Parameter	Test conditions		Limits		
Gymbo)	Taramete	rest conditions	Min	Typ	Max	Unit
tpLH	Low-to-high-level output propagation time	C _L =15pF (Note 2)		12	20	ns
t _{PHL}	High-to-low-level output propagation time	OL = 13pr (Note 2)		37	55	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, Vp = 3Vp.p, Z_0 = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM



HEX SCHMITT TRIGGER INVERTER

DESCRIPTION

The M74LS19P is a semiconductor integrated circuit containing 6 schmitt trigger inverter circuits.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage (V₁ ≥15V)
- Low power dissipation (P_d = 67mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

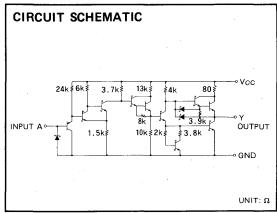
FUNCTIONAL DESCRIPTION

It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When input A is high, output Y is low, and when A is low, Y is high.

M74LS14P can be replaced with M74LS19P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.

PIN CONFIGURATION (TOP VIEW) 6A INPUT 6Y OUTPUT INPUT 3A → OUTPUT 3Y GND 4 Y OUTPUT **Outline 14P4**



FUNCTION TABLE

Α	Y
L	н
Ι	L

ABSOLUTE	MAXIMUM	RATINGS
$(Ta = -20 \sim +75)$	C. unless otherwise	noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	. v
Topr	Operating free-air ambient temperature range		-20~+75	,C
Tstg	Storage temperature range		-65~+150	Č

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75\%$, unless otherwise noted)

C	D	P		Limits			
Symbol	Parameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	· V	
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μA	
		V _{OL} ≤0.4V	0		4	.mA	
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

HEX SCHMITT TRIGGER INVERTER

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

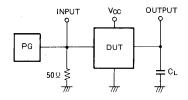
Cumbal	Parameter	T	41:11:22		Limits		Unit
Symbol	Faranieter	lest con	Test conditions			Max	Unit
V _{T+}	Positive-going threshold voltage	V _{CC} =5V		1.65	1.9	2.15	V
V _T -	Negative-going threshold voltage	V _{CC} =5V		0.75	1.0	1.25	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =5V	,	0.4	0.9		V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =0.	V _{CC} =4.75V, V _I =0.5V		3.4		V
VOH	riigiriievel output voitage	$I_{OH} = -400 \mu A$		2.7	3.4		
V-	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =1.9V	I _{OL} =8mA		0.35	0.5	٧
I _{T+}	Input current at positive-going threshold	V _{CC} =5V, V _I =V _{T+}			- 2		μΑ
I _T _	Input current at negative-going threshold	V _{CC} =5V, V _I =V _{T-}			-5		μΑ
t	High-level input current	V _{CC} =5.25V, V _I =2.	7 V			20	μА
hн	nigh-level input current	$V_{CC} = 5.25V$, $V_{I} = 10V$				0.1	mA .
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.05	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			9.9	18	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.	5V		17	30	mA

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, Ta = 25 °C, unless otherwise noted)

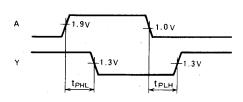
Symbol	Parameter	Test conditions		Limits		11-1-
	Tarameter		Min	Тур	Max	Unit
tpLH	Low-to-high-level output propagation time	0 -15-E (Nata 3)		11	20	ns
t _{PHL}	High-to-low-level output propagation time	C _L =15pF (Note 2)		15	30	ns

Note 2: Measurement circuit



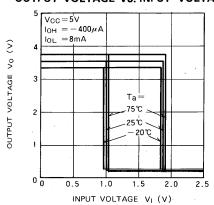
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM

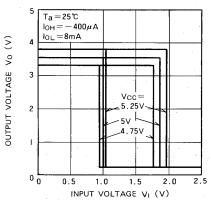


TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS. INPUT VOLTAGE



OUTPUT VOLTAGE VS. INPUT VOLTAGE



Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS20P is a semiconductor integrated circuit containing two 4-input positive NAND gates, usable as negative-logic NOR gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 4mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

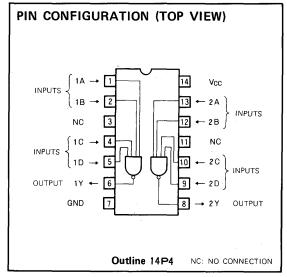
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

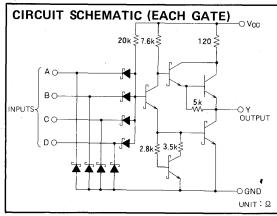
When inputs A, B and C are high, output Y is low, and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Υ,
L	L	Н
Н	L	Ħ
L	н	. н
н	Н	L

 $N = B \cdot C \cdot D$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı .	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

DUAL 4-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D	_		Limits		Limits		
Symbol	Parameter	•	Min Typ		Max	Unit		
Voc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
	Low-level output current	V ₀ ∟≦0.4V	0		4	mA		
loL		V _{OL} ≤0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

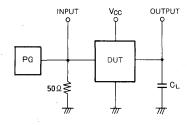
Symbol	D	Parameter Test conditions			Limits		Unit
Symbol	Parameter	rest condit	rest conditions		Тур*	Max	. Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} =4.75V, V _I =0.8	$V_{CC} = 4.75V, V_1 = 0.8V, I_{OH} = -400 \mu A$		3.4		V
.,	Lauriania autoria ariba	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High to all in	V _{CC} =5.25V, V _I =2.7	V			20	μA
Іін	High-level input current	V _{CC} =5.25V, V _I =10V			-	0.1	mA
ηL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		- 20		-100	mA
I _{CCH}	Supply current, all inputs high	V _{CC} =5.25V, V _I =0V			0.4	0.8	mA
I _{CCL}	Supply current, all inputs low	V _{CC} =5.25V, V _I =4.5	V		1.2	2.2	mA

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time,

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta = 25°C, unless otherwise noted)

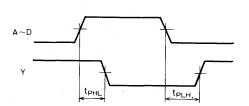
Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Farameter	rest conditions	Min	Тур	Max	Oint
t _{PLH}	Low-to-high-level/high-to-low-level	C _L =15pF		6	15	ns
tpHL	output propagation time	(Note 2)		13	15	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .

(2) C_L includes probe and jig capacitance.



M74LS21P

DUAL 4-INPUT POSITIVE AND GATE

DESCRIPTION

The M74LS21P is a semiconductor integrated circuit containing two 4-input positive AND and negative OR gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 8.5mW typical)
- High speed (tpd = 9ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

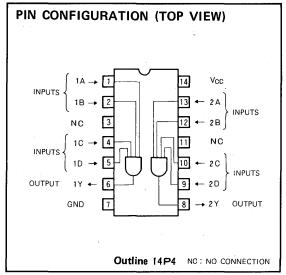
The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

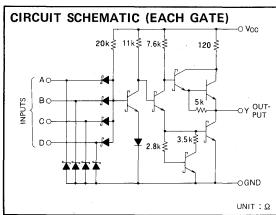
When inputs A, B, C and D are high, output Y is high, and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

. А	N	Υ
L	L	٦
н	L	L
L	н	L
н	Н	Н

 $N = B \cdot C \cdot D$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range	,	-20~+75	°C
Tstg	Storage temperature range		-65~ +150	℃

DUAL 4-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	•			Limits			
Symbol	raramet	Parameter Min Typ Max		- Unit			
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μА	
		V ₀ L≦0.4V	0		4	mA	
loL	Low-level output current	V ₀ L≦0.5V	. 0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

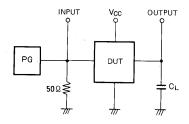
		Total conditions		Limits		
Symbol	Parameter	Test conditions	Min	Typ*	. Max	Unit
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			1.5	V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =2V, I _{OH} =-	400μA 2.7	3.4		٧
		V _{CC} =4.75V I _{OL} =4	4 mA	0.25	0.4	V
VoL	Low-level output voltage	V ₁ =0.8V	8 mA	0.35	0.5	V
		V _{CC} =5.25V, V _I =2.7V			20	μА
Iн	High-level input current	V _{CC} =5.25V, V _I =10V			0.1	mA
h.	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V ₀ =0V	-20		-100	mA
Госн	Supply current, all outputs high	V _{CC} =5.25V, V _I =4.5V		1.2	2.4	mΑ
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =0V		2.2	4.4	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

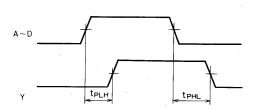
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	raidinetei		Min	Тур	Max	Unit
t _{PLH}	Low-to-high-output level propagation time	C _L =15pF		. 9	15	ns
t _{PHL}	High-to-low-output level propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_Q = 50Ω .
- (2) $\,$ CL includes probe and jig capacitance.



Note 1: All measurements must be done quickly and not more than one output should be shorted at a time,

DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS22P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage (V₁ ≥ 15V)
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (Pd = 4mW typical)
- High speed (tpd = 18ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

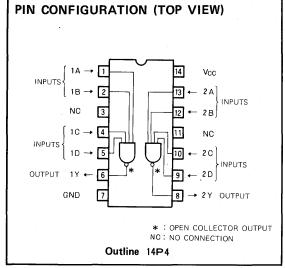
With the use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

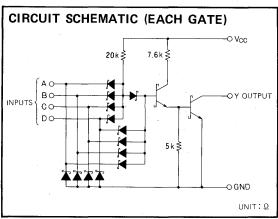
When inputs A, B, C and D are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Υ
· L	L	Н
Н	L	н
L	Н	Н
Н	I	L

 $N = B \cdot C \cdot D$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65 - +150	°C

DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING OCNDITIONS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

				Unit		
Symbol	Paramet	er	Min	Тур	Max 5.25 100 4	Oiiit
Voc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		100	μА
	Low-level output current $V_{0L} \le 0.4V$ $V_{0L} \le 0.5V$	V ₀ ∟≦0.4V	0		4	mA
JOL		V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

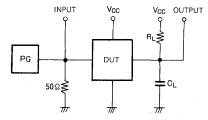
Symbol	Parameter	Ţ			Limits		1.1-14	
Symbol	rarameter	l est c	onditions	Min Ty		Max	Unit	
ViH	High-level input voltage			2			V	
VIL	Low-level input voltage					0.8	٧	
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	= — 18mA			-1.5	٧	
		V _{CC} =4.75V, V _I =	0.8V					
юн.	High-level output current	V ₀ =5.5V				100	μΑ	
	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V	
VoL	Low-level output voltage	V _I =2V	I _{OL} = 8mA		0.35	0.5	٧	
	High lovel in the second	V _{CC} =5.25V ₁ , V _I =	2.7V	*. *		20	μА	
ЧН	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mΑ	
lı_	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA	
Гссн	Supply current, all inputs high	V _{CC} =5.25V, V _I =	0V		.0.4	0.8	mA	
Iccl	Supply current, all inputs low	V _{CC} =5.25V, V _I =	4.5V	·	1.2	2.2	mA	

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

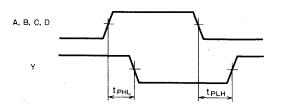
Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Symbol	rest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level/high-to-low-level	R _L = 2kΩ		10	3 2	ns
tpHL	output propagation time	C _L =15pF (Note 1)		25	28	ns

Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns; V_P = $3V_{P,P}$, Z_O = 50Ω

(2) C_L includes probe and jig capacitance.



QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS24P is a semiconductor integrated circuit containing four 2-input positive-logic NAND gates having a schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage $(V_1 \ge 15V)$
- Low power dissipation (Pd = 44mW typical)
- High speed (tpd = 18ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

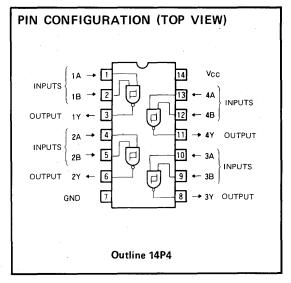
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When A and B inputs are high, output Y is low, and when more than one is low, output Y is high.

M74LS132P can be replaced with M74LS24P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level

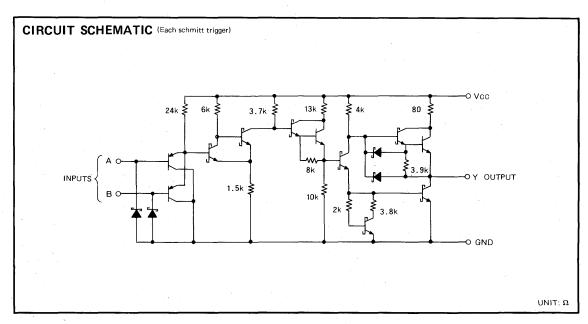


of the threshold voltage setting, low level noise margin can be improved.

For typical characteristics see M74LS19P.

FUNCTION TABLE

Α .	В	Y
L	٦	Н
н	L	Н
L	н	н
Н	Η,	L



QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	÷c
Tstg	Storage temperature range		-65~+150	°

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

				Unit		
Symbol	Parame	eter	Min	Тур	Max 5.25 - 400	Omit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μΑ
La	Low-level output current	V _{OL} ≦0.4V	0		4	mA
IOL	cow-level output current	V _{OL} ≤0.5V	0		8	mΑ

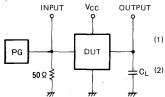
ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Complete		T	Test conditions Limits				Unit
Symbol	Parameter	l est con	aitions	Min	Тур *	Max	Unit
VT+	Positive-going threshold voltage	V _{CC} =5V	1.65	1.9	2.15	V	
V _T –	Negative-going threshold voltage	V _{CC} =5V		0.75	1.0	1.25	V
VT + VT -	Hysteresis width	V _{CC} =5V		0.4	0.9		V .
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} = - 18mA				-1.5	V
VoH	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.5V$ $I_{OH}=-400\mu A$		2.7	3.4		٧
	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I = 1.9V	I _{OL} =8mA		0.35	0.5	V
IT+	Input current at positive-going threshold	$V_{CC}=5V$, $V_{I}=V_{T+}$			·-2		μΑ
I _T =	Input current at negative-going threshold	$V_{CC}=5V$, $V_I=V_{T-}$			-5		μΑ
		V _{CC} = 5.25V V _I = 2.7V				20	μΑ
IIH	High-level input current	V _{CC} '= 5.25V V _I = 10V				0.1	mA
lıL.	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.05	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _C =0V		-20		— 100	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			6.6	12	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.	.5V		11	20	mA

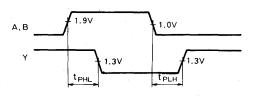
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions Limits			1.1-14	
	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time	C _L = 15pF (Note 2)		13	20	ns
t _{PHL}	High-to-low-level output propagation time			24	40	ns.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6$ ns, $t_f =$ 6ns, $t_W \approx 500$ ns, $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$ C_L (2) C_L includes probe and jig capacitance.



TIMING DIAGRAM

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74LS27P is a semiconductor integrated circuit containing three triple-input positive NOR and negative NAND gates.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (P_d = 13.5mW typical)
- High speed (tpd = 6ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

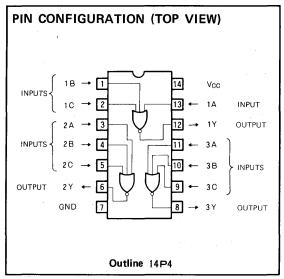
The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

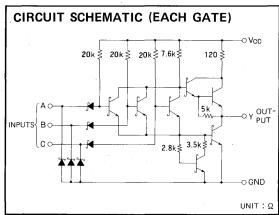
When one or more of the A, B and C inputs are high, output Y is low and when all inputs are low, Y is high.

FUNCTION TABLE

Α	N	Υ
. L	L	Н
Н	L	L
L	Н	L
Н	Н	L

$$N = B + C$$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit	
V _{CC}	Supply voltage		-0.5~+7	V	
VI	Input voltage		-0.5~+15	V	
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		−65 ~ + 150	°C	

TRIPLE 3-INPUT POSITIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol			Limits			Unit	
	Paramet	er	Min	Тур	Max	Onit	
Voc	Supply voltage		4.75	5	5.25	V	
lон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
loL		V _{OL} ≤0.4V	0		4	mA	
	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

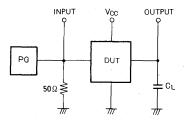
Symbol	P-veneto-	Test conditions			Limits		Unit
	Parameter			Min	Typ*	Max	
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC}	= - 18mA			-1.5	· V
Voн	High-level output voltage	$V_{CC} = 4.75V, V_{I} = 0.8V, I_{OH} = -400\mu A$		2.7	3.4		. V
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧
Vol		V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High level in the second	V _{CC} =5.25V, V _I =	2.7V			20	μА
. ИН	High-level input current	V _{CC} =5.25V, V _I =10V			0.1	mA	
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V		*		-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		- 20	-	-100	mA
I _{CCH}	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			2	4	mA
IccL	Supply current, all outputs low	V _{CC} =5,25V, V _I =4,5V			3.4	6.8	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

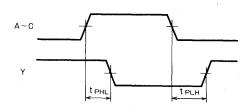
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
	. Talametel		Min	Тур	Max	Offic
t _{PLH}	Low-to-high-level output propagation time	C _L =15pF		6	15	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		6	15.	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) CL includes probe and jig capacitance.



Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

MITSUBISHI LSTTLS M74LS30P

SINGLE 8-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS30P is a semiconductor integrated circuit containing one 8-input positive-logic NAND gate, usable as a negative-logic NOR gate.

FEATURES

- High breakdown input voltage ($V_1 \ge 15V$)
- Low power dissipation (P_d = 2.4mW typical)
- High speed (tpd = 11ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

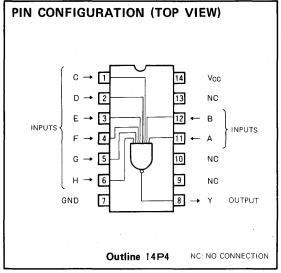
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

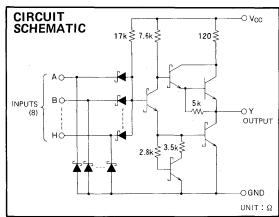
When inputs A, B, C, D, E, F and G are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

A	Z	Υ
L	٦	Η
Н	L	н
L	н	H
Н	Н	L

 $N = B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+V _{CC}	· V
Topr	Operating free-air ambinet temperature range		−20~ +75	°C
Tstg	Storage temperature range		-65~+150	°C

SINGLE 8-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА	
loL	Low-level output current	V _O L≦0.4V	0		4	mA	
		V ₀ L≦0.5V	0	-	8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

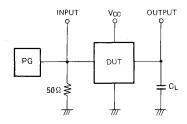
		-			Limits		
Symbol	Parameter	Test condi	itions	Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =0.	$V_{CC}=4.75V$, $V_1=0.8V$, $I_{OH}=-400\mu A$		3.4		V
.,	Low-level output voltage	V _{OC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High level input everes	V _{CC} =5.25V, V _I =2.	7V			20	μА
Ιιн	High-level input current	$V_{CC} = 5.25V, V_{I} = 10^{\circ}$	V			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4	4V			-0.4	mΑ
los	Short-circuit output circuit (Note 1)	V _{CC} =5.25V, V _O =0V	V	- 20		- 100	mA
Icch	Supply current, all inputs high	V _{CC} =5.25V, V _I =0\	,		0.35	0.5	mA
ICCL	Supply current, all inputs low	V _{CC} =5.25V, V _I =4.	5V		0.6	1.1	mA

^{* :} All typical values are at V_{CC}=5V, T_a=25°C Note 1: All measurements should be done quickly.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta = 25°C, unless otherwise noted)

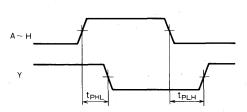
Symbol	Parameter	Test conditions		Limits		Unit
Symbol	i aranieter	rest conditions	Min	Тур	Max	Oint .
t _{PLH}	Low-to-high-level/high-to-low-level	C _L =15pF		6	15	ns
t _{PHL}	output propagation time	(Note 2)		16	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characterisites: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns; V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



PRECAUTION FOR USE

Connect pins not being used to the V_{CC} supply voltage.

M74LS32P

QUADRUPLE 2-INPUT POSITIVE OR GATES

DESCRIPTION

The M74LS32P is a semiconductor integrated circuit containing 4 dual-input positive OR and negative AND gates.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (Pd = 20mW typical)
- High speed (tpd = 7ns typical)
- · Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

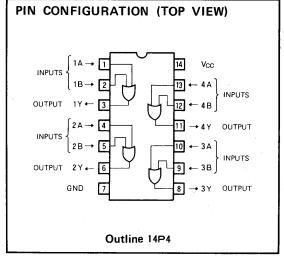
FUNCTIONAL DESCRIPTION

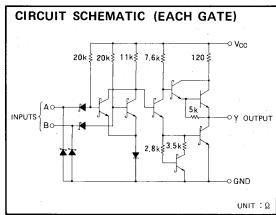
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When either or both of the inputs A and B is/are high, output Y is high, and when both A and B are low, Y is low.

FUNCTION TABLE

Α	В	Y
L	Г	L
н	L	н
L	Н	Н
r	I	H





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5∼+7	V
Vı	Input voltage		-0.5~+15	-V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	. °C
Tstg	Storage temperature range		−65~ ±150	°C

QUADRUPLE 2-INPUT POSITIVE OR GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			11-7-		
Symbol			Min	Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	Ō		4	mA
lor		V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

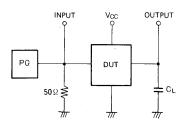
0	2	T Pri		Limits			
Symbol	Parameter	Test cond	itions	Min	Тур*	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					8.0	V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	18mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V$, $V_{I} = 2V$ $I_{OH} = -400\mu A$		2.7	3.4		٧
		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =0.8V	I _{OL} =8mA		0.35	0.5	٧
	High level in the second	V _{CC} =5.25V, V _I =2.7	V			20	μА
Іін	High-level input current	V _{CC} =5.25V . V _I =10V				0.1	mA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mΑ
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		20		- 100	mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =4.5V			3.1	6.2	mA
I _{CCL}	Supply current, all outputs low	V _{CC} =5.25V, V _I =0V			4.9	9.8	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C. Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

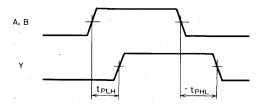
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol Parameter	Test conditions		Limits			
Symbol	raiametei	rest conditions		Тур	Max	Unit
tpLH	Low-to-high-level output propagation time	0 15-5 40 0		7	22	ns
tpHL	High-to-low-level output propagation time	C _L =15pF (Note 2)		. 7	22	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characterstics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P-P}, Z_0 \approx 50\Omega$
- (2) C_L includes probe and jig capacitance.



QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

DESCRIPTION

The M74LS37P is a semiconductor integrated circuit containing four 2-input positive NAND and negative NOR buffer gates.

FEATURES

- High fan-out ($I_{OL} = 24mA$, $I_{OH} = -1.2mA$)
- High breakdown input voltabe $(V_l \ge 15V)$
- Low power dissipation (P_d = 17.5mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

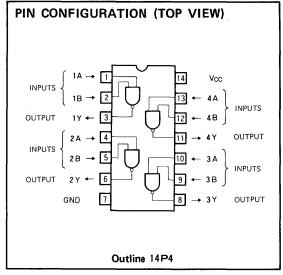
FUNCTIONAL DESCRIPTION

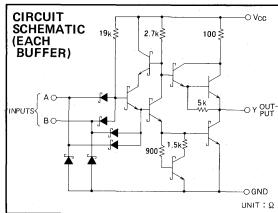
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When inputs A and B are high, output Y is low, and when one or both inputs are low, Y is high.

FUNCTION TABLE

В	Υ
L	Η
L	Η
н	Ħ
I	L
	L L





MAXIMUM ABSOLUTE RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V.
Vı	Input voltage		-0.5~+15	. v
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

			Limits Min Typ			Unit	
Symbol	Paran	neter			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≥2.7V	0		-1.2	mA	
	IoL Low-level output current	V ₀ L≦0.4	V ₀ L≦0.4V	0		12	mA
IOL		V _{OL} ≤ 0.5 V	0		24	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

			A		Limits		Unit
Symbol	Parameter	les	t conditions	Min	Typ *	Max	Onit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC}	= - 18mA			-1.5	V
Voн	High-level output voltage	$V_{CC} = 4.75V$, $V_1 = 0.8V$, $I_{OH} = -1.2 \text{mA}$		2.7	3.4		٧
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	$I_{OL} = 24 \text{mA}$		0.35	0.5	٧
	High local income	V _{CC} =5.25V, V _I =	2.7V	1.		20	μΑ
Ιιн	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
l _I L	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mΑ
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		- 30		-130	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V		-	0.9	2	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	= 4.5V	4.5	6	12	mA

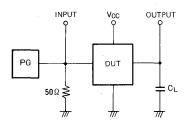
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

Note 1: All measurement should be done quickly, and not more than one output should be shorted at a time.

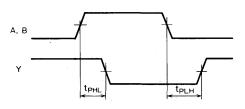
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	raianetei	rest conditions	Min	Тур	Max	Oint
t _{PLH}	Low-to-high-level output propagation time	C _L =45pF		7	24	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		12	24	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) CL includes probe and jig capacitance.



M74LS38P

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS38P is a semiconductor integrated circuit containing four 2-input positive NAND and negative NOR buffer gates with open collector outputs.

FEATURES

- Usable in wire-AND connection
- High fan-out (I_{OL} = 24mA max)
- High breakdown input voltage ($V_I \ge 15V$)
- High breakdown output voltage $(V_O \ge 7V)$
- Low power dissipation (P_d = 17.5mW typical)
- High speed (tpd = 14ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

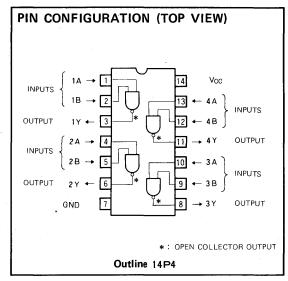
General purpose, for use in industrial and consumer equipment.

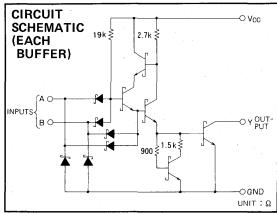
FUNCTIONAL DESCRIPTION

With the use of open collector outputs and SBD inputs having a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection, which has been impossible with conventional gates. The maximum low-level output current (I_{OL}) of 24mA makes this device suitable as a buffer gate. When inputs A and B are high, output Y is low and when one or both inputs are low, Y is high.

FUNCTION TABLE

A	В	Υ
L	L	Н
Н	L	Н
L	I	Н
н	Ι	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5-+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits				
Symbol	Parame	ter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V ₀ =5.5V	0		250·	μА		
		V _{OL} ≦0.4V	0		12	mA		
loL Low-level output current	Low-level output current V ₀ L≤0.5V	0		24	mΑ			

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

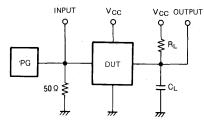
Complete	Parameter	Tost	Test conditions		Limits		
Symbol	rarameter	lest	conditions	Min	Тур. *	Max	Unit
ViH	High-level input voltage			- 2			V
VIL	Low-level input voltage					0.8	/ V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			1.5	V
Іон	High-level output current	V _{CC} =4.75V, V _I =	$V_{CC}=4.75V, V_1=0.8V, V_0=5.5V$			250	μΑ
.,	Law law all autout voltage	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =24mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =	2.7V			20	μА
lтн	High-level input current	V _{CC} =5.25V, V _I =	10 V			0.1	mA
lլ <u>լ</u>	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
Іссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	0V		0.9	2	mA
IccL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	Open		6	12	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

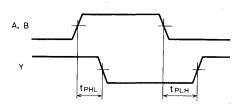
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Max Unit 32 ns 28 ns
Symbol	i didilietei	rest conditions	Min	Тур	Max	Oilit
t _{PLH}	Low-to-high-level output propagation time	R _L =667Ω		13	32	ns
t _{PHL}	High-to-low-level output propagation time	C _L =45pF (Note 1)		14	28	ns .

Note 1: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.



DUAL 4-INPUT POSITIVE NAND BUFFER

DESCRIPTION

The M74LS40P is a semiconductor integrated circuit containing 2 built-in quadruple-input positive NAND and negative NOR buffer gates.

FEATURES

- High fan-out (I_{OL} = 24mA, I_{OH} = −1.2mA)
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d =9mW typical)
- High speed (t_{pd} = 14ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

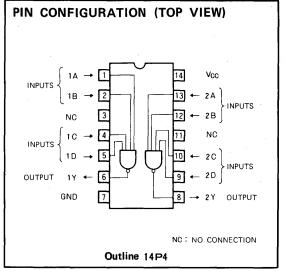
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

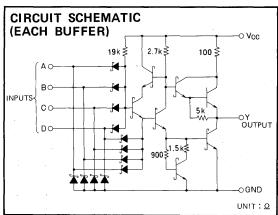
When all inputs A, B, C and D are high, output Y is low and when one or more of the inputs is low, Y is high.

FUNCTION TABLE

Α	Ν	Υ
L	L	н
н	L	H
L	н	Н
Н	Н	L

 $N = B \cdot C \cdot D$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted·)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		65-+150	°C

DUAL 4-INPUT POSITIVE NAND BUFFER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D		Limits		1	
	Para	meter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		-1.2	mA
		V _{OL} ≤0.4V	0		12	mA
OL Low-level output current	V _{OL} ≤0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	_			Limits		Unit
Symboli	Parameter Test conditions		conditions	Min	Тур*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	= — 18mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V, V_1 = 0.8V, I_{OH} = -1.2mA$		2.7	3.4		٧
		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	. V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =24 mA		0.35	0.5	V
1		V _{CC} =5.25V, V _I =	2.7V			20	μΑ
Ін	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V ₀ =0V		- 30		- 130	. mA
Icch	Supply current, all outputs high	V _{CC} =5.25V, V _I =	=0V	7	0.45	1	mA
ICCL	Supply current, all outputs low	V _{CC} =5.25V, V _I =	- Open		3	6	mA

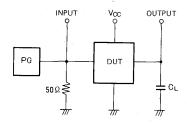
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

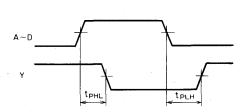
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
	r al arrieter	l.	Min	Тур	Max	Oilit
t _{PLH}	Low-to-high-level output propagation time	C _L =45pF		7	24	ns
t _{PHL}	High-to-low-level output propagation time	(Note 2)		20	24	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics:
 - \cdot PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
 - $V_P = 3V_{P.P}, Z_O = 50\Omega.$
- (2) C_L includes probe and jig capacitance.



MT4LS42P

BCD-TO-DECIMAL DECODER

DESCRIPTION

The M74LS42P is a semiconductor integrated circuit provided with a BCD-to-decimal decoder function.

FEATURES

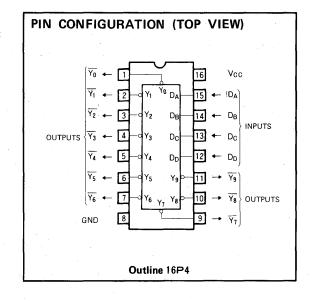
- All outputs set high with reactive input
- Usable as a 3-bit binary/octal decoder
- Wide operating temperature range (T_a=-20~+75°C)

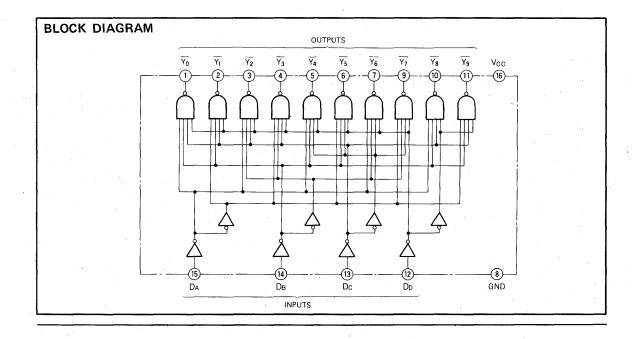
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When inputs D_A , D_B , D_C and D_D are specified in BCD code, the output corresponding to the number among $\overline{Y_0} \sim \overline{Y_9}$ is set low and all the other 9 outputs are set high. When a binary number of 10 or more is applied to $D_A \sim D_D$, all the outputs are set high.





BCD-TO-DECIMAL DECODER

FUNCTION TABLE

Decimal number	D _D	Dc	D _B	DA	₹ ₀	Ϋ́I	Y ₂	<u> 7</u> 3	<u>Y</u> 4	Y ₅	₹6	Ÿ7	<u>∀</u> 8	Y ₉
0	L	L	L	L	Ł	н	н	н	Н	Н	Н	Н	Н	Н
1	L	L	L	н	Н	L	н	Н	н	Н	н	Н	- н	H
2	. L	L	Н	L	н	H	L	Н	н	н.	Н	н	н	н
3	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	H	Н	Н
4	L	Н	L	L	н	н	н	н	L	Н	Н	H	н	Н
5	L	Н	L	Н	н	н	Н	н	Ĥ	L	Н	Н	Н	н
6	L	н	Н	L	Н	н	н	Н	н	H	L	н	. Н	Н
7	L	н	н	Π	н	Η	Н	Н	Н	Н	н	. L	н	н
8	Н	L	L	L	н	н	н	н	Н	' н	н	Н	L	н
9	I	L	٦	н	Ι	Н	Н	н	Н	н	н	н	н	L
10	н .	L	н	.L	н	н	Н	Н	н	н	Н	Н	н	Н
11	I	L	н	. н	н	н	н	н	Н	н	н	н	н	Н
12	н	Н	L	· L	н	Н	Н	н	н	н	н	н	Ĥ	Н
13	Ι	Ι	١	н	н	Ι	Н	Н	Н	Н	Н	н	н	н
14	I	н	I	L	H	н	н	н	Н	Н	н	н	н	Н
15	н	Н	Н	H [:]	Н	н	Н	н	Н	Н	Н	н	н	н

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20∼ +75	°C
Tstg	Storage temperature range	,	−65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75 \, \text{°C}$, unless otherwise noted)

C				Limits					
Symbol	Parame	eter	Min	Тур	Max	Unit			
Vcc	Supply voltage		4.75	5	5.25	٧			
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА			
		V _{OL} ≦0.4V	0		4	mA			
lor ·	Low-level output current	V _{OL} ≤0.5∨	0		8	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Cumbal	Parameter	Total condition					
Symbol	Parameter	Test condit	ions	Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC} = 4.75 \text{ V}, V_1 = 0.8 \text{ V}$ $V_1 = 2 \text{ V}, I_{OH} = -400 \mu \text{A}$		3.4		v
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
▼ 0L	Low level output voltage	$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} =8mA		0.35	0.5	٧
	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μА
ін,	High-level input current	V _{CC} =5.25V, V ₁ =10\	1			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mΑ
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _C =0	/	- 20		-100	mA
Icc	Supply current	V _{CC} =5.25V (Note 2)			7	13	mA

 $[\]boldsymbol{*}$: All typical values are at $V_{CC} = 5\,\text{V}$, $T_{a} = 25^{\circ}\text{C}$

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 2: I_{CC} is measured with all inputs at 0V.

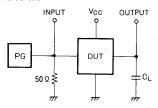


BCD-TO-DECIMAL DECODER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

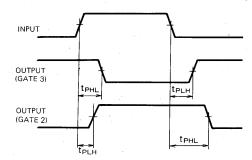
Symbol	Parameter	Test conditions		Limits	nits	
Symbol	Farameter	Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output			8	.25	ns
tphL	propagation time, gate 2	C _L =15pF (Note 3)		14	25	ns
tpLH	Low-to-high-level, high-to-low-level output	OL-15pr (Note 3)		12	30	ns
t _{PHL}	propagation time, gate 3			12	30	ns

Note 3: Measurement circuit



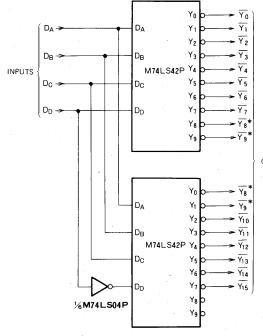
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_O =50 Ω
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



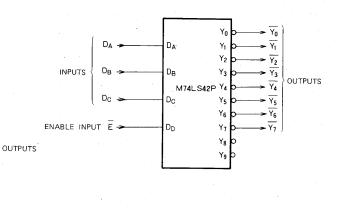
APPLICATION EXAMPLES

(1) 4-bit binary/hexadecimal decoder



Outputs marked with * are provided from both decoders.

(2) 3-bit binary/octal decoder with enable input



DESCRIPTION

The M74LS47P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function and open collector outputs.

FEATURES

- Suitable for 7-segment display element lighting
- RBI input and BI/RBO outputs for zero suppression
- LT input for lamp testing
- BI/RBO input for extinguishing all segments
- Open collector outputs
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

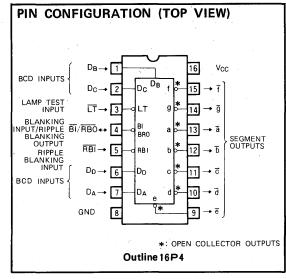
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a number is designed in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment outputs $\overline{a} \sim \overline{g}$ are set low in accordance with that number. By connecting the 7-segment display element to each of the outputs, the character indicated on the display character can be displayed. $\overline{a} \sim \overline{g}$ are open collector outputs with a breakdown voltage of not less than 15V and a low-level output current of 24mA, thereby making it possible to directly drive a 7-segment LED for the display of anode-common numbers.

Suppression of the high-order unnecessary zeroes is possible by setting the highest order \overline{RBI} ripple blanking input low and connecting ripple blanking output $\overline{BI}/\overline{RBO}$ to the next-order \overline{RBI} for each of the digits. (Refer to the application example.)

By setting blanking input $\overline{BI}/\overline{RBO}$ low, outputs $\overline{a}\sim\overline{g}$ are set high and the display element is extinguished irrespective

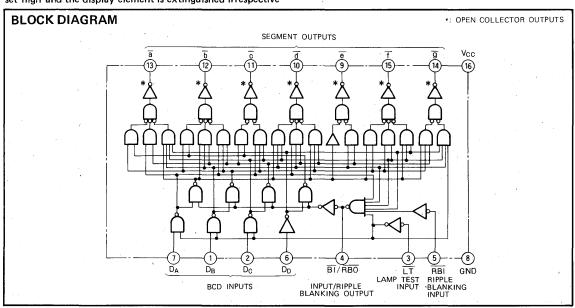


of the status of the other inputs. The luminous intensity can be controlled by applying pulses.

Since BI/RBO serves as both an input and output pin, only ICs with open collector outputs can be connected to this pin.

By setting lamp test input \overline{LT} low, $\overline{a} \sim \overline{g}$ are set low irrespective of the status of $\overline{BI}/\overline{RBO}$, D_A , D_B , D_C and D_D , all the segments in the display element are lighted and each segment can be tested.

Except for that pins 6 and 9 differ in character from the M74LS47P has exactly the same functions, pin connections and characteristics as the M75LS247P.



FUNCTION TABLE (Note 1)

Decimal number or function	LT	RBI	D _D	Dc	DB	DA	BI/	RBO	a	b	c	d	e	f	g	Note
0	Н	Н	L	L	L	L		Η	L	L	L	L	L	L	Н	
. 1	Н	×	L	L	Ĺ	Н		Н	Н	L	L	Η	Н	н	н	
2	Н	x	L	L	Н	L		Н	L	L	Н	L	L	H	L	
3	Н	x	L	L	н	H		Н	L	L	L	L	н	н	L	
4	Н	Х	L	Н	L	L		Н	Н	L	L	Н	Н.	L	. L	
5	Н	X	L	н	L	Н		Н	L	H	L	L	Н	L	L	
6	Н	х	L	Н	Н	L	, .	Н	Н	Н	L	L	L	L	L	
7	Н	Х	L	Н	н	Н		H	L	L	L	Н	Н	н	н	(1)
8	Н	Х	Н	L	L	L		H	L	L	L	L	L	L	L]. '''
9 .	H	X	н	L	L	Н		Н	L	· Ľ	L	Н	Н	٦	L	
10	Н	, x	Н	L	Н	L		Н	Н	н	н	L	L	Н	.L	
. 11	Н	Х	Н	L	н	Н		Н	Н	Н	L	L.	Н	Н	L	
12	Н	Х	Н	Н	L	L		Н	н	L	н	Н	Н	L	L	
13	Н	Х	Н	Н	L	Н		Н	L	Н	н	L	н	L	L	
14	Н	Х	Н	н	ıН	L		Н	Н	Н	н	L	L	Ľ	L	
15	Н	Х	Н	Н	Н	Н		Н	Н	Н	Н	Н	Н	Н	н	
Blanking	- X	X	Χ,	Х	Х	х	L		Н	Н	н	Н	Н	Н	н	(2)
Ripple blanking	Н	L	L	L	L	Ļ		. L	H	н	Н	Н	Ĥ	Н	н	(3)
Lamp test	L	Х	X	Х	х	х		Н	L	L	Ŀ	L	L	L	L	(4)

Note 1. (1) \overline{LT} is normally kept in high

RBI is kept open or in high with a decimal 0 output.

- (2) When BI/RBO is low, all the segment outputs are high irrespective of the status of the other inputs.
- (3) All the segment outputs are set high and $\overline{BI}/\overline{RBO}$ is set low when \overline{LT} is high and \overline{RBI} , D_A , D_B , D_C and D_D are low.
- (4) When LT is low, all the segment outputs are low.
- X: Irrelevant





CHARACTERS DISPLAYED

Decimal number	0	1	2	3	. 4	5	6	7	8	9	10	1.1	12	13	14	.15
Character	CO	.	ñυ	3	Ľ	5	.0	7	8	O'	ū	⊃	C	ıП	는	

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C , unless otherwise noted)

Symbol		Parameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vı	Input voltage	Input BI/RBO		-0.5~V∞	· V
VI	Input vortage	Other inputs		-0.5~+15	V
1/6	Output voltage	Output BI/RBO	Liber Lavel Asset	-0.5~ V _{CC}	V
•0	V ₀ Output voltage	Other outputs	High-level state	-0.5~+15	V
l _{O(peak)}	Output current		tw≤1ms, dutycycle≤10%	200	mA
10	Output current		High-level state	1	mA
Topr	Operating free-air amb	ient temperature range		-20~+75	°C
Tstg	Storage temperature ra	ange		−65~+150	°C

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		Parameter			Limits					
Symbol	Parame	ter	Min	Тур	Max	Unit				
Vcc	Supply voltage		4.75	5	5.25	V				
Юн	High-level output current, outputs ā ~ 引	V _{OH} = 15 V	, 0		250	μА				
Юн	High-level output current, output BI/RBO	V _{OH} ≧2.4V	0		50	μА				
	Low-level output current,	V _{OL} ≤0.4V	0		12	mA				
lor	outputs $\overline{a} \sim \overline{g}$	V _{OL} ≦0.5V	0		24	mA				
	Low-level output current,	V _O L≦0.4V	0		1.6	mA				
lor.	output BI/RBO	VoL≦0.5V	0		3.2	mΑ				

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

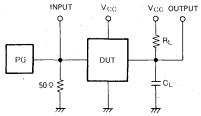
Symbol	Parameter		Test cond	itions		Limits		Unit
Зунион	raiametei	·	rest condi	itions .	Min	Typ *	Max	Ont
Viн	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage	-	V _{CC} =4.75V, I _{IC} =-1	18 m A			— 1.5	. V
VoH	High-level output voltage, output B I	/RBO	V _{CC} =4.75V	$I_{OH} = -50\mu A$	2.4	4.2		V
Юн	High-level output current, outputs a	~ g	$V_1 = 0.8 V, V_1 = 2 V$	V _O = 15 V			250	μА
		o = =		I _{OL} = 12 mA		0.25	0.4	
.,	Low-level output voltage	Outputs $\overline{a} - \overline{g}$	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.8 -1.5	
Vol	1 ' '	Outputs BI/RBO	$V_1 = 0.8 \text{V}, \ V_1 = 2 \text{V}$	I _{OL} = 1.6mA	1	0.25	0.4	V
	- , , , , , , , ,	Outputs B1/ NBO	•	I _{OL} =3.2mA		0.35	0.8 -1.5 250 0.4 0.5 0.4 0.5 20 0.1 -1.2 -0.4	
	Link level in put voltage event in put	DI / DDO	V _{CC} =5.25V, V _I =2.7	v			20	μА
he ,	High-level input voltage, except input	BI/NBO	V _{CC} =5.25V, V _I =10V				0.1	mA
	Low lovel in part any and	Input BI/RBO		.,			- 1.2	mA
h_	Low-level input current	Other inputs	$V_{CC} = 5.25 \text{V}, V_I = 0.4$	V			-0.4	mA
los	Short-circuit output current, output	BI/RBO	V _{CC} =5.25V, V _O =0V		-0.3		-2	mA
. lcc	Supply current		V _{CC} =5.25V (Note 2)			7	13	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

SWITCHING CHARACTERISTICS ($Ta = -20 \sim +.75$ °C, unless otherwise noted)

Symbol	Parameter	Test condition	nns		Limits		Unit
Symbol	i di diffetei	rest condition		Min	Тур	Max	Offic
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	D -0050			35	100	ns
t _{PHL}	time, from input D_A to outputs $\overline{a} \sim \overline{g}$	R _L =665Ω			30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	$C_L = 15 pF$	Γ		50	100	ns
t _{PHL}	time, from input RBI to outputs a ~ f	(Note 3)			45	100	ns

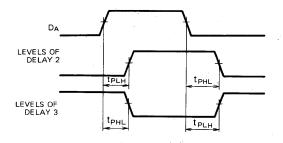
Note 3: Measurement circuit

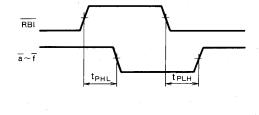


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

Note 2: I_{CC} is measured with all inputs at 4.5V.

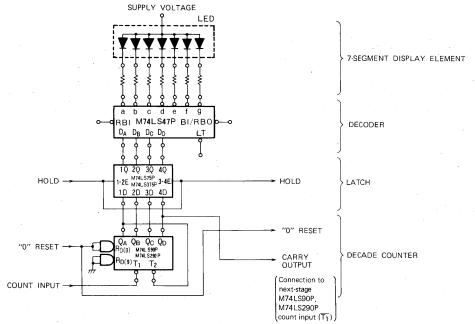
TIMING DIAGRAM (Reference level = 1.3V)



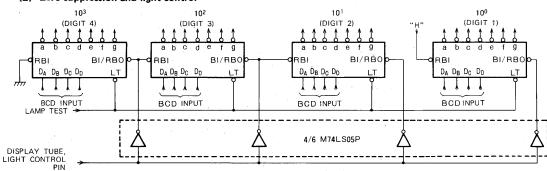


APPLICATION EXAMPLES

(1) Counter using M74LS47P



(2) Zero suppression and light control



DESCRIPTION

The M74LS48P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function.

FEATURES

- Suitable for 7-segment display element lighting
- RBI input and BI/RBO output for zero suppression
- LT input for lamp testing
- BI/RBO input for extinguishing all segments
- NPN transistor can be externally mounted for Highcurrent drive.
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device resembles the M74LS47P without the output transistors and when a number is specified in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment outputs a~g are set high in accordance with that number. Outputs a~g contain 2Ω pull-up resistors which are suitable for driving common-cathode LEDs. By connecting an NPN transistor to these outputs, it is possible to drive high current display elements.

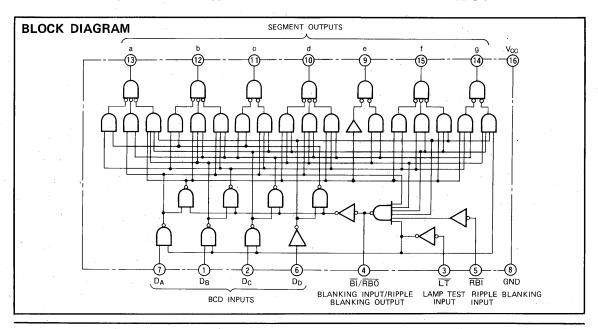
The ripple blanking, blanking and lamp test functions are the same as those for the M74LS47P.

Refer to the M74LS47P for the application example.

Except for that pins 6 and 9 differ in character form the M74LS48P has exactly the same functions, pin connections

PIN CONFIGURATION (TOP VIEW) Vec BCD INPUTS Dc LAMP TEST INPUT 14 BLANKING INPUT/RIPPLE BI/RBO↔ SEGMENT OUTPUTS RIPPLE RBI-BLANKING INPUT $D_D \rightarrow$ Dn 1.1 BCD INPUTS 10 GND Outline 16P4

and characteristics as the M74LS248P.



FUNCTION TABLE (Note 1)

Decimal number or function	LT	RBI	DD	Dc	DB	DA	BI/F	₹ <u>B</u> 0	а	b	С	d	е	f	g	Note
0	Н	Н	L	L	L	L		Н	Н	Н	Н	H	Н	Н	L	
1	Н	Х	L	L	L	Н		Н	L	Н	Н	L	L	L	L	1
2	Н	Х	L	L	Н	L		Н	Н	Н	L	Н	н	L	н]
3	Н	Х	L	L	Н	Н		Н	н	Н	Н	Н	L	L	Н	
4	Н	Х	L	Н	L	L		Н	L	Н	Н	L	·L	Н	Н]
5	Н	X	L	Н	L	Н		Н	Н	L	Н	Н	L	Н	Н	1
6	Н	X	L	Н	Н	L		Н	L	L	Н	Н	Н	Н	Н	1
7	Н	X	L	Н	Н	Н		Н	Н	Н	Н	L	L	L	L	1
8	Н	Х	Н	L	L	L		Н	Н	н.	Н	Н	Н	Н	Н	(1)
9	н	Х	H	L	L	Н		Н	н	Н	Н	L	L	Н	н	1 .
10	Н	X	Н	∟	H	L		Н	L	L	L	Н	Н	L	Н	1
11	н	Х	Н	L	Н	н	-	Н	L	L	н	Н	L	L	Н]
12	Η,	X	Н	Н	L	L		Н	L	Н	L	Ļ	L	Н	Н	1
. 13	Н	Х	Н	Н	. L	Н		Н	Н	L	L	Н	L	Н	Н	1
14	Н	Х	Н	Н	Н	L		Н	L	L	L	н	Н	Н	Н	1
15	Н	Х	H	Н	Н	Н		Н	L	L	L	. L	L	L	L	1
Blanking	X	Х	Х	X	X	Х	L		L	L	L	L	L	L	L	(2)
Ripple blanking	Н	L	L	L	L	L		Ľ	L	L	L	L	L	L	L	(3)
Lamp test	L	Х	Х	Х	X	Х		Н	н	н	Н	Н	Н	Н	н.	(4)

Note 1. (1) LT is normally kept in high.

DEFINITION OF SEGMENTS

- RBI is kept open or in high with a decimal 0 output.
- (2) When \$\overline{BI}\rightarrow{RBO}\$ is low, all the segment outputs are low irrespective of the status of the other inputs.
- (3) All the segment outputs are set high and BI/RBO is set low when LT is high and RBI, DA, DB, DC and DD are low.
- (4) When LT is low, all the segment outputs are high.
- X: Irrelevant



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	- 11	12	13	14	15
Character		1	ñ	3	Ę	5	О	7	8	<u>.</u>	u	J	U	_	ηT	

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Paran	neter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	٧
i.	Input voltage	Input BI/RB0		-0.5~V _{CC}	V
Vı	input voltage	Other inputs		-0.5~+15	V
	Output voltage	Output BI/RBO	High-level state	-0.5~V _{CC}	V
V ₀	Output voltage	Other outputs	nigh-level state	-0.5~Vcc	V
Topr	Operating free-air ambient	temperature range		-20~+75	°C
Tstg	Storage temperature range			−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

C b - 1			Unit			
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current, outputs a - q	V _{OH} ≧2.4V	. 0		- 100	μА
Іон	High-level output current, output BI/RBO	V _{OH} ≥2.4V	0		50	μА
1	Low-level output current,	V ₀ L≦0.4V	0	,	2	mA
loL	outputs a ~ g	V _{0L} ≤0.5V	0		6	. mA
1	Low-level output current,	V _{OL} ≤0.4V	0		1.6	mA
loL	output BI/RBO	V _{OL} ≤0.5V	0		3.2	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +70^{\circ}C$, unless otherwise noted)

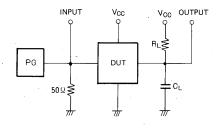
			T- 4 1			Limits		Unit
Symbol	Paramete	r .	Test condi	tions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	· V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	.V
	High-level output voltage	Outputs a ~ g	V _{CC} =4.75V	I _{OH} = -100μA	2.4	4.2		V
Voн	ingrinever output voltage	Output BI/RBO	$V_1=0.8V$, $V_1=2V$	$I_{OH} = -50 \mu A$	2.4	4.2		. V
Іон	High-level output current	Outputs a - g	Vcc=4.75V.V _I =0.8V	, V _I =2V, V _O =0.85V	-1.3	2		mA
		0		I _{OL} =2mA		0.25	0.4	V
.,		Outputs a ~ g	V _{CC} =4.75V	I _{OL} =6mA		0.35	0.5	V
VoL	Low-level output voltage	Output BI/RBO	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =1.6mA		0.25	0.4	· v
		Curput BI/ NBO		I _{OL} =3.2mA		0.35	0.5	V
	III-b II	Inputs BI/RBO	V _{CC} =5.25V, V _I =2.7	'V			20	μА
hн ·	High-level input current	other than BI/RBO	V _{CC} =5.25V, V _I =10V	,			0.1	mA
I	Low level input ourrant	Input BI/RBO	V 5 25V V - 0 4				-1.2	mA
hL	Low-level input current	Other inputs	$V_{CC} = 5.25V \cdot V_{I} = 0.4$	· v			-0.4	mA
los	Short-circuit output current	Output BI/RBO	V _{CC} =5.25V. V _O =0V		-0.3		-2	mA
loc	Supply current		V _{CC} =5.25V (Note 2)			25	38	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

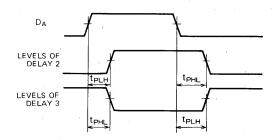
$\textbf{SWITCHING} \ \ \textbf{CHARACTERISTICS} \ \ (\textbf{V}_{\text{CC}} = 5 \textbf{V} \ , \ \textbf{T}_{\textbf{a}} = 25 ^{\circ} \textbf{C} \ , \ \text{unless otherwise noted})$

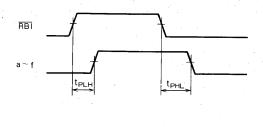
Symbol	Parameter	Test conditions		Unit		
Symbol	rarameter	Test conditions	Min	Тур	Max	Oiiit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	R _L =4kΩ		30	100	ns
tPHL	time, from input D_A to outputs a \sim g	C _L =15pF (Note 3)		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	R _L =6kΩ		40	100	ns
tphL	time, from input \overline{RBI} to outputs a $\sim f$	C _L =15 pF (Note 3)		45	100	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w = 500ns, V_P =3 V_P -P, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





Note 2: I_{CC} is measured with all inputs at 4.5V.

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE

DESCRIPTION

The M74LS51P is a semiconductor integrated circuit containing dual 2-wide 2-input/3-input AND-OR-INVERT gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d=5.5mW typical)
- High speed (tpd=7ns typical)
- Low output impedance
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Schottky TTL technology enables input high breakdown voltage, high speed, low power dissipation and high fan-out.

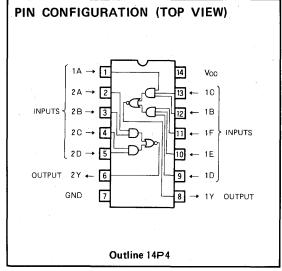
This device consists of a NOR gate with two 2-input AND gates as the inputs and a NOR gate with two 3-input AND gates as the inputs, and the following logical expressions are yielded:

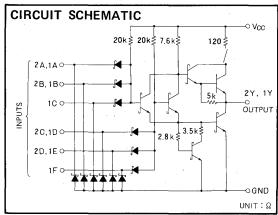
$$1Y = \overline{1A \cdot 1B \cdot 1C + 1D \cdot 1E \cdot 1F}$$
$$2Y = \overline{2A \cdot 2B + 2C \cdot 2D}$$

FUNCTION TABLE

М	N	Υ
L	L	Ξ.
Н	L	L
L	Н	L
Н	Н	L

 $M = 1A \cdot 1B \cdot 1C$ $N = 1D \cdot 1E \cdot 1F$ $AND \cdot OR$ $M = 2A \cdot 2B$ $N = 2C \cdot 2D$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	. V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range-		-65~+150	°C

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	D		Unit			
Symbol	Paramete	31	Min	Тур	Max ,	Omit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	Lauda al auta de aurant	V _{OL} ≦0.4V	. 0		4	mA
loL	Low-level output current	, V _{0L} ≤0.5V	0		8	mA .

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0 1 1	Parameter				Limits		Unit
Symbol	rarameter	lest co	Test conditions			Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V -
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	- 18mA			-1.5	٧
V _{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_1 = 0.8V$ $I_{OH} = -400\mu A$		2.7	3.4		. V
.,	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	0.5	V
	High level input a great	V _{CC} =5.25V, V _I =3	2.7V			20	μΑ
liH	High-level input current	V _{CC} =5.25V, V _I =	10V			0.1	mΑ
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		-20		- 100	m A
Госн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V			0.8	1.6	mA
lock	Supply current, all outputs low	V _{CC} =5.25V, V _I =4.5V			1.4	2.8	mA

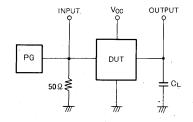
 $[\]star$: All typical values are at V_{CC}= 5V, T_a= 25°C).

Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

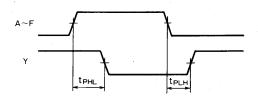
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	, al allie tel	rest conditions	Min	Тур	Max	Onit
tpLH	Low-to-high-level output propagation time	C _L =15pF		6	20	ns
tPHL	High-to-low-level output propagation time	(Note 2)		8	20	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P = $3V_{P.P.}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

DESCRIPTION

The M74LS73AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , inputs J and K and direct reset input $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct reset input
- Q and Q outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

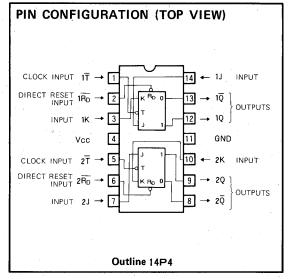
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when \overline{T} changes from high to low, the J and K signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By setting $\overline{R_D}$ low, Q and \overline{Q} are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, $\overline{R_D}$ must be kept high.

Also available is M74LS107AP with the same functions and electrical characteristics. This offers easy mounting with V_{CC} positioned at pin 14 and GND at pin 7.



FUNCTIONAL TABLE (Note 1)

Ŧ	R _D	J	K	Q	Q
Х	L	Х	. X	L	Н
1	н	Н	н	Tog	ggle
,	Н	L	Н	L .	Н
. ↓	Н	Н	L	Н	L
↓	Н	L.	L	Q ⁰	Q ₀
Н	Н	. X	Х	Q ⁰	Q ⁰

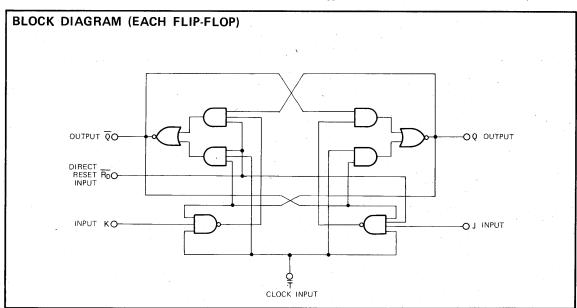
Note 1 \downarrow : Transition from high to low-level (negative edge trigger)

X : Irrelevant

Q0: level of Q before the indicated steady-state input conditions were established.

 \overline{Q} 0: level of \overline{Q} before the indicated steady-state input conditions were established.

Toggle: complement of previous state with ↓ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	` V
Vı	Input voltage		-0.5~+15	· V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°°
Tstg	Storage temperature range		−65∼+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	Parame	eter	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	. 5	5.25	٧	
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ	
		V _{OL} ≦0.4V	0		4	mΑ	
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Test condi			Limits		
Зуппоот	raiameter		rest condi	tions	Min	. Тур 🛊	Max	Unit
ViH	High-level input voltage				2			٧
ViL	Low-level, input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 m A			— 1.5	٧
Voн	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-400		2.7	3.4		٧
	N. C.		V _{CC} =4.75V	I _{OL} =4mA	-	0.25	0.4	V
VoL	DL Low-level output voltage		$V_{i=0.8V}, V_{i=2V}$	I _{OL} =8mA		0.35	0.5	٧
		J, K					20	μА
	1	.R _D	V _{CC} =5.25V				60	μĀ
l	List level in the second	Ŧ	V ₁ =2.7V			,	80	μΑ
lн	High-level input current	J, K	\/				0.1	· mA
		RD	V _{CC} =5.25V				0.3	mA
		Ť	V₁= 10 V				0.4	mA
		J, K	V _{CC} =5.25V				-0.4	mA
h <u>L</u>	Low-level input current	R _D T	V _I =0.4V	•			-0.8	m A
los	Short-circuit output current (No	ote 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
lcc	Supply current		V _{CC} =5.25V (Note 3)			4	6	mA

 $[\]star$: All typical values are at $V_{CC} = 5 \, V$, $T_a = 25 ^{\circ} C$

SWITCHING CHARACTERISTICS ($V_{CC}=5\,V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	Farametei	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency	·	30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	. 20	ns
t _{PHL}	time, from T to Q, Q	C _L = 15 pF (Note 4)		6	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	20	ns
t _{PHL}	time, from $\overline{R_D}$ to Q , \overline{Q}			. 7	20	ns

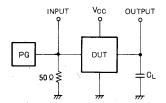


Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current measurements should be done with Q and \overline{Q} set alternately high and \overline{T} should be set low during actual measurement.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

Note 4: Measurement circuit

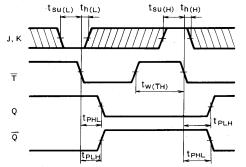


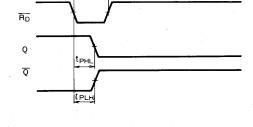
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_o = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0	B	Total	Limits			11-3
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _W (TH)	Clock input T high pulse width	-	20	12		ns
tw(RD)	Direct reset input pulse width		25	4		ns
tr	Clock rise time			650	100	ns
t _f :	Clock fall time			900	100	ns
t _{su(H)}	Setup time high T to J, K		20	9		ns
t _{su(∟)}	Setup time low T to J, K		20	10		ns
th(H)	Hold time high Tto J, K		0	- 8		ns
t _{h(L)}	Hold time low T to J, K		0	– 5		ns

TIMING DIAGRAM (Reference level = 1.3V)



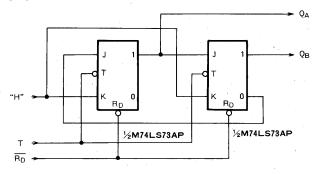


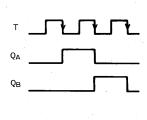
tw(RD)

Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

High-speed 1/3 divider





OUTPUTS

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS74AP is a semiconductor intergrated circuit containing 2 D-type positive edge-triggered flip-flop circuits with discrete terminals for clock input T, data input D and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Each flip-flop can be used independently.
- Direct set and reset inputs
- Positive edge-triggering
- Q and Q outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and \overline{Q} in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both S_D and R_D are low, $Q=\overline{Q}=$ high. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a D-type filip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

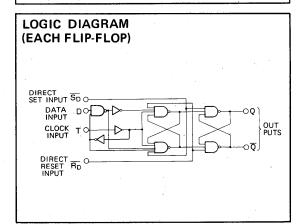
FUNCTION TABLE

SD	Ŕ₽	Т	D	Q	Q
L	Н	х	Х	Н	٦,
Н	L	X	· X	L	Н
L	L	Х	х	н*	н*
Н	Н	L	X	Q ⁰	Ō0
Н	Н	t	Н	Н	L
Н	Н	t	L	L	Н

- Note 1: ↑: Transition from low to high-level
 - $Q^{\,0}$. level of Q before the indicated steady-state input conditions were established.
 - $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established.
 - X : Irrelevan
 - Nonstable, it will not persist when RD, SD inputs return to their inactive (high) level.

DIRECT RESET INPUT $1\overline{R}_D \rightarrow 1$ 14 V_{CC} DATA INPUT $1D \rightarrow 2$ $13 \leftarrow 2\overline{R}_D$ DIRECT RESET INPUT CLOCK INPUT $1T \rightarrow 3$ $17 \leftarrow 17$ $17 \leftarrow 17$ CLOCK INPUT DIRECT SET INPUT $1\overline{S}_D \rightarrow 4$ $11 \leftarrow 2\overline{S}_D$ DIRECT SET INPUT OUTPUTS $10 \leftarrow 17$ $10 \leftarrow 1$

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage	:	-0.5~+7	V
V _I °	Input voltage		$-0.5 \sim +5.5$	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		−20∼+75	°C
Tstg	Storage temperature range		-65~+150	°C

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Cbal	Parameter			Limits				
Symbol	Paramet	er	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА		
1	Low-level output current	V _{OL} ≦0.4V	0		4	mA		
lo _L	Low-level output current	V _{OL} ≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Combal	D	Parameter Test conditions		Test conditions		Limits		
Symbol	rarameter			aitions	Min	Typ*	Max	. Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage	Low-level input voltage					0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	18mA			-1.5	V
V _O H	High-level output voltage		$V_{CC} = 4.75V, V_1 = 0.8$ $I_{OH} = -400\mu A$	V, V _I =2V	2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
			V _I =0.8V, V _I =2V	I _{OL} = 8mA		0.35	0.5	V
		D, T	V _{CC} =5.25V, V _I =2.7	V			20	
. 1	High-level input current	SD, RD	VCC-5.25V, VI-2.7	v _			40	μΑ
Чн	High-level input current	D, T	5 05)()/ -40)	,			0.1	
		SD, RD	$V_{CC} = 5.25V, V_1 = 10V$,			0.2	mΑ
		D, T	5 051/ 1/ 0 4	N. /			-0.4	
(IIL	Low-level input current	SD, RD	$V_{CC} = 5.25V, V_1 = 0.4$	• •			-0.8	mΑ
los	Short-circuit output current (N	Note 2)	V _{CC} =5.25V, V _O =0V	,	-20		-100	mA
Icc	Supply current		V _{CC} =5.25V, (Note 3)			4	8	mA

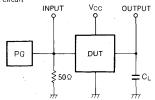
^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Complete	Parameter	Test conditions	Limits			Unit
Symbol	r al afficier	rest conditions	Min	Тур	Max	Omit .
f _{max}	Maximum clock frequency		25	50		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	25	ns
t _{PHL}	time, from T to Q, Q	C _L =15pF		11	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 4)		. 8	25	ns
t _{PHL}	time, from $\overline{S_D}$, $\overline{R_D}$ to Q , \overline{Q}			-11	40	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_P .p., Z_0 = 50 Ω
- (2) C_L includes probe and jig capacitance.

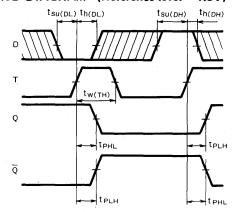
Note 3: Measurement circuit

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

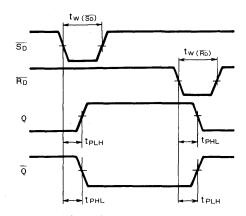
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	
tw(TH)	Clock input T high pulse width		25	4		ns
tw(SD, RD)	Direct set and reset inputs SD, RD pulse width		25	4		ns
tsu(DH)	Setup time high D to T		- 20	10	-	ns
t _{su(bL)}	Setup time low D to T		20	. 8		ns
th(DH)	Hold time high D to T		5	- 5		ns
th(DL)	Hold time low D to T		5	- 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

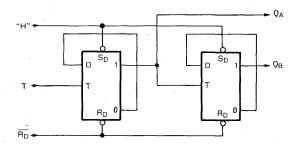


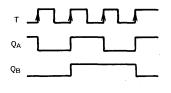
Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.



APPLICATION EXAMPLE

%divider





MITSUBISHI LSTTLS M74LS75P

4-BIT BISTABLE LATCH

DESCRIPTION

The M74LS75P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Q and \overline{Q} .

FEATURES

- Enable inputs common to two circuits each
- \mathbf{Q} and $\overline{\mathbf{Q}}$ outputs
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and \overline{Q} . When the D signal changes, the signal that appears in outputs Q and \overline{Q} also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and \overline{Q} does not change even if D is changed.

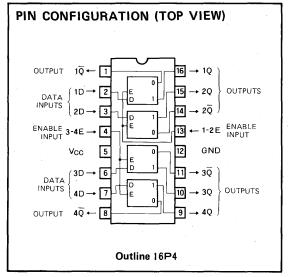
Also provided is the M74LS375P with the same functions and electrical characteristics. With the V_{CC} positioned at pin 16 and GND at pin 8, this device makes for easy mounting.

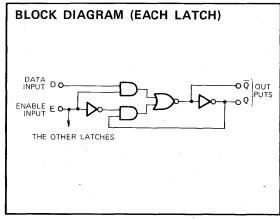
FUNCTION TABLE (Note 1)

E	D	Q	Q
н	Н	Н	L
Н	L	L	н
L	×	Q ⁰	Q ⁰

Note 1 $Q^0, \overline{Q^0}$: Level of Q and \overline{Q} before the indicated steady-state input conditions were established.

X : Irrelevant





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	٧ .
Vo	Output voltage	High-level state	-0.5~+V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	℃

4-BIT BISTABLE LATCH

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Combal				Limits				
Symbol	Parame	rarameter		Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Тон	High-level output current	V _{OH} ≥ 2.7V	0		- 400	μA		
loL	Low-level output current	V _{OL} ≤0.4∨	0		4	mΑ		
		V _{OL} ≤0.5V	0		8	mΑ		

ELECTRICAL CHARACTERISTICS (Ta = -20 - +75°C, unless otherwise noted)

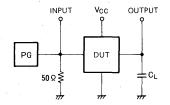
Symbol	Parameter		Test conditions	Test conditions		Limits		
Symbol			rest conditions			Typ *	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA	7			- 1.5	V
Voн	High-level output voltage		$V_{CC} = 4.75V, V_1 = 0.8V$ $V_1 = 2V, I_{OH} = -400\mu A$	*,	2.7	3.5		٧
V	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
V _{OL}	Low-lever output vortage		$V_1 = 0.8V, V_1 = 2V$	IOL=8mA		0.35	0.5	V
		D	V _{CC} = 5.25V				20	
	Uligh lovel inner a consess	E	V _I = 2.7V				80	μΔ
lін	High-level input current	D	V _{CC} = 5.25V				0.1	
		E	V ₁ = 10 V				0.4	mΑ
	Low level input ourrent	, D	V _{CC} = 5.25V				-0.4	^
TIE.	Low-level input current E	V₁ = 0.4V				- 1.6	mΑ	
los	Short-circuit output current (No	te 2)	V _{CC} =5.25V, V _O = 0 V		-20		- 100	mA
lcc	Supply current		V _{CC} = 5.25V (Note 3)			6.3	12	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Syllibol		rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	27	ns
t _{PHL}	time, from input D to output Q			8	17	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O 45.5 (New 4)		10	20	ns
t _{PHL}	time, from input D to output $\overline{\mathbb{Q}}$			6	15	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 4)		13	27	ns
t _{PHL}	time, from input E to output Q			12	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	30	ns
t _{PHL}	time, from input E to output Q	•		6	15	ns

Note 4: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .

Note 2: All measurements should be done guickly and not more than one output should be shorted at a time,

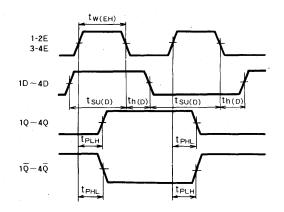
Note 3: I_{CC} is measured with all inputs at OV.

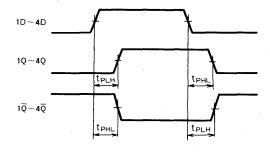
⁽²⁾ CL includes probe and jig capacitance.

4-BIT BISTABLE LATCH

TIMING REQUIREMENTS (Vcc=5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	r at attreter	lest conditions	Min	Тур	Max	Unit
tw(EH)	Enable input E high pulse width		20	7		ns
tsu(D)	Setup time 1D ~ 4D to E		20	12		ns
th(D)	Hold time 1D ~ 4D to E		8	5		ns





High-level 3-4E, 1-2E

MITSUBISHI LSTTL **M74LS76A**

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS76AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input T, inputs J and K and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Each fli-flop can be used independently
- Direct set and reset inputs
- Q and Q outputs
- Wide operating temperature range (T_a = −20~+75°C)

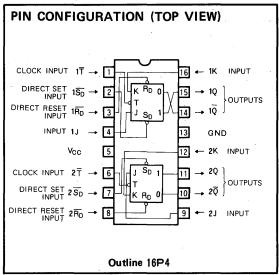
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While T is high, signals J and K are put in the read-in state, and when T changes from high to low, the J and K signals immmediately before the change emerge in outputs Q and $\overline{\mathbf{Q}}$ in accordance with the function table. By using $\overline{\mathbf{S}_{\mathbf{D}}}$ and RD this IC can be made into a direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, $Q = \overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

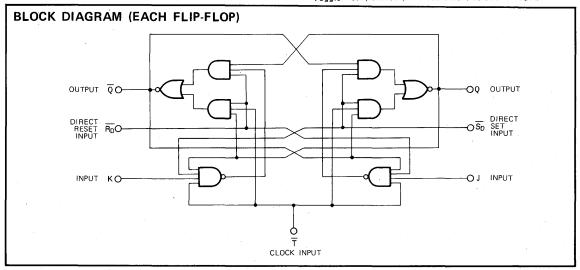
Also available is M74LS112AP with the same functions and electrical characteristics. This offers easy mounting Note 1 1: Transition from high to low-level (negative edge trigger) with V_{CC} positioned at pin 16 and GND at pin 8.



FUNCTION TABLE (Note 1)

Ŧ	S _D	Ŕ _D	J	K,	Q	Q	
Х	L	Н	Х	Х	Ι	L	
Х	н	L	Х	Х	L.	н	
Х	L	L	Х	Х	H*	· H*	
↓	н	н	н	Ι	Toggle		
1	н	Н	L	н	L	н	
1	н	Н	н	L	н	L	
↓	н	н	L	L	Ó ₀	Q0	
Н	Н	н	X	Х	Q ⁰	Q ⁰	

- X : Irrelevant
- *: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D}$ are set high, the status of Q and \overline{Q} cannot be anticipated.
- Q0: level of Q before the indicated steady-state input conditions were established.
- 00: level of 0 before the indicated steady-state input conditions were established.
- Toggle: Complement of previous state with ↓ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	. v
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	ο σ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$), unless otherwise noted)

6	Parameter			Unit		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mΑ
loL		V _{OL} ≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			
Зупци	rarameter		rest cond	itions	Min	Typ *	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage	•					0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			-1.5	V
Vон	High-level output voltage	High-level output voltage		V A	2.7	3.4		v .
V _{OL}	High-level input current	-	$V_{CC} = 4.75V$ $V_{I} = 0.8V, V_{I} = 2V$	I _{OL} =4mA		0.25	0.4	V
		J, K S _D , R _D	V _{CC} =5.25V V _I =2.7V				20 60 80	μΑ
ін	Low-level input current	J, K S _D , R _D	V _{CC} =5.25V V _I =10V				0.1 0.3 0.4	mA
I _{IL}	Low-level output voltage	J, K S _D , R _D , T	V _{CC} =5.25V V _I =0.4V (Note 2)				-0.4 -0.8	· mA
los	Short-circuit output current (no	ote 3)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
lcc	Supply current		V _{CC} =5.25V (Note 4)			4	6	mA

^{* :} All typical values are at $V_{CC} = 5 V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0	Parameter	Test conditions	Limits			Unit
Symbol	bol rarameter lest conditions		Min	Тур	Max	Unit
fmax	Maximum clock frequency		30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	20	ns
t _{PHL}	time, from T to Q, Q	C _L = 15 pF (Note 5)		7	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	20	ns
t _{PHL}	time, from \overline{S}_D , \overline{R}_D to Q , \overline{Q}			7	20	ns

Note 2: $\overline{S_D}$ and $\overline{R_D}$ should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

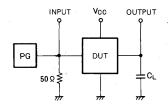
Note 4: Supply current measurements should be done with Q and $\overline{\mathbb{Q}}$ set alternately high and $\overline{\mathbb{T}}$ should be set low during actual measurement,

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

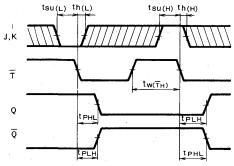
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

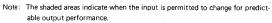
Complete	Parameter	Test and distant	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		20	12		ns
tw(SD, RD)	Direct set, reset pulse width		25	4	Ī	ns
tr	Clock rise time			650	100	ns
tf	Clock fall time	• •		900	100	ns
t _{su(H)}	Setup time high J, K to T		20	12		ns
t _{su(L)}	Setup time low J, K to T		20	12		ns
t _{h(н)}	Hold time high J, K to T		0	10		ns
t _{h(L)}	Hold time low J, K to T		0	– 6 ,		ns

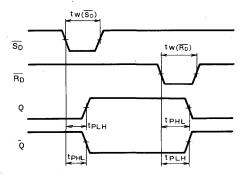
Note 5: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_P .P, Z_Q = 50 Ω .
- (2) C_L includes probe and jig capacitance.







MITSUBISHI LSTTLS M74LS83AP

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74LS83AP is a semiconductor integrated circuit containing a 4-bit binary look ahead carry type full adder.

FEATURES

- High speed with look-ahead carry addition
- Possible configuration of systems with partial look-ahead carry
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

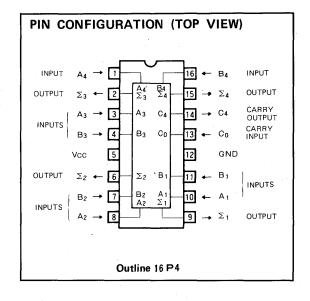
General purpose, for use in industrial and consumer equipment.

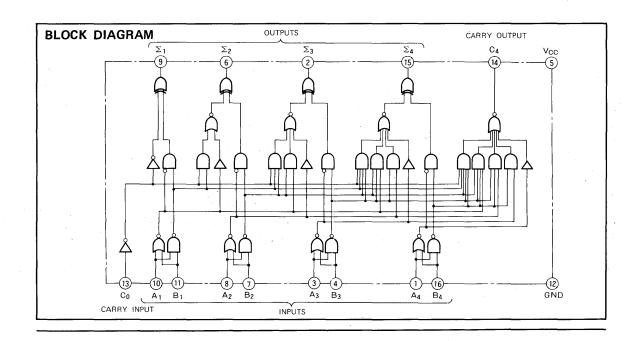
FUNCTIONAL DESCRIPTION

This device performs the addition of two 4-bit binary numbers. When a 4-bit binary number is applied to inputs $A_1 \sim A_4$ and $B_1 \sim B_4$ and the carry signal from the previous digit is applied to input C_0 , the respective bit sum output and carry outputs for the next upper digit appear in outputs $\Sigma_1 \sim \Sigma_4$ and C_4 .

This adder features full internal look ahead across all four bits generating the carry term in 8ns typically. Therefor, the carry output can be obtained in a delay time of 8Nns when N-stages are connected and a 4N-bit parallel adder is configured. (Refer to application example.)

Also available is the M74LS283P with the same functions and electrical characteristics and with a pin 16 V_{CC} and 8 GND configuration.





4-BIT BINARY FULL ADDER WITH FAST CARRY

FUNCTION TABLE (Note 1)

C _{k-1}	A _k	Bk	$\Sigma_{\mathbf{k}}$	Ck
L	L	L	L	L `
L	н	L	н	L
L	L	H	Н	L
L	Н	Н	L	Н
. н	L	Γ	. Н	L
Н	Н	L	L	Н
Н	L	Н	L	Н
Н	Н	Н	Н	H.

Note 1 G_k and Σ_k are the carry output and sum output obtained by adding A_k , B_k and G_{k-1} (carry input), and they are expressed in the following logical expression.

 $\Sigma_k = A_k \oplus B_k \oplus C_{k-1}$

 $C_k = A_k \cdot B_k + (A_k + B_k) \cdot C_{k-1}$

Where $k = 1 \sim 4$

⊕=Exclusive OR

+=OR

• = AND

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		−65∼+150	℃

$\begin{tabular}{ll} \textbf{RECOMMENDED} & \textbf{OPERATING}. & \textbf{CONDITIONS} & (\textbf{T}_{\textbf{a}} = -20 \sim +75^{\circ}\text{C}, \text{ unless otherwise noted}) \\ \end{tabular}$

C				Limits		Unit
Symbol	Parame	Min	Тур	Max		
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
loL	Low-level output current	V _{OL} ≦0.4V	0		4	mA
		V _{0L} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			
					Min	Typ∗	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
V _{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-400\mu A$		2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V V _I =0.8V, V _I =2V	$I_{OL} = 4mA$ $I_{OL} = 8mA$		0.25	0.4	V
	High-level input current	Co				20	μА	
		A1~A4, B1~B4	V _{CC} =5.25V, V _I =2.7V					40
UН .		Co	V _{CC} =5.25V, V _I =10V			0.1	mA	
-		A1~A4, B1~B4				0.2		
lii.	Low-level input current C_0 $A_1 \sim A_4$, $B_1 \sim B_4$	C ₀ ,	V _{CC} =5.25V, V _I =0.4V				-0.4	mΑ
		VGC-5.25V, VI-0.4V				-0.8	IBA	
los	Short-circuit output current (Note 2) V _{CC} =5.25V', V _O =0V			-20		- 100	mA	
Icc	Supply current		V _{CC} =5.25V, V _I =0V			22	39	mΑ
			V _{CC} =5.25V, V _I =0V,	V _I =4.5V (Note 3)		19	34	mΑ
			$V_{CC} = 5.25V, V_{I} = 4.5$	V .		19	34	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

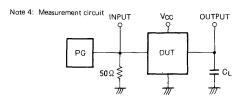
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Measurement should be conducted with inputs B₁-B₄ at 0V and the other inputs at 4.5V.

4-BIT BINARY FULL ADDER WITH FAST CARRY

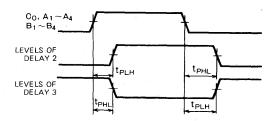
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	lest conditions	Min	Тур	Max	· Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	24	ns
tpHL	time, from input C_0 to outputs $\Sigma_1 - \Sigma_4$			13	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	24	ns
t _{PHL}	time, from inputs $A_1 \sim A_4$, $B_1 \sim B_4$ to outputs $\sum_1 \sim \sum_4$	C ₁ = 15 pF (Note 4)		11	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OL = 13DF (Note 4)		8	17	ns
t _{PHL}	time, from input Co to output C4			8	22	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	17	ns
t _{PHL}	time, from inputs $A_1 \sim A_4$, $B_1 \sim B_4$ to output C_4			8	17	ns



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w = 500ns, V_P =3 V_P , V_P =00 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



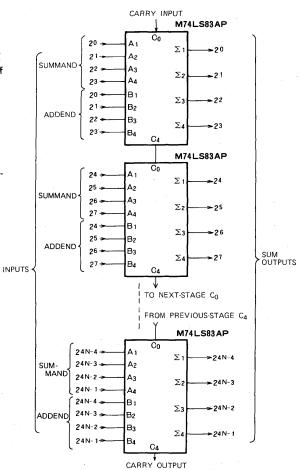
APPLICATION EXAMPLE

Shown on the right is a 4N-bit binary parallel adder using N number of M74LS83AP devices. The typical delay times of the carry output in this circuit are:

N = 1 (4 bits) 10.5ns N = 2 (8 bits) 21ns N = 3 (12 bits) 31.5ns N = 4 (16 bits) 42ns

N = 4 (16 bits) 42ns N = 8 (32 bits) 84ns

This allows a high-speed ripple carry adder to be configured.



4-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS85P is a semiconductor integrated circuit containing a 4-bit digital comparator.

FEATURES

- Easy expansion of number of bits
- Binary or BCD comparison
- Wide operating temperature range (T_a=-20~+75°C)

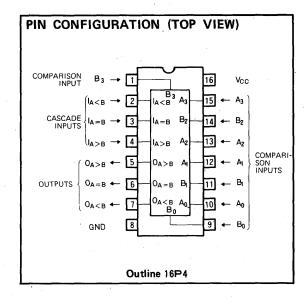
APPLICATION

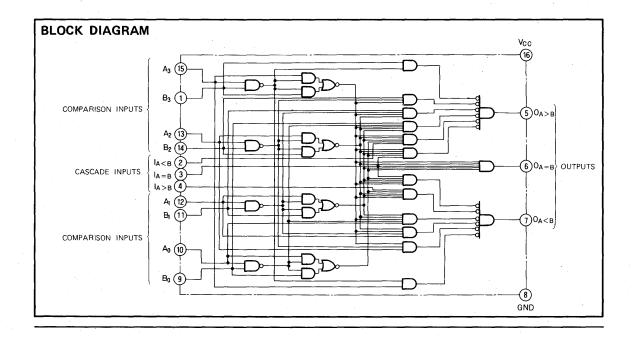
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

By applying two sets of 4-bit binary numbers A and B to be compared to comparison inputs $A_0 \sim A_3$ and $B_0 \sim B_3$ and by setting cascade input $I_{A=B}$ high, high appears in outputs $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ in accordance with the magnitude. This is used for connecting cascade inputs $I_{A>B}$, $I_{A\,<\,B}$ and $I_{A\,=\,B}$ and increasing the number of bits.

(Refer to application example)





M74LS85P

4-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE (Note 1)

A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A>B}	IA <b< th=""><th>I_{A=B}</th><th>O_{A>B}</th><th>O_{A<b< sub=""></b<>}</th><th>O_{A=B}</th></b<>	I _{A=B}	O _{A>B}	O _{A<b< sub=""></b<>}	O _{A=B}
A 3>B 3	Х	Х	×	Х	×	х	н	L	L
A 3 <b 3<="" td=""><td>X</td><td>X</td><td>×</td><td>.X</td><td>X</td><td>х</td><td>L</td><td>Н</td><td>L</td>	X	X	×	. X	X	х	L	Н	L
A 3=B 3	A ₂ >B ₂	х	×	Х	X	X	н	L	L
A ₃ =B ₃	A 2 <b 2<="" td=""><td>X</td><td>×</td><td>х</td><td>×</td><td>х</td><td>L</td><td>Н</td><td>L</td>	X	×	х	×	х	L	Н	L
A 3=B 3	A 2=B 2	A ₁ >B ₁	×	Х	×	х	н	L	L
A 3=B 3	A 2=B 2	A1 < B1	Х	Х	X	х	L	Н	L
A 3=B 3	A 2=B 2	A1=B1	A ₀ >B ₀	Х	X	х	н	L	L
A 3=B 3	A 2=B 2	A ₁ =B ₁	A ₀ <b<sub>0</b<sub>	Х	X	X	L.	н	L
A 3=B 3	A 2=B 2	A ₁ =B ₁	A 0=B 0	н	L	L	н	L .	L
A 3=B 3	A ₂ =B ₂	A1=B1	A 0=B 0	L	Н	L	L	Н	L
A 3=B 3	A 2=B 2	$A_1 = B_1$	A 0=B0	Х	X	Н	L	L	Н
A 3=B 3	A 2=B 2	A ₁ = B ₁	A 0=B 0	н	Н	L	L	L	L
A 3=B 3	A 2=B 2	$A_1 = B_1$	A ₀ =B ₀	L	L	L	н	Н	L

Note 1, X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = $-20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions .	Limits	Unit
Vcc	Supply voltage	· ·	-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		- 65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ} \! \text{C}$, unless otherwise noted)

	Parameter			11-24		
Symbol	Parame	, ratameter			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μΑ
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
lor		V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

C	Danasa		Test cond	litions		Limits		Unit
Symbol	Parame	eter	rest cond	ITTOTIS	Min	Тур 🛊	Max	. Unit
VIH	High-level input voltage	vel input voltage			2			٧
VIL	Low-level input voltage						0.8	>
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 m A			-1.5	>
Voн	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8V$ $V_{I} = 2V, I_{OH} = -400 \mu A$		2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} =4.75V			0.25	0.4	V V
	High-level input current	IA <b, ia="">B A₀~A₃,B₀~B₃,I_{A=B}</b,>	V _{CC} =5.25V	102 5,			20	μΑ
нн	riigii-level input current	A < B, A > B $ A \cap A _3, B \cap B _3, A = B $	$V_{CC} = 5.25V$ $V_1 = 10V$				0.1	mA
li L	Low-level input current	A <b, a="" ="">B A 0~A 3,B 0~B 3, A=B</b,>	V _{CC} =5.25V V _I =0.4V				-0.4 -1.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V		-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)	11.		11	20	mA

 $[\]clubsuit$: All typical values are at VCC=5V, Ta= 25°C.

Note 2: All measurements must be done quickly and not more than output should be shorted at a time.

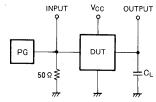
Note 3: $\, I_{CC}$ is measured with $\, I_{A=B}$ at 0V and with all other inputs at 4.5V.

4-BIT MAGNITUDE COMPARATOR

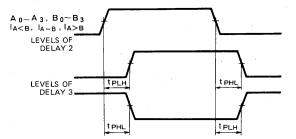
SWITCHING CHARACTERISTICS (VCC=5V, Ta=25°C, unless otherwise noted)

			Test conditions		Limits	:	Unit
Symbol	Parameter		rest conditions	Min	Тур	Max	Unit
t _{PLH}		Number of delay			6		ns
t PHL	Low-to-high-level, high-to-low-level	gate steps 1			11		ns
tpLH	output propagation time, from	Number of delay			10		ns
t _{PHL}	inputs, $A_0 \sim A_3$, $B_0 \sim B_3$ to outputs $OA < B$, $OA = B$, $O_A > B$	gate steps 2			18		ns
tpLH		Number of delay			12	36	ns
t _{PHL}		gate steps 3			20	30	ns
tpLH		Low-to-high-level, high-to-low-level output propagation			16	45	ns
t _{PHL}	time, from inputs $A_0 \sim A_3$, $B_0 \sim B_3$ $O_A < B$, $O_A = B$, $O_A > B$	to outputs			20	45	ns .
tpLH	Low-to-high-level, high-to-low-level o	utput propagation			6	22	ns
t _{PHL}	time, from input IA=B to outputs C	$O_{A < B}$, $O_{A > B}$			12	17	ns
tpLH	Low-to-high-level, high-to-low-level or	utput propagation			7	20	ns
t _{PHL}	time, from input IA=B to output OA	.=.B			13	26	ns
tpLH	Low-to-high-level, high-to-low-level of				9	22	ns
t _{PHL}	time, from inputs IA <b, ia="">B to o OA<b, oa="">B</b,></b,>	utputs			15	- 17	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P =3 V_P -P, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

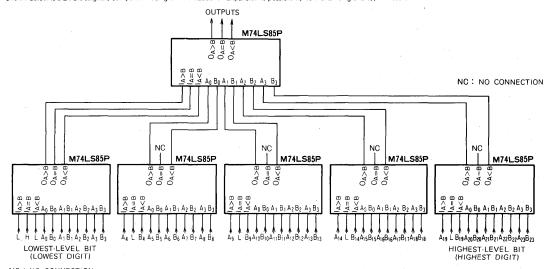


M74LS85P

4-BIT MAGNITUDE COMPARATOR

APPLICATION EXAMPLES

(1) Shown below is a 24-bit (digital) comparator using the M74LS85P. Expansion is possible up to n bits using this type of cascade connection.



NC: NO CONNECTION

(2) Shown below is an n-bit comparator using the M74LS85P. The speed is decreases as the number of bits in the configuration below increases. configuration below.



QUADRUPLE 2-INPUT EXCLUSIVE OR GATES

DESCRIPTION

The M74LS86P is a semiconductor integrated circuit containing 4 dual-input exclusive-OR gates.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (Pd = 30.5mW typical)
- High speed (tpd = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

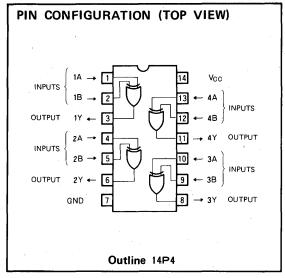
FUNCTIONAL DESCRIPTION

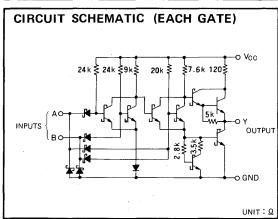
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

Α	В	Υ
L	L.	L
. н	L	н
L	Н	Н
Н	Н	L





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 \, ^{\circ}\!\!\! \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		$-0.5 \sim +7$	V
V ₁	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5∼ V _{CC}	V
Topr	Operating free-air ambient temperature range	·	-20~+75	°c
Tstg	Storage temperature range		− 65∼ + 150	°C

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

C h l	Daywasaa			Limits			
Symbol	Parameter	i ai ai i etei			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _{OH} ≥2.7V	0		400	μА	
1		V _{OL} ≤0.4V	0		4	mA	
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Constant	Parameter		Test conditions		Limits		
Symbol	Parameter	lest condi	tions	Min	Typ*	Max	Unit
· VIH	High-level input voltage		2			V	
VIL	Low-level input voltage				0.8	٧	
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	$V_{CC} = 4.75V$, $I_{IC} = -18 \text{ mA}$			- 1.5	V
Voн	High-level output voltage	$V_{CC} = 4.75V, V_{I} = 0.8V$ $V_{I} = 2V, I_{OH} = -400 \mu A$		2.7	3.4		V
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0 .4	V
		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
r I _{IH}	High-level input current	$V_{CC} = 5.25V, V_{I} = 2.7$	V			40	μΑ
чн		$V_{CC} = 5.25V, V_I = 1.0$	V _{CC} =5.25V, V _I =10V			0.2	mΑ
t _{IL}	Low-level input current	V _{CC} =5.25V, V ₁ =0.4	V _{CC} =5.25V, V ₁ =0.4V			-0.8	mΑ
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V		- 20		-100	mA
lcc	Supply current	V _{CC} =5.25V (Note 2)			6.1	10	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

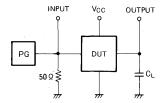
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 2: I_{CC} is measured with all inputs grounded.

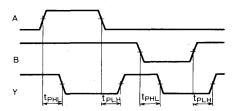
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation	$C_L = 15 p F$, Other input low (Note 3)		8	23	ns
t _{PHL}	time			12	17	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O - 15 o F Other input hint (New 2)		8	30	ns
t _{PHL}	time	C _L = 15pF, Other input high (Note 3)		10	22	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.



M74LS90P

DECADE COUNTER

DESCRIPTION

The M74LS90P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset inputs and direct 9-set inputs.

FEATURES

- Direct reset inputs provided
- Direct 9 set inputs provided
- Usable independently as binary and divide-by-five counter
- High-speed counting (f_{max}=75MHz typical)
- Wide operating temperature range (T_a=-20~+75°C)

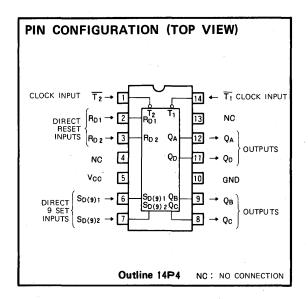
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

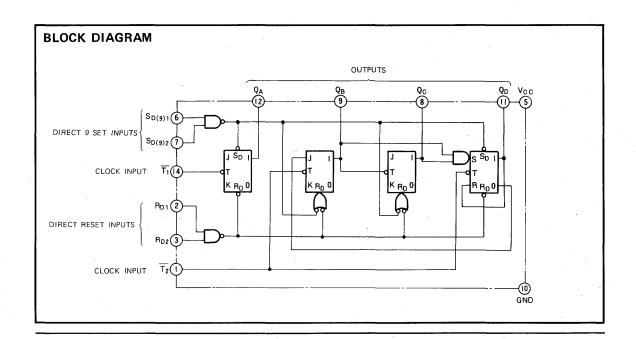
This device consists of independent binary and divide-by-five counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-five counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-five counters can be reset or



set to 9 simultaneously by setting direct reset inputs R_{D1} and R_{D2} high or direct 9 set inputs $S_{D(9)1}$ and $S_{D(9)2}$ high. For use as a counter, R_{D1} and/or R_{D2} , and $S_{D(9)1}$ and/or $S_{D(9)2}$, are set low.

Also provided is the M74LS290P with the same functions and electrical characteristics. Its GND positioning at pin 7 and V_{CC} at pin 14 makes for easy mounting.



DECADE COUNTER

FUNCTION TABLE (Note 1)

Ŧ	R _{D1}	R _{D 2}	S _{D(9)1}	S _{D(9)2}	QΑ	Qв	Qc	Q₽
X	н	Н	L	Х	L	L.	L	L
X	Н	н	х	L	Ł	L	L	L
X	×	X	н	I	н	L	L	н
\downarrow	L	×	L	Х		Co	unt	
↓ ↓	×	L	х	٦		Co	unt	
↓	L	×	Х	L	Count			
1	×	L	L	×	Count			

Note 1	1	•	Transition	from	high	to I	οw

X: Irrelevant

Count	QΑ	Qв	Qc	QD
0	L	L	L	L
1	н	L	, L	L
2	L	I	L	L
3	н	н	L	L
4	L	١	Н	L
5	I	L	H	L _
6	١	I	Ι	L
7	H	Ħ	н	L
8	L	L	L	н
9	н	L	L	Н

⁽¹⁾ Output \mathbf{Q}_{A} is connected to input B for BCD count.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Voc	Supply voltage	`	-0.5~+7	V	
.,	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5		
VI	Input vortage	Inputs R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	-0.5~ +15	7 V	
Vo	Output voltage	High level state	-0.5~ V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°C	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75 \text{ }^{\circ}$, unless otherwise noted)

Currhal	Parameter			Limits				
Symbol	Parameter		Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Тон	High-level output current	V _{OH} ≥2.7V	0		- 400	μА		
		V _{OL} ≤0.4V	0		4	mA		
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	P	arameter	Tost coa	nditions		Limits		Unit
Зупцы	, ,	ar di lie tei	rest coi	nations	Min	Тур 🛊	Max	Omt
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	V
Vон	High-level output voltage		$V_{CC} = 4.75V, V_1 = 0.8$ $V_1 = 2V, I_{OH} = -400$		2.7	3.4		٧
	1 1		V _{CC} =4.75V	I _{OL} =4 mA (Note 2)		0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA (Note 3)		0.35	0.5	V
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	V F 25V				20	
		T ₁ .	7 VCC=5.25V				40	μA
1	High-level input current	T ₂	V ₁ =2.7V				80	
I _{IH}	Ingir-level input current	T ₁	V _{CC} =5.25V				0.2	mA
		T ₂	V _I =5.5V				0.4	IIIA
*		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	$V_{CC} = 5.25V, V_i = 10$	V			0.1	mA
	,	R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	V _{CC} =5.25V				-0.4	
l _{IL}	Low-level input current	Ť ₁	V _I =0.4V				-2.4	m A
		T ₂	VI-0.4 V				-3.2	
los	Short-circuit output curre	ent (Note 3)	$V_{CC} = 5.25V, V_{O} = 0$	V	20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 4))		9	. 15	mA

 $[\]bigstar$: All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 4: I_{CC} is measured with R_{D1} , R_{D2} inputs grounded following momentary connection to 4.5V, and T_1 , T_2 , $S_{D(9)1}$ and $S_{D(9)2}$ inputs grounded following momentary connection to 4.5V, and T_1 , T_2 , $S_{D(9)1}$ and $S_{D(9)2}$ inputs grounded following momentary connection to 4.5V, and T_1 , T_2 , T_2 , T_3 , T_4 , T_4 , T_4 , T_4 , T_5 ,



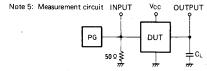
Note 2: Testing of output QA should be conducted with input T2 connected to output QA.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

DECADE COUNTER

SWITCHING CHARACTERISTICS (Voc=5V, Ta=25°C, unless otherwise noted)

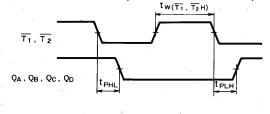
	D	Test conditions	Limits			Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		. 32	75		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		. 16	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	16	ns
t _{PHL}	time, from input T ₁ to output Q _A			8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	48	ns
t _{PHL}	time, from input T ₁ to output Q _D			16	50	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	16	ns
t _{PHL}	time, from input T ₂ to output QB			8	21	ns
t _{PLH}	Low-to-high-output, high-to-low-level output propagation	C _L = 15pF (Note 5)		15	. 32 /	ns
t _{PHL}	time, from input T ₂ to output QC	OL = 150F (Note 5)		15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		7	32	ns
t _{PHL}	time, from input T2 to output QD			8	35	ns
t _{PHL}	High-to-low-level output propagation time, from inputs RD1, RD2 to outputs QA, QB, QC, QD	· · ·		17	40	ns
t _{PLH}	Low-to-high-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QA, QD			10	30	ns
t _{PHL}	High-to-low-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QB, QC			14	40	ns

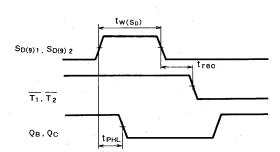


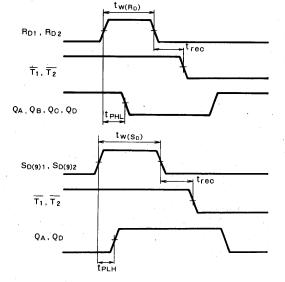
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_i =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
3911001	r arameter	rest conditions	Min	Тур	Max	Oillt
t _{w(Ţ, H)}	Clock input T ₁ high pulse width		15	6		ns
t _{w(T₂H)}	Clock input $\overline{T_2}$ high pulse width		30	17 .	,	ns
tw(RD)	Direct reset R _{D1} , R _{D2} pulse width	1	15	6		ns
tw(sp)	Direct 9 set SD(9)1, SD(9)2 pulse width		15	8		ns
t _r	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(Rp)	Recovery time RD1, RD2 to T1, T2	1	25	8		ns
trec(sp)	Recovery time SD(9)1, SD(9)2 to T1, T2]	25	8		ns









MITSUBISHI LSTTLS M74LS91P

8-BIT SHIFT REGISTER

DESCRIPTION

The M74LS91P is a semiconductor integrated circuit containing an 8-bit serial input-serial output shift register function.

FEATURES

- Synchronous serial input-serial ouptut
- Positive edge-triggering
- ullet Q_7 and \overline{Q}_7 outputs provided
- Wide operating temperature range (Ta=-20~75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

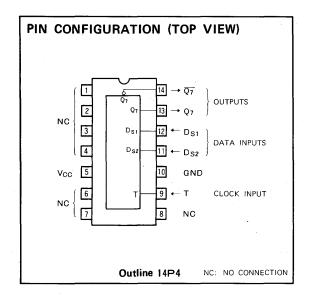
FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered R-S-T flip-flops and the serial data input D_{S1} , D_{S2} and $D_{S1} \cdot D_{S2}$ represents the first-stage flip-flop data input.

When D_{S1} and D_{S2} are both high and eight clock pulses are applied to clock input T, the high signal appears in Q_7 and the low signal in $\overline{Q_7}$. When one or more of the inputs is low and the eight clock pulses are applied to T, the low signal appears in $\overline{Q_7}$ and the high signal in $\overline{Q_7}$.

Data reading and shifting operations are performed when T changes from low to high.

Either D_{S1} and D_{S2} should be set low and eight or more clock pulses should be applied to T in order for all the 8 flip-flops to be set low.

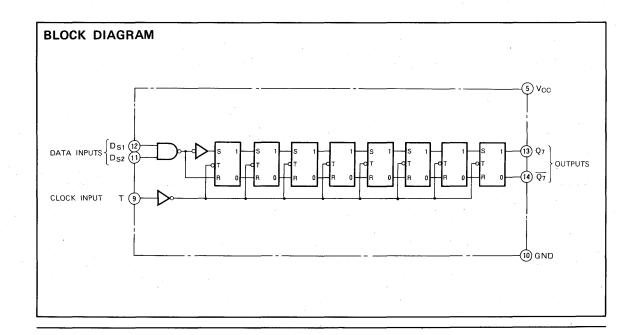


FUNCTION TABLE (Note 1)

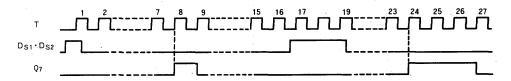
	<u> </u>		
. tr	1	tn+	3
D _{S1}	Ds2	Q7	Q7
L	L.	L	н
L	н	L	Н
н	L	L	Н
Н	Н	Н	L L

Note 1 tn : Bit time before clock

 t_{n+8} : Bit time after 8 clock pulses have been applied



OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage	-	-0.5~+7	V
Vı	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level state	-0.5~ Vcc	٧
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Paramet					
Symbol	. raidilet	er .	Min	Тур	Max 5.25 — 400	Unit
Voc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

					Limits		
Symbol	Parameter	lest cond	Test conditions		Typ *	Max·	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V.1 _{IC} =-	18mA			-1.5	V
,	High I and a state of the state	V _{CC} =4.75V, V ₁ =0.8V		2.7	2.5		V
VoH	VOH High-level output voltage	$V_1 = 2V \cdot I_{OH} = -400 \mu A$		2.7	3.5		٧
	Law level output voltage	V _{CC} = 4.75 V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8 V, V_1 = 2 V$	I _{OL} =8mA		0.35	0.5	· V
	High local income oursing	V _{CC} =5.25V, V _I =2.	7 V			20	μА
Iн	High-level input current	V _{CC} =5.25V, V _I =10V	V			0.1	mA
liL	Low-level input current	V _{CC} =5.25V, V _I =0.4	4 V			- 0.4	mA
los	Short-circuit output current	V _{CC} =5.25V. V _O =0\	(Note 2)	-20		- 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3))		12	20	mA

 $[\]star$: All typical values are at V_{CC}= 5V, T_a= 25°C

Note 2: All measurements should be done quickly.

Note 3: I_{CC} is measured with D_{S1} and D_{S2} at OV after 8 clock pulses have been applied to T

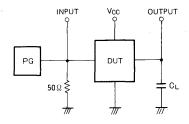
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
3yinboi	i a differen	rest conditions	Min	Тур	Max	· OIIIt
fmax	Maximum clock frequency		- 10	60		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L = 15 pF (Note 4)		12	40	ns
t _{PHL}	time, from input T to outputs Q_7 , $\overline{Q_7}$			15	40	ns

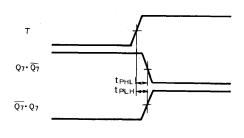
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

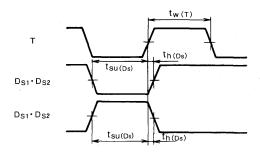
Symbol	Parameter	Test conditions	Limits			Unit
Symbol	raidnietei	rest conditions	Min	Тур	Max	Unit
tw(T)	Clock input pulse width		25	6		ns
tsu(Ds)	Setup time DS1, DS2 to T		25	7		ns
th(Ds)	Hold time DS1, DS2 to T		6	0		ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P.P.}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





MT4LS92P

DIVIDE-BY-TWELVE COUNTER

DESCRIPTION

The M74LS92P is a semiconductor integrated circuit containing an asynchronous divide-by-twelve counter function with direct reset inputs.

FEATURES

- Direct reset input provided
- Usable independently as binary and divide-by-six counter
- High-speed counting (f_{max} = 80MHz typical)
- Wide operating temperature range (T_a = -20~+75°C)

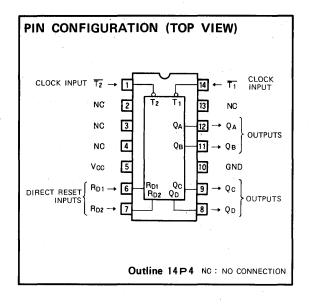
APPLICATION

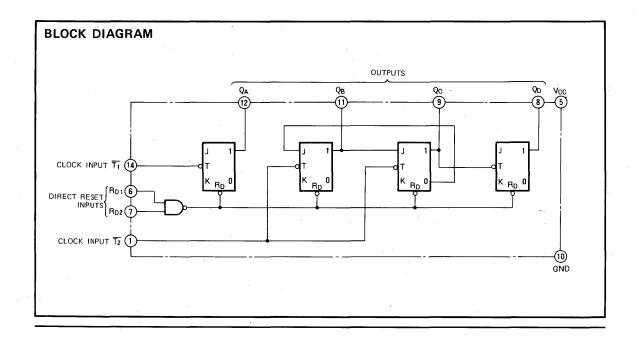
General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-6 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-6 counter. When employed as a divide-by-12 counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the output appears in outputs Q_A , Q_B , Q_C and Q_D in accordance with the function table. The code appearing in the output is not pure binary code. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-6 counters can be reset simultaneously by setting direct reset inputs $R_{D\,1}$ and $R_{D\,2}$ high. For use as a counter, either $R_{D\,1}$ or $R_{D\,2}$ or both set low.





DIVIDE-BY-TWELVE COUNTER

FUNCTION TABLE (Note 1)

T	R _{D1}	R _{D2}	$Q_{\mathbf{A}}$	Qв	Qc	Q _D		
×	Н	Н	L	L	L	Ļ		
1	L	Н	Count					
1	Н	L		Count				
→	L	L		Co	unt			

Note 1 ↓ : Transition from high to low

X : Irrelevant

Count number	Q_{A}	QВ	Q _C	Q _D
0	L	L	, L	L
1	Н	L	L	L
2	L	Н	L,	L
3	Н	H	L	L
4	L	٦	Н	٦
5	H	L	Н	L
6	L	L	L	I
7	I	Ĺ	L	Н
8	L	I	L	н
9	Ι	Н	L	Н
10	L	L	Н	Ŧ
11	Н	L	I	Н
(1) 1/ 11 1 0	.=-			

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS

 $(T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5	V
VI		Inputs R _{D1} , R _{D2}	-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDTIONS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter			Unit		
Symbol	, aranie	orei .	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mΑ
IOL	Low-level output current	V ₀ ∟≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parame		Test co			Limits		112.
Symbol	rarame	ter	l est co	naitions	Min	Тур *	Max	Unit
ViH	High-level input voltage		,		2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18mA			-1.5	V
Vон	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		· V
	Low lavel output voltage			V _{CC} =4.75V I _{OL} =4mA (Note 2)		0.25	0.4	V
VoL	Low-level output voltage		V ₁ =0.8V, V ₁ =2V I _{OL} =8mA (Note 2)			0.35	0.5	V
		R _{D1} , R _{D2}					20	
		T ₁	T ₁ V _{CC} =5.25V, V _I =2.7V	7V			40	μA
.1	High-level input current	T ₂	7.				80	
TaH	r light-level input current	T ₁	V _{CC} =5.25V, V _I =5.	EV			0.2	mA
		T ₂	VCC-5.23V, VI=5.				0.4	IIIA.
		R _{D1} , R _{D2}	V _{CC} =5.25V, V _I =10	V			0.1	mA
		R _{D1} , R _{D2}					-0.4	
LiL	Low-level input current	T ₁	$V_{CC} = 5.25V, V_{I} = 0.$	4V .			-2.4	mA
		T ₂					-3.2	
los	Short-circuit output current (Note 3)	V _{CC} =5.25V, V _O =0	V	-20		— 100	mA
loc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC} = 5V; Ta = 25°C.

Note 2: Testing of output Q_A should be conducted with input $\overline{T_2}$ connected to output Q_A ,

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

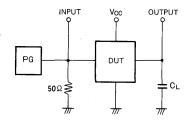
Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V from 4.5V.

DIVIDE-BY-TWELVE COUNTER

SWITCHING CHARACTERISTICS ($V_{CO}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

C	Parameter	Test conditions	Limits			Unit
Symbol	Farameter	lest conditions	Min	Тур	Max	-Unit
f _{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		32	- 80		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			7	16	ns
tpHL	propagation fime, from input $\overline{T_1}$ to output Q_A			8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			25	48	ns
tehl	propagation time, from input $\overline{T_1}$ to output Q_D			25	50	ns
tpLH	Low-to-high-level, high-to-low-level output			7	16	ns
tpHL	propagation time, from input $\overline{T_2}$ to output Q_B			8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L =15pF (Note 4)		8	16	ns
tpHL	propagation fime, from input $\overline{T_2}$ to output Q_C			10	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			15	. 32	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D			15	35	ns
t _{PHL}	High-to-low-level output propagation time, from inputs R _{D1} , R _{D2} to outputs Q _A , Q _B , Q _C , Q _D			17	40	ns

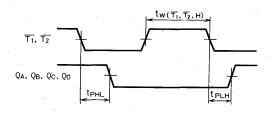
Note 4: Measurement circuit

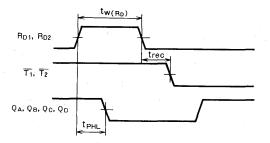


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MNz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$.
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	i arameter	rest conditions	Min	Тур	Max	Unit
t _W (₹iH)	Clock input T ₁ high pulse width	·	15	6		ns
t _W (₹ ₂ H)	Clock input T ₂ high pulse width	•	30	17		ns
t _{W(RD)}	Direct reset R _{D1} , R _{D2} pulse width		15	5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(R _D)	Recovery time R _{D1} , R _{D2} to \overline{T}_1 , \overline{T}_2		25	8		ns





MITSUBISHI LSTTLS M74LS93P

4-BIT BINARY COUNTER

DESCRIPTION

The M74LS93P is a semiconductor integrated circuit containing an asynchronous 4-bit binary (hexadecimal) counter function with direct reset inputs.

FEATURES

- Direct reset inputs provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max} = 60MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

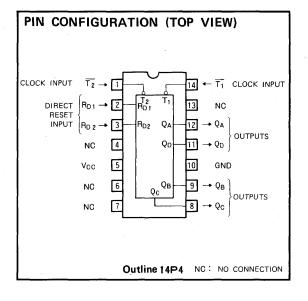
General purpose, for use in industrial and consumer equipment.

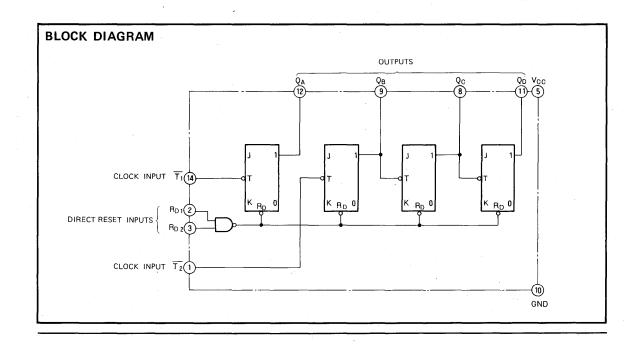
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A , Q_B , Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and octal counters can be reset simultaneously by setting direct reset inputs R_{D1} or R_{D2} , high. For use as a counter, either R_{D1} or R_{D2} , or both, is set low.

Also provided is the M74LS293P with the same functions and electrical characteristics. Its GND positioning at pin 7 enables easy mounting.





4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

T	R _{D1}	R _{D2}	QΑ	Qв	Qc	QD
Х	Н	Н	L .	L	Ĺ	L
1	L	Н		Cou	ınt	
↓	н	L		Cou	ınt	
↓	L	L	***************************************	Cou	ınt	

Note 1 \downarrow : Transition from high to low

X : Irrelevant

Count number	QΑ	Qв	Qc	Q_{D}
0	L.	L	L	L
. 1	Н	L	L "	L
. 2	L	н	L	L
3	Н	Н	L	الما
4	L	L	н	L
5	Н	L	н	L
6	L	н	н	· L
7	Н	н	н	L
8	· L	L	L	н
9	Н	L	L	Н
10	L	Н	L	Н
11"	Н	Н	L	Н
12	L	L	Н	н
13	Н	L	Н	Н
14	L	Н	н	Н
15	Н	Н	Н	Н
		.= .		

Valid when $Q_{\underline{A}}$ and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
		Inputs $\overline{\Gamma_1}$, $\overline{\Gamma_2}$	-0.5~+5.5	
Vı	Input voltage	Inputs RD1, RD2	-0.5~+15	7 °
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		−20 ~+75	°C
Tstg	Storage temperature range		- 65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	rarame	rter	Min	Тур	Max 5.25 -400	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
la.	Low-level output current	V _{OL} ≤0.4V	0		4	mA	
OL	Edwieror dathat current	V _{OL} ≤0.5V	0		8	mA	

4-BIT BINARY COUNTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramete	Parameter		tions		Limits		Unit
Symbol	raramete	ſ	Test condi	LIONS	Min	Typ ∗	Max	Onit
VIH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage	Low-level input voltage					0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA	-		-1.5	V
.,	OH High-level output voltage		V _{CC} =4.75V, V _I =0.8	3V	2.7			v
VOH			$V_1 = 2V$, $I_{OH} = -400 \mu$	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		V
	VoL Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA (Note 2)		0.25	0.4	V
VOL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA(Note 2)		0.35	0.5	V
	R _{D1} , R _{D2}		V _{CC} =5.25V				20	
	High-level input current	T ₁ , T ₂	V _I =2.7V	·			40	μΑ
ΙН	Trigit-level input current	T ₁ , T ₂	V _{CC} =5.25V, V _I =5.5	īV			0.2	mA
		RD1, RD2	V _{CC} =5.25V, V _I =10V	v .			0.1	mA
-		R _{D1} , R _{D2}	Va E 25V	***			-0.4	
I _{IE}	Low-level input current	T ₁	V _{CC} =5.25V V _I =0.4V				-2.4	mΑ
		T ₂					-1.6	
los	Short-circuit output current (N	Short-circuit output current (Note 3)		V	-20		— 100	mA
lcc	Supply current	Supply current				9	15	mΑ

 $[\]star$: All typical values are at V_{CC} = 5V, Ta=25°C.

Note 2: Testing of output Q_A should be conducted with input T_2 connected to output Q_A

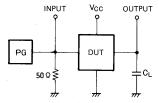
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V from 4.5 V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	T		Limits		Unit
Symbol	Falametel	Test conditions	Min	typ	Max	Unit
fmax	Maximum clock frequency, from input T ₁ to output Q _A		32	60		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	35		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			7	16	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_A			8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			28	70	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_B			28	70	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L = 15pF (Note 5)		7	16	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_C	OL — ISPF (Note 5)		8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			15	32	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D			15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			22	51	ns
t _{PHL}	propagation time, from input T ₁ to output Q _D			22	51	ns
t _{PHL}	High-to-low-level output propagation time, from inputs RD1, RD2 to outputs QA, QB, QC, QD	·		17	40	ns

Note 5: Measurement circuit

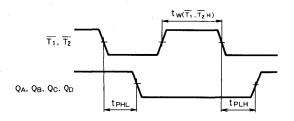


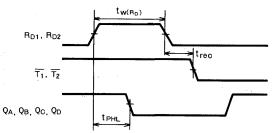
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MNz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

4-BIT BINARY COUNTER

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0	D	To a constitution		11.5		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width		15	6		ns
t _{w(T₂H)}	Clock input T ₂ high pulse width		30	15		ns
tw(RD)	Direct reset RD1, RD 2 Pulse width		15	5.		ns
tr	Clock pulse rise time.			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(RD)	Recovery time R_{D1} , R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns





MITSUBISHI LSTTLS M74LS95BP

4-BIT PARALLEL-ACCESS SHIFT REGISTER

DESCRIPTION

The M74LS95BP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

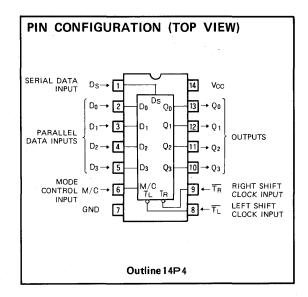
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- · Special right and left shift inputs provided
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

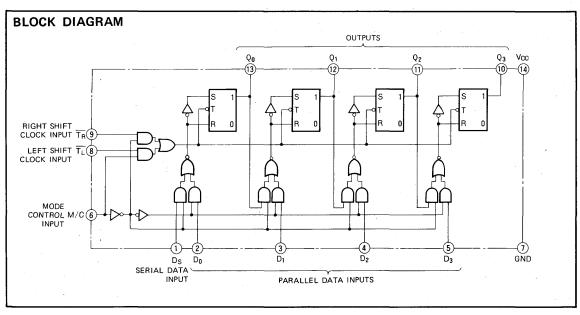
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept at low, the serial data are applied to serial data input Ds and the clock pulse is applied to right shift clock input \overline{T}_R , the serial data are shifted sequentially into outputs $Q_0 \sim Q_3$ in synchronization with the clock pulse. When M/C is kept at high, the parallel data are applied to parallel data inputs $D_0 \sim D_3$ and the 1-bit clock pulse is applied to left shift clock input \overline{T}_L , the signals $D_0{\sim}\underline{D}_3$ appear in outputs $Q_0 \sim Q_3$ respectively. When \overline{T}_R and \overline{T}_L change from high to low, the right shift or parallel data reading operation is performed. When M/C is kept in high, Q3 is connected to D_2 , Q_2 to D_1 and Q_1 and D_0 , the serial data are applied to D_3 and the clock pulse is applied to $\overline{T_L}$, the device functions as a left shift register. Care should be taken when



switching the M/C signal since the output changes in accordance with the status of $\overline{T_R}$ and $\overline{T_L}$. Refer to the function table,



4-BIT PARALLEL-ACCESS SHIFT REGISTER

FUNCTION TABLE (Note 1)

Operational mode	M/C	TR	TL	Ds	D ₀ ~D ₃	Q_0	Q ₁	Q2	Q ₃
Right shift	L	↓	Х	L	X	L	Q ₀ 0	Q ₁ 0	Q ₂ 0
right shift	. L	↓	X	Н	X	Н	Q ₀ 0	Q ₁ 0	Q ₂ 0 .
Parallel reading	Н	X		Х	D ₀ ~D ₃	D ₀	D ₁	D ₂	D ₃
	↓	L	١	Χ.	, X	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q ₃ 0
	1	٦	L	Х	Х	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q ₃ 0
. •	1	Н	L	Х	X	Q ₀ o	Q ₁ 0	Q ₂ 0	Q ₃ 0
M/C switching	1	н	٦	х	X	*	*	*	*
		Ľ	н	Х	Х	*	*	*	*
1	<u></u>	Ĺ	Н	Х	X	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q ₃ 0
	1	H.	Н	Х	X	*	*	*	*
	1	Н	, H	X	X	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q ₃ 0

Note 1. | : Transition from high to low (negative edge trigger)

↑ : Transition from low to high (positive edge trigger)

Q0: Level of Q before the indicated steady-state input conditions were established

* : Cannot be predicted

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage	:	$-0.5 \sim +7$	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D	Parameter				Unit	
Symbol	Paramet	ler	Min	Тур	Max	Ollit	
Vcc	Supply voltage	4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
		V _{OL} ≤0.4V	V _{OL} ≤0.4V	0		4	mΑ
IOL L	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75$ °C, unless otherwise noted)

Symbol	Parameter		Tank and die		Limits			Unit
Symbol	rarame	t di di lietei		Test conditions		Тур*	Max	Onit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage			*****			0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	I8mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-400μ		2.7	3.4		٧
V _{OL}	Low-level output voltage		$V_{CC} = 4.75V$ $V_{I} = 0.8V, V_{I} = 2V$	I _{OL} =4mA		0.25	0.4	V
		M/C					20	
	Link to at in mot a	M/C	$V_{CC}=5.25V, V_{I}=2.7V$		-		40	μA
ин .	High-level input current	M/C	Vcc=5.25V, Vi=10V				0.1	
		M/C	VCC - 5.25V, VI= 10V				0.2	m A
I _{IL}	Low-level input current	M/C	V _{CC} =5.25V, V _I =0.4	.,			-0.4	mΑ
III.	M/C V _{CC} =5.25V, V _I =0.4V		ν .			-0.8	ША	
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		- 20		100	mA
loc	Supply current		V _{CC} =5.25V (Note 3)			13	21	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time,

Note 3: I_{CC} is measured with $D_0 \sim D_3$ at 0V, D_S open and M/C at 4.5V after $\overline{T_R}$ and $\overline{T_L}$ have been set from 3V to 0V.

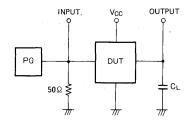


4-BIT PARALLEL-ACCESS SHIFT REGISTER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

		Task	Limits			Unit
Symbol	Parameter	Test conditions	Min.	Тур	Max	Unit
f _{max}	Maximum clock frequency		25	50		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		14	27	ns
tphL	time, from inputs $\overline{T_R}$, $\overline{T_L}$ to outputs $Q_0 \sim Q_3$			14	32	ns

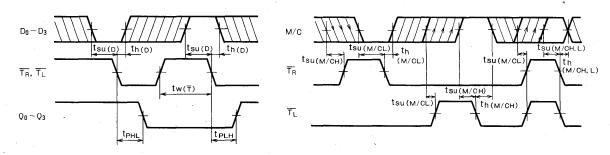
Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P.P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

	B	Test conditions		Limits		
Symbol	Parameter	l est conditions	Min	Тур	Max	Unit
t _{w(T)}	Clock input Thigh pulse width		25	8		ns
tf	Clock input T falltime			350	100	ns .
t _{SU(D)}	Setup time D to T		20	0		ns
t _{SU(M/CL)}	Setup time M/C low to T		20	14		ns
tsu(M/CH)	Setup time M/C high to T		20	0		ns
th(D)	Dhold time to T	The second secon	10	2		ns
th (M/CL)	Hold time M/C low to T		. 10	2		ns
th (M/CH)	Hold time M/C high to T		10	-13		ns



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

The arrows on the shaded areas indicate the direction for when the input is permitted to change.

MITSUBISHI LSTTLS M74LS96P

5-BIT SHIFT REGISTER

DESCRIPTION

The M74LS96P is a semiconductor integrated circuit containing a 5-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

- · Positive edge-triggering
- Right shift function
- Asynchronous parallel input provided
- Direct reset input provided
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

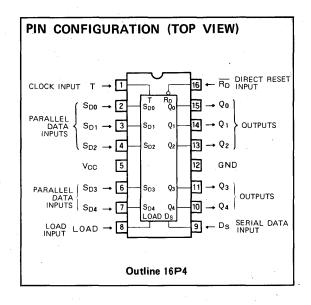
FUNCTIONAL DESCRIPTION

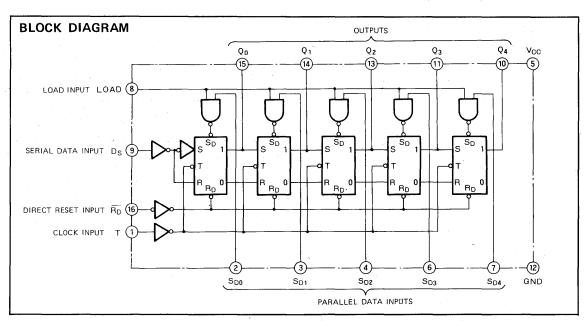
This 5-bit shift register is composed with 4 R-S-T flip-flops and it functions as a serial/parallel inpput-serial/parallel output shift register.

For use as a serial input-serial/parallel output shift register, the load input LOAD or parallel data inputs $S_{D0} \sim S_{D4}$ are kept in high and the data are applied to the serial data input D_S . When a clock pulse is applied to clock input T with D_S in high, the high signal is shifted sequentially to Q_0 , Q_1 ... Q_4 . Shifting is performed when T changes from low to high. When the serial data are applied to $D_{S0} \sim S_{D4}$ and LOAD is set high, the $S_{D0} \sim S_{D4}$ signals appear in $Q_0 \sim Q_4$ respectively irrespective of T.

When direct reset input $\overline{R_D}$ is set low, $Q_0 \sim Q_4$ are set low if LOAD is low irrespective of the other input signals.

When LOAD is high, parallel reading takes precedence, and the $S_{D\,0}{\sim}S_{D\,4}$ signals appear in $Q_0{\sim}Q_4$.





FUNCTION TABLE (Note 1)

SERIAL INPUT-PARALLEL OUTPUT

	tn	t _{n+1}	tn+2	tn+3	tn + 4	tn + 5	tn+6
Ds	١	Н	L	Н	L	Н	L
, Qo	*	L	н	L	Н	L	Н
Q ₁	*	*	L	Н	L	н	L
Q ₂	*	*	*	L	Н	L	Н
Q ₃	*	*	*	*	L	Н	L
Q ₄	*	*	*	*	*	L	H.

Note 1: For use as a serial input-parallel output, LOAD, S_{D0} , S_{D1} , S_{D2} , S_{D3} and S_{D4} are all kept at low and \overline{RD} is kept at high.

tn: Bit time prior to clock

tn+1: Bit time after application of 1 clock pulse tn+6: Bit time after application of 6 clock pulses

* : Cannot be predicted

PARALLEL INPUT-PARALLEL OUTPUT

LOAD	S _{D(N)}	ŖD	Q(N)
L	L	٦	L
· L	L	Н	Q٥
' L	Н	L	L
L	Н	Н	Q ⁰
н	L'	L	L
Н	L.	н	Q ⁰
, н	н	L	Н
Н	Н	Н	н

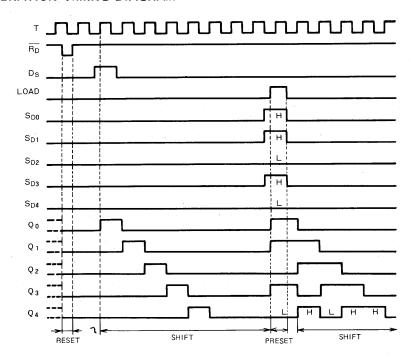
Note 2: For use as a parallel input-parallel output, $\overline{R_D}$ is first set low and kept at high. The parallel input data are input into $S_{D0} \sim S_{D4}$.

The data are read when LOAD is high and they simultaneously appear in the outputs. $\overline{R_D}$ is usually kept at high and LOAD at low.

The "N" in $S_{D(N)}$ refers to 0, 1, 2, 3, 4.

 $\mathbf{Q}^{\mathbf{0}}$ is the level of Q before the indicated steady-state input conditions were established

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
. Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
V _O	Output voltage	High-level output	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature		-65~+150	င

RECOMMENDED OPERATING CONDITIONS (Ta = $-20 \sim +75 \, \circ$, unless otherwise noted)

Symbol	0			Limits				
Symbol	Paramete	raiametei		Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Lon.	High-level output current	V _{OH} ≧2.7V	0		- 400	μΑ		
10.	I OL Low-level output current	V _{OL} ≦0.4V	0		4	mA ·		
I TOL		V _{OL} ≦0.5V	. 0		8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Parameter		Test condit		Limits			Unit
Symbol	i di arrietei		l est condit	Olis	. Min	Typ ∗	Max	Unit
VIH	High-level input voltage		, .		2			٧
VIL	Low-level input voltage						0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	BmA			-1.5	V
Voн	High-level output voltage		V _{CC} =4.75V, V _I =0.8V	,	2.7	2.4		V
∨он	Thigh-level output voltage	-	$V_1 = 2V, I_{OH} = -400 \mu A$	\	2.1	3.4		V
VoL	Voi Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		LOAD	V _{CC} =5.25V				100	
Local	High-level input current	Other inputs	V _I = 2.7V				20	μΑ
Ιн	High-level input current	LOAD	V _{CC} =5.25V				0.5	
		Other inputs	V _I = 10V				0.1	mA
-1	Low-level input current	LOAD	V _{CC} =5.25V				-2.0	
'IL	THE Low-level input current		V _I = 0.4V				-0.4	mΑ
los	Short-circuit output current (Note 3)		V _{CC} =5.25V, V _O = 0 V		- 20		— 100	mA
loc	Supply current		V _{CC} =5.25V (Note 4)			12	20	mA

 $^{{\}boldsymbol *}~:~$ All typical values are at VCC=5V, Ta=25°C.

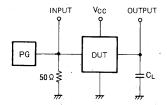
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Offic
fmax	Maximum clock frequency		25	45		MHz
t _{PLH} .	Low-to-high-level, high-to-low-level output propagation			12	40	ns
tpHL	time, from input T to outputs $Q_0 \sim Q_4$	C _= 15pF (Note 5)		12	40	ns
tpLH	Low-to-high-level output propagation time, from input $$\sf S_D, \; LOAD \; to \; outputs \; Q_0 \sim Q_4 \;$			11	35	ns
t _{PHL}	High-to-low-level output propagation time, from input $$\overline{R}_D^{}$$ to outputs $Q_0\sim Q_4$			11	35	ns

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time,

Note 4: I_{CC} is measured with $\overline{R_D}$ at 0V and all the other inputs at 4.5V.

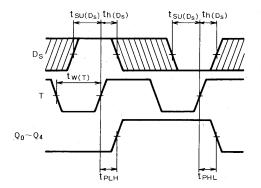
Note 5: Measurement circuit

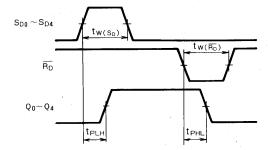


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
 - $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	rarameter	rest conditions	Min	Тур	Max	Onit
tw(T)	Clock input T pulse width		20	5		ns
tw(sD)	Parallel data input pulse width		30	5		ns
tw(₩)	Direct reset pulse width		30	5		ns
tsu(Ds)	Setup time D _S to T	· ·	30	3		ns
th(Ds)	.Hold time Ds to T		5	-1		ns





Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS107AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{\mathsf{T}}$, J and K inputs and direct reset input R_D.

FEATURES

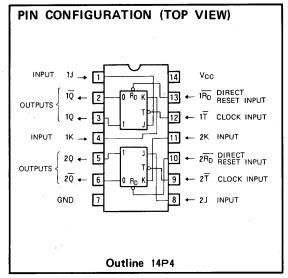
- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct reset input
- Q and Q outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals are read when \overline{T} is "H". When \overline{T} changes from "H" to "L", Q and \overline{Q} transit with the J and K signals to the states described in the function table. By setting \overline{R}_D in "L" state, Q and \overline{Q} become "L" and "H", respectively, irrespective of the states of the other input signals. For use as a J-K flio-flop, keep \overline{R}_D in the "H" state. M74LS107AP is the same as M74LS73AP except for pin configuration.



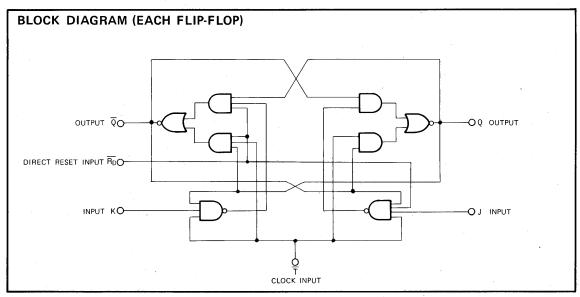
FUNCTION TABLE (Note 1)

Ŧ	RD	J	K	Q	Q	
X	L	Х	Х	L	H	
	н	Н	Н	Toggle		
1	H-	L	Н	· L	Н.	
1	н	н	L,	H ·	L	
1 ·	Н	L '	L	Q ⁰	Q0	
Н	Н	×	Х	Q ⁰	\overline{Q}^0	

Note 1: \downarrow : transition from high to low-level

- X: irrelevant
- Q0: level of Q before the indicated steady-state input conditions were established.
- $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established.

Toggle: complement of previous state with $\ensuremath{\downarrow}$ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		-65-+150	° ℃

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Parameter			Unit		
			Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μА
	I OL Low-level output current	V _{OL} ≤0.4V	0		4	mΑ
OL		V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0			-	-		Limits		
Symbol	Paramet	er	Test cond	itions	Min	Тур*	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage					,	0.8	V
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			- 1.5	V
Voh	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8$ $V_{I} = 2V, l_{OH} = -400$		2.7	3.4		٧
	VOL Low-level output current		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧
VOL Low-level output current	Low-level output current		$V_i = 0.8 V, V_i = 2 V$	fol = 8mA		0.35	0.5	V
		J, K	V - F 05V				20	
		RD	V _{CC} =5.25V				60	μA
Local	High-level input current	T	V _I =2.7V				80	
I _{IH}	High-lever input current	J, K	\/ F 25\/				0.1	
		R _D	$V_{CC} = 5.25V$ $V_{I} = 10V$. 0.3	mΑ
		Ŧ,		V ₁ = 10 V			0.4	
	1 1 1	J, K	V _{CC} =5.25V				-0.4	
IIL	Low-level input current	R _D T	V _I =0.4V				-0.8	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	. – 20		- 100	mA
loc	Supply current		V _{CC} =5.25V (Note 3)			4	6	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Cumbal	Symbol Parameter	Tank and divine	Limits			Unit
Symbol	rarameter	Test conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		30	45		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation			8	20	ns
tpHL	time, from input \overline{T} to output Q , \overline{Q}	C _L = 15pF (Note 4)		6	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	•		10	20	ns
t _{PHL}	time, from input $\overline{R_D}$ to output Q, \overline{Q}			7	20	ns

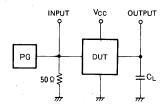
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 2: I_{CC} is measured with Q and \overline{Q} outputs high in turn. At the time of measurement, \overline{T} input is grounded.

M74LS107AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

Note 4: Measurement circuit

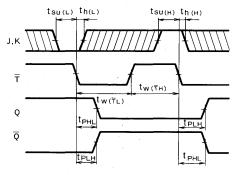


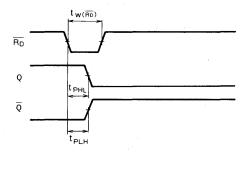
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, $V_P=3V_{P,P}, Z_Q=50\Omega$
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5 V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Зупівої	Parameter	l est conditions	Min	Тур	Max	Oint
t _w (∓н)	Clock input T high pulse width		20	12 .		ns
tw(RD)	Direct reset input RD pulse width	<u>'</u>	25	4		ns
tr	Clock rise time			650	100	ns
tf	Clock pulse fall time			900	100	ns
t _{su(H)}	Setup time high J, K to T		20	9		ns
t _{su(L)}	Setup time low J, K to T		20	10		ns
t _{h(H)}	Hold time high J, K to T		0	- 8		ns
t _{h(L)}	Hold time low J, K to T		0	- 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

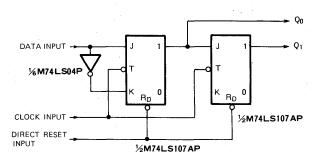


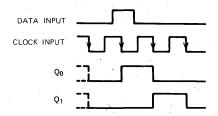


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

2bit shift register





Note 6: Output switching characteristics may not satisfy the ratings if the clock signal is applied without observing the set-up time.

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS109AP is a semiconductor integrated circuit containing 2 J- \overline{K} positive edge-triggered flip-flop circuits with discrete terminals for clock input T, inputs J and \overline{K} , and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Positive edge-triggering
- Each flip-flop can be used independently
- Direct set and reset inputs
- J and K inputs
- Q and Q outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

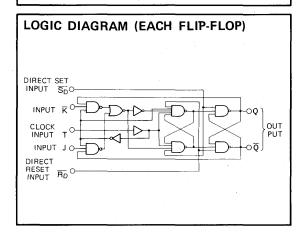
General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

When T changes from low to high, the J and \overline{K} signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = \overline{Q} = high. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high. By connecting J and \overline{K} , this IC can be used as a D-type flip-flop.

FUNCTION TABLE (Note 1)

SD	RD	T	j	ĸ	Q	Q	
L	Н	X	Х	Х	Н	L	
Н	L	X	×	Х	L	Ι	
. L	L	X	Х	Х	н*	н*	
Н	Н	L	X	Х	Q ⁰	Q ⁰	
Н	Н	1	L	L	L	H .	
н	Н	1	Н	L	Toggle		
Н	н	1	L	н	Q ⁰	Q ⁰	
Н	Н	1	Н	н	H	L	



- Note 1 1: Transition from low to high-level (positive edge trigger)
 - Q^0 : Level of Q before the indicated steady-state input conditions were established.
 - $\overline{Q^0}$: Level of \overline{Q} before the indicated steady-state input conditions were established. Toggle: complement of previous state with \uparrow transition of output
 - X : Irrelevant
 - *: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D} \text{ are set high, the status of } Q \text{ and } \overline{Q} \text{ cannot be anticipated.}$

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+5.5	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \, \text{C}$, unless otherwise noted)

				Limits				
Symbol	Paramet	ter	Min	Тур	Max 5.25 400	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ		
	Low-level output current	V _{OL} ≤0.4V	0		4	mA		
1 OL	Low-level output current	V _{OL} ≦0.5V	0		8	mA		

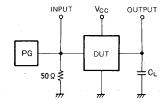
ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter		Tost conditi	Test conditions		Limits		
Symbol			lest conditi	ions	Min	Typ ∗	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} = -18mA				-1.5	V
Vон	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
	, , ,		$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	٧
		J, K, T	Voc = 5.25V, Vi = 2.7V	,			20	μА
Iн	High-level input current	SD, RD	VCC = 3.23V, VI = 2.7	v			40	μд
чн	Trigit lever input current	J, K, T	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	,			0.1	^
	S _D , R _D		V _{CC} =5.25V, V _I =10V				0.2	mĄ
lic	Low-level input current	J, K, T	V _{CC} =5.25V, V _I =0.4V				-0.4	4
III.	Low-level input current	S _D , R _D					-0.8	mΑ
los	Short-circuit output current (No	te 2)	V _{CC} = 5.25 V, V _O = 0 V		-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V, (Note 3)			4	8	mΑ

 $[\]pmb{*}$: All typical values are at $V_{CC}{=}$ 5 V, $\,Ta\,{=}\,25\,^{\circ}\!C$

Cumbal	Symbol Parameter .	Test conditions		Unit		
Syllibol		rest conditions	Min	Тур	Max	· Oilit
fmax	Maximum clock frequency		25	45		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 4)		10	25	ns
t PHL	time, from T to Q, Q			12	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	25	ns
t PHL	time, from $\overline{S_D}$, $\overline{R_D}$ to Q , \overline{Q}			10	40	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$. (2) C_L includes probe and jig capacitance.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

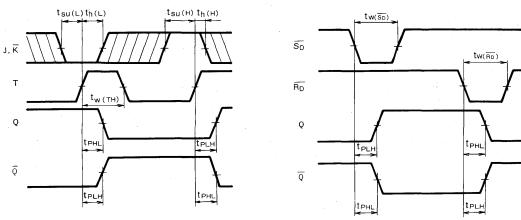
Note 3: The supply current should be measured with Q and \overline{Q} alternately set high and with T set low during actual measurement.

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

TIMING REQUIREMENTS (VCC= 5 V, Ta=25°C, unless otherwise noted)

Symbol	D	Total and Park		11.5		
	Parameter	Test conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		25	11		ns
tw(SD, RD)	Direct set, reset pulse width		25	4		ns
t _{su(H)}	Setup time high to T		20	19		ns
t _{su(∟)}	Setup time low to T		20	7		ns
t _{h(H)}	Hold time high to T		5	2		ns
t _{h(L)}	Hold time low to T		5	-16		ns

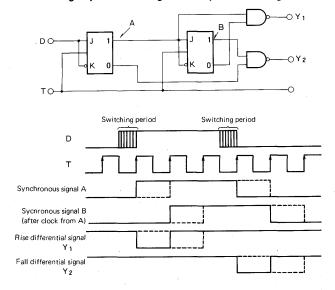
TIMING DIAGRAM (Reference level = 1.3V)



Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Typical circuit for converting asynchronous signal into synchronous signal and rise/fall differential circuit



Note 5: The waveforms indicated by the dotted lines apply when reading with the next clock without observing the set-up time to T.

M74LS112AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS112AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , J and K inputs and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

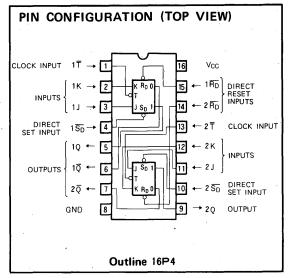
- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and Q outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals of are read, while \overline{T} is high. When \overline{T} changes from high to low, the signals of J and K immediately before the change appear in outputs Q and \overline{Q} in accordance with the function table. By using \overline{S}_D and \overline{R}_D , this IC can be made into an direct R-S flip-flop. When both \overline{S}_D and \overline{R}_D are low, Q = \overline{Q} = high. However, when both of them changed to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, keep \overline{S}_D and \overline{R}_D high. M74LS112AP is the same as M74LS76AP except for pin configuration.

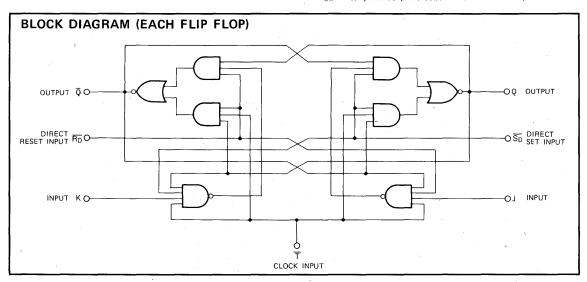


FUNCTION TABLE (Note 1)

T	SD	R _D	J	К	Q	Q	
X	L	Н	X	×	Н	L	
Х	Н	L	Х	×	L	Н	
X	L	L	Х	Х	Н*	. H*	
1	Н	Н	н	Н	Toggle		
1	Н	. н	L	н	L	н	
1	н	н	н	L	н	L	
1	н	Н	L	L	Q ⁰	Q̄0	
Н	Н	Н	X	Х	Q ⁰	Q ⁰	

Note 1: \downarrow : transition from high to low-level

- X : irrelevant
- *: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D} \text{ are set high, the status of } Q \text{ and } \overline{Q} \text{ cannot be anticipated.}$
- Q^0 : level of Q before the indicated steady-state input conditions were established. $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established.
- Toggle: complement of previous state with ↓ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5 ~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65 - + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	•		Limits	11-14	
Symbol	rarameter .		Min .	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА
		· V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _O L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		T	Took and dalars		Limits		
Зуптьог	Paramete	er	Test conditions		Min	Тур*	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	. V
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
V _{OH}	High-level output voltage	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8V$ $V_{I} = 2V, I_{OH} = -400 \mu A$		3.4		V
	Voi Low-level output voltage		V _{CC} =4.75V	$I_{OL} = 4 \text{ mA}$		0.25	0.4	·V
VOL		I _{OL} = 8mA		0.35	0.5	V		
		J,K					20	
		SD, RD	V _{CC} =5.25V, V ₁ =2.7V				60	μA
		Ŧ					. 80	
I _H	High-level input current	J,K					0.1	mA
		SD, RD	V _{CC} =5.25V, V _I =10V	/			0.3	
		Ŧ					0.4	
		J,K					-0.4	
fiL	Low-level input current	SD. RD T	V _{CC} =5.25V, V _I =0.4	IV			-0.8	mΑ
los	Short-circuit output current	(Note 3)	V _{CC} =5.25V, V _O =0V		- 20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 4)			4	6	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: Sp and Rp should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly, and not more than one output should be shorted at a time.

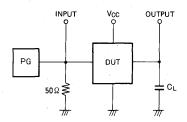
Note 4: I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, \overline{T} input is grounded.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	, alamete	rest conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock frequency		30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	20	ns
tphL	time from input T to output Q, Q	C _L =15pF (Note 5)		7	20	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			7	20	ns
tpHL	tent time, from input SD, RD to output Q, Q			7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

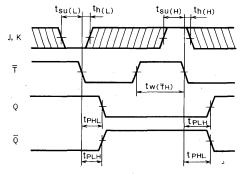
Note 4: Measurement circuit



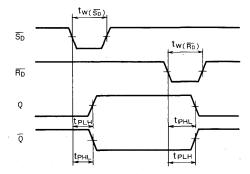
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P =3 V_{P-P} , Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Unit
t _W (₹H)	Clock input Thigh pulse width		20	12		ns
$t_{W(\overline{S_D},\overline{R_D})}$	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width	1	25	4		ns
tr	Clock rise time] .		650	100	ns
tf	Clock pulse fall time	1		900	100	ns
t _{SU(H)}	Setup time high J, K to T	1	20	12		ns
t _{SU(L)}	Setup time low J, K to T		20	12	-	ns
t _{h(H)}	Hold time high J, K to \overline{T}	1	0	- 10		ns
t _{h(L)}	Hold time low J, K to T	1	0	- 6		ns



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.



MITSUBISHI LSTTLs M74LS113A

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

DESCRIPTION

The M74LS113AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input \overline{T} , inputs J and K and direct set input SD.

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct set input
- Q and \overline{Q} outputs
- Wide operating temperature range (T_a = −20~+75°C)

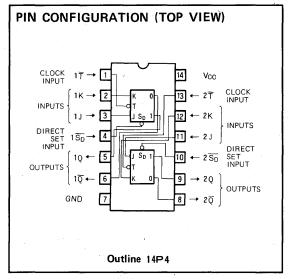
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when T changes from high to low, the J and K signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By setting $\overline{S_D}$ low, Q and $\overline{\mathbf{Q}}$ are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, SD must be kept high.

The only difference in functions from M74LS112AP is that this IC has no RD input.

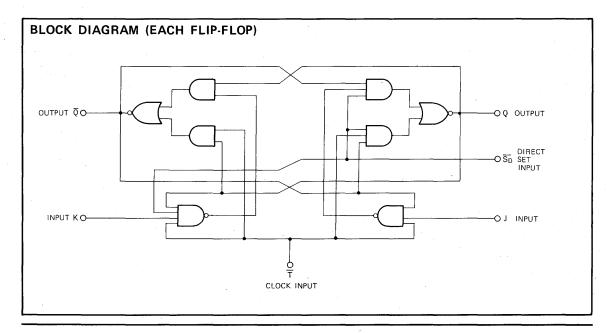


FUNCTION TABLE (Note 1)

Ŧ	SD	J	К	Ó	Q
×	L	Х	Х	Н	L
1	н	н	н	Tog	ggle
↓	Ŧ	L	н	L	Н
→	Н	Н	L	н	L
Ţ	н	L	L	Q٥	Q0
Н	Н	X	. X	Q ⁰	Q0

- \downarrow : Transition from high to low-level (negative edge trigger)

 - OD: level of Q before the indicated steady-state input conditions were established.
 - $\frac{\nabla}{\nabla}^0$: level of $\overline{\Omega}$ before the indicated steady-state input conditions were established. Toggle: complement of previous state with \downarrow transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

C 1	6			Unit		
Symbol	Paramet	er	Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V _{0L} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	· ·	Test condi	elama .		Limits		Unit
Symbol	rarante	tei	rest contai	tions	Min	Typ *	Max	
VIH	High-level input voltage				2			· V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18 mA			-1.5	- V
Voн	High-level output voltage	High-level output voltage		$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, I_{OH}=-400 \mu A$		3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V	$I_{OL} = 4 mA$		0.25	0.4	V
VOL	Low-level output voltage		$V_1 = 0.8V \cdot V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
		J.K				20		
	-	SD	V _{CC} =5.25V, V _I =2.7V				60	μA
1	High-level input current	Ŧ					80	
I _{IH}	r rigit-level input current	J,K					0.1	mA
		SD	V _{CC} =5.25V, V _I =10	V			0.3	
	,	Ŧ					0.4	
	I am I am I in a man a man a	J,K					-0.4	
hι	Low-level input current	S _D T	V _{CC} =5.25V, V _I =0.4V				-0.8	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		– 100	m A
loc	Supply current		V _{CC} =5.25V (Note 3)			4	6	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

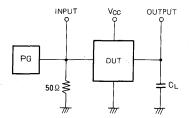
Note 3: Supply current measurements should be done with Q and \overline{Q} set alternately high and \overline{T} should be set low during actual measurement.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

0	D	Test conditions		Limits			Unit	
Symbol	Parameter	Test conditions			Min	Тур	Max	Oiiit
f _{max}	Maximum clock frequency				30	45		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation					8	20	ns
t _{PHL}	time, from T to Q, Q	C _L =15pF {Note 4}				7	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(110164)				8	20	ns
t _{PHL}	time, from $\overline{S_D}$ to \overline{Q}					7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

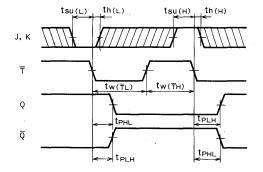
Note 4: Measurement circuit

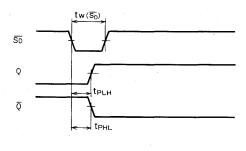


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, v_P = 3 v_{P-P} , z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{OC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit	
tw(₹H)	Clock input T high pulse width		20	13		ns	
tw(sD)	Direct set pulse width		25	10		ns	
tr	Clock rise time			650	100	ns	
tf	Clock fall time			900	100	ns	
t _{SU(H)}	Setup time high J , K to T		20	9		ns	
t _{SU(L)}	Setup time low J , K to T		20	12		ns	
t _{h (H)}	Hold time high J.K to T		0	-10		ns	
t _{h(L)}	Hold time low J, K to T		0	-5		ns	





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance,

MITSUBISHI LSTTLS M74LS114AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET. AND COMMON CLOCK

DESCRIPTION

The M74LS114AP is a semiconductor integrated circuit containing 2 J-K flip-flop circuits with common terminals for clock input T and direct reset input $\overline{R_D}$ and discrete terminals for inputs J and K and direct set inputs $\overline{S_D}$.

FEATURES

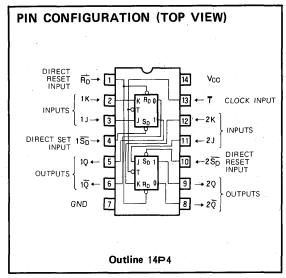
- Negative edge-triggering
- Common clock input and direct reset input
- Discrete direct set input
- Q and Q outputs
- Wide operating temperature range ($T_a = -20 \sim +75$ °C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While \overline{T} is high, signals J and K are put in the read-in state, and when \overline{T} changes from high to low, the J and K signals immediately before the change emerge in outputs Q and \overline{Q} in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$ this IC can be made into a direct R-S clip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, $Q = \overline{Q} = \text{high}$. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

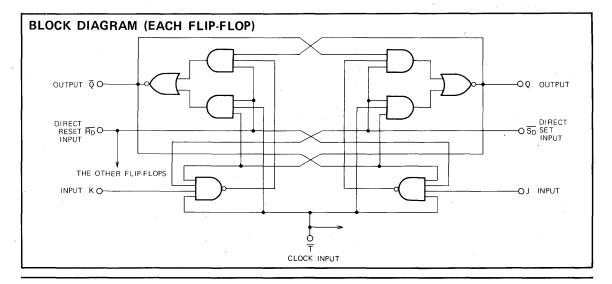


FUNCTION TABLE (Note 1)

Ŧ	SD	RD	J	K	Q	Q	
X	L	н	×	X	Н	L	
×	Н	Ĺ	X	×	L	Н	
×	, L	L	Х	×	H*	Н*	
1	н	н	н	н	Toggle		
↓	Н	Н	L	Н	L	н	
1	Н	Н	Н	٦	Н	L	
	Н	Н	L	L	Q ⁰	Q ₀	

- Note 1 \downarrow : Transition from high to low-level (negative edge trigger)
 - X : Irrelevan
 - *: $Q = \overline{Q} = \text{high when } \overline{S_D} = \overline{R_D} = \text{low and so when both } \overline{S_D} \text{ and } \overline{R_D} \text{ are set high, the status of } Q \text{ and } \overline{Q} \text{ cannot be anticipated.}$
 - Q0: Status of output before ↓ change.
 - $\overline{\mathbb{Q}^0}$: level of Q before the indicated steady-state input conditions were established.

Toggle: complement of previous state with $\+ \downarrow$ transition of outputs



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

	D	-	Limits			
Symbol	Parame ⁻	ter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		. 4	mA
loL	Low-level output current	V ₀ ∟≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test cond	tions		Limits		Unit [*]
Sylfibol	T diamet	61	rest condi	itions	Min	Тур 🛪	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage	,,,	V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		V
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL .	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	٧ ,
		J,K					20	
		SD	V _{CC} =5.25V, V _I =2.7			60		
		RD	VCC=3.23V, V =2.7V				120	μА
I _{IH}	High-level input current	Ŧ					160	
.10	, and the same of	J,K					0.1	
		SD	V _{CC} =5.25V, V _I =10V				0.3	
		RD	VGC-5.25V, VI-10V				0.6	mA
		Ť					0.8	
		J,K					-0.4	
I _{IL}	Low-level input current	SD	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	V (Note 2)			-0.8	4
'IL	pat carront	R _D T	V _{CC} =5.25V, V _I =0.4V (Note 2)				-1.6	. mA
los	Short-circuit output current (Note 3)	V _{CC} =5.25V, V ₀ =0V	7	-20		- 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 4)		1	4	6	mA

^{* :} All typical values are at V_{CC}=5V, T_a=25°C

Note 2: $\overline{S_D}$ and $\overline{R_D}$ should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: Supply current measurements should be done with Q and \overline{Q} set alternately high and \overline{T} should be set low during actual measurement.

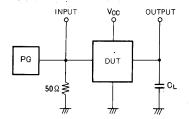
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions			Unit	
Symbol	Faraneter	rest conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		30	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	20	ns
tpHL	time, from T to Q. Q	C _L =15pF (Note 4)		. 7	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	20	ns
tphL	time, from \overline{S}_D , \overline{R}_D to Q , \overline{Q}			7	20	ns

M74LS114AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

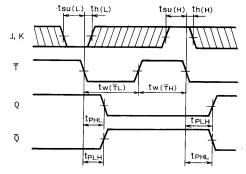
Note 4: Measurement circuit



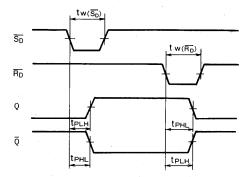
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{OC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Const. I		Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Туре	Max	Offic
tw(₹H)	Clock input T high pulse width		20	12		ns
tw(SD, RD)	Direct set, reset pulse width		25	4		ns
tr	Clock rise time			650	100	ns
t _f	Clock fall time			900	100	ns
t _{SU} (H)	Setup time high J, K to T	::	20	. 11		ns
t _{SU(L)}	Setup time low J, K to T		20	-13		ns
t.h (H)	Hold time high J, K to T		0	11		ns
t _{h(L)}	Hold time low J, K to T		0	– 6		ns



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.



DESCRIPTION

The M74LS122P is a semiconductor integrated circuit containing a retriggerable monostable multivibrator circuits with a direct reset input.

FEATURES

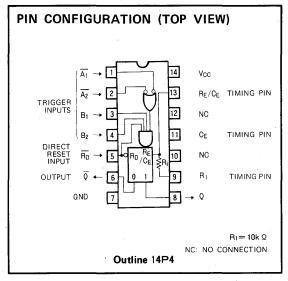
- Long pulse widths can be generated using the retriggerable function.
- Output pulses can be stopped at any time with direct reset inputs.
- A, B complementary inputs provided.
- High breakdown input voltage (V₁ ≥ 15V)
- Q and Q outputs provided
- Wide operating temperature range (T_a = -20 ~ +75°C)
- Internal timing resistance provided (R₁ = 10kΩ)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

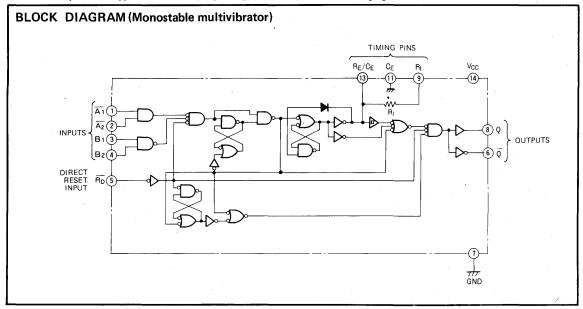
As shown in Fig. 1, the timing pins R_E/C_E and C_E are connected to the external resistance R_T and static capacitance C_T , and when a triggering pulse is applied to inputs $\overline{A_1}$, $\overline{A_2}$ and B_1 or B_2 , a positive pulse appears at output Q, with a negative pulse appearing at \overline{Q} . When the internal timing resistance is used (Fig. 2 (a)), the static capacitance C_T is connected to the C_E and R_E/C_E pins. Thus, connecting the R_1 and V_{CC} pins causes the device to function as a monostable multivibrator and eliminates the need for an external resistance. The width of the pulse (t_w) appearing at output can be controlled by the values for R_T and C_T . (When the internal timing resistance is used, the setting is made with C_T). The trigger is affected by $\overline{A_1}$ or $\overline{A_2}$ switch-



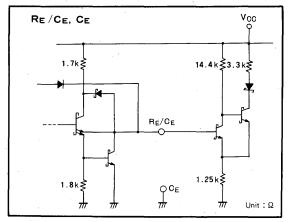
ing from high to low-level, or by B_1 or B_2 switching from low to high.

The retriggering function is used when a wide output pulse width is desired. It is obtained by triggering $\overline{A_1}$ or $\overline{A_2}$, or B_1 or B_2 prior to the pulse being fully output, thus extending its length (See Fig. 2 (b)).

Dropping the direct reset input $\overline{R_D}$ to low-level immediately causes Ω to go low-level and $\overline{\Omega}$ to be set high, regardless of the present output status. This allows the $\overline{R_D}$ signal to be used to shorten the output pulse width to the desired length (See Fig. 2 (c)). A precaution worth noting is that when $\overline{A_1}$ or $\overline{A_2}$ is low-level and $B_1=B_2=$ high, and $\overline{R_D}$ is switched from low to high-level, the trigger will be activated changing the status of Ω and $\overline{\Omega}$.



TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

RD	Ā1	A ₂	B ₁	B ₂	Q	Q
L	×	Х	X	X	L	Н
X	Н	Н	Х	·×	L	I
Х	×	×	L	X	L	Τ
X	Х	X	Χ .	L	L	Η
Н	L	×	1	н	7	
н	L	X	Н	1		7
Н	X	L	1	н .	7	7
Н	Х	L	Н	1	7	Ţ
. н	Н	. 1	Н	н	7	7
Н	↓	1	н	н	7	7
Н	1	Н	Н	н .	Ţ	L
1	L	×	Н	Н	Л	7
1	Х	L	Н	Н	J.L.	7

Note 1, 1: Transition from low to high (positive edge trigger)

 \downarrow : Transition from high to low (negative edge trigger)

☐: Positive-going one-shot trigger

☐: Negative-going one-shot trigger

X : Irrelevant

OPERATIONAL DESCRIPTION

1. Using the timing pins

Figure 1 shows the timing pins R_E/C_E and C_E connected to the external resistance R_T and static capacitance C_T respectively. An alternate method to connecting R_T is to connect the R_I and V_{CC} Pins together. When a electrolytic capacitor is used as C_T , connect R_E/C_E to the positive (+) side and C_E to the negative (-) side. In this case, the device functions as a TTL IC, and eliminates the requirement for a switching diode. Where noise causes operational problems, connect the C_E pin to GND (located near the 7 pin) as shown by the dashed line in the diagram.

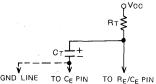


Fig. 1 Connecting External Resistance R_T and Static Capacitance C_T to Timing Pins R_F/C_F and C_F

2. Output Pulse Width tw

Output pulse width t_w is set by the values of R_T and C_T as shown below. When R_1 is used, R_T should equal $10k\Omega.$

2-1. When $C_T > 1000 pF$, $t_w = K \cdot R_T \cdot C_T \cdot (1 \pm 0.1) (ns)$. For the value for K, also refer to Typical Characteristics, $K - C_T$ characteristics. (The value for R_T does not affect K.)

Units for R_T and C_T are $k\Omega$ and pF respectively.

2-2. When C_T ≤ 1000pF, refer to the output pulse width vs. C_T, R_T shown in the Typical Characteristics section in back of this specification sheet.

3. Controlling Output Pulse Width

The width of the output pulse can be controlled using three methods, based on the presence or absence of the trigger signal and \overline{R}_D signal.

3-1. Used as conventional device

Figure 2(a) shows the device used in the normal monostable multivibrator mode. Here, output pulse width $t_{\rm w}$ is set using the equations and diagram shown in the above section.

 Extending the width of the output pulse by retriggering

Figure 2(b) shows that the output pulse can be extended to any width desired by triggering again before the pulse is fully output.

3-3. Shortening the width of the output pulse by signal $\overline{R_D}$

Figure 2(c) shows that the \overline{R}_D signal can be used to terminate the output pulse initiated by the trigger. The output pulse can be shortened to any width desired.

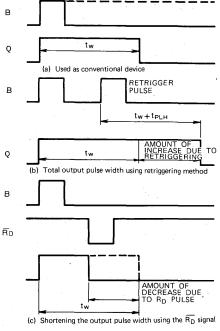


Fig. 2 Output Pulse Width Control



4. Precautions

- 4-1. The retriggering pulse should follow the trigger by $0.22C_T$ (ns), where the unit for C_T is picofarads. During this interval, the retriggering pulse will be ineffective.
- 4-2. The wiring used to connect the external C_T and R_T should be shielded from noise, and be as short as possible (less than 3cm) to minimize line capacitance and noise-induced errors.
- 4-3. Use a capacitor with good high-frequency characteristics and a value of 0.01 to $0.1\mu F$ to connect V_{CC} and GND.
- 4-4. Note that an output pulse will be produced when the power to the device is turned on.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	, °C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

C				Limits			
Symbol	Parameter		Min .	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Юн	High-level output current	VoH≧2.7V	0		-400	μΑ	
la.	Low-level output current	VoL≦0.4V	0		4	mΑ	
loL	Low-level output current	VoL≦0.5V	0		8	. mA	
R _T	External timing resistance		5		260	kΩ	
Ст	External timing capacitance			No limits			
CR	R _E /C _E pin line capacitance				50	pF	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

	_			Limits		
Symbol	Parameter	ter Test conditions		Typ *	Max	Unit
- VIH	High-level input voltage	-	2			V
VIL	Low-level input voltage				0.8	V
VIC	Input clamp voltage	Vcc=4.75V, lic=-18mA			-1.5	٧
Vон	High-level output voltage	V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} =-400μA	2.7	3.5	,	V
VoL	Low-level output voltage	Voc=4.75V		0.25	0.4	V ·
		V _{CC} =5.25V, V _I =2.7V			20	μА
ин	High-level input current	Vcc=5.25V, Vi=10V			0.1	mΑ
hL.	Low-level input current	Vcc=5.25V, Vi=0.4V			-0.4	mA
los	Short-circuit output current	Vcc=5.25V, Vo=0V	-20		- 100	mΑ
loc	Supply current	Vcc=5.25V (Note 2)		6	11	mΑ

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

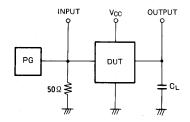


Note 2. I_{CC} is measured with R_E/C_E , C_E open, 4.5V is applied to $\overline{R_D}$, $\overline{A_1}$, $\overline{A_2}$, B_1 and B_2 , with the measurement taken after $\overline{A_1}$ and $\overline{A_2}$ are momentarily dropped to 0V, then raised to 4.5V.

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Зупівої	r al atticlei	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{A_1}$, $\overline{A_2}$ to output Q	• •		19	33	ns
tpLH	Low-to-high-level output propagation time, from input B ₁ , B ₂ to output Q			20	44	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{A_1}$, $\overline{A_2}$ to output \overline{Q}	CT=OpF		21	45	ns
t _{PHL}	High-to-low level output propagation time, from input B_1 , B_2 to output $\overline{\mathbb{Q}}$	Rτ=5k Ω		23	56	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q	C _L = 15pF (Note 3)		18	27	ns
t _{PLH}	Low-to-high-level output propagation time, from input RD to output Q	1		23	45	ns
twQ(min)	Minimum output pulse width, from inputs $\overline{A_1}$, $\overline{A_2}$, B_1 and B_2 to output Q			70	200	ns
two	Output pulse width, from input \overline{A} , B to output Q	$C_T = 1000 pF$, $R_T = 10 k \Omega$ $C_L = 15 pF$ (Note 3)	4	4.55	5	μs

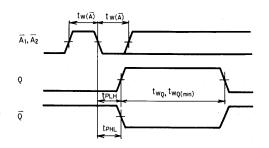
Note 3. Measurement Circuit

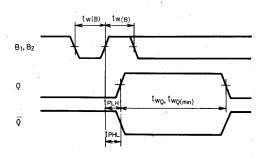


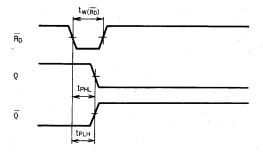
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz (t_{wQ} measurement: 100kHz), t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_Q = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (VCC=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	. Test conditions	Limits			
		rest conditions	Min	Тур	Max	Unit
$t_{W(\overline{A}_1, \overline{A}_2)}$	Trigger A pulse width		40	15		ns
tw(B1, B2)	Trigger B pulse width		40	10		ns
tw(RD)	Direct reset RD pulse width		40	15		ns

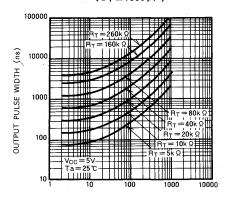






TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH vs C_T , R $(C_T \le 1000 \, pF)$

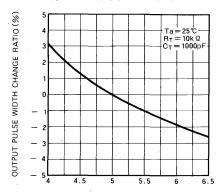


EXTERNAL TIMING CAPACITANCE CT (pF)

K vs C_T (C > 1000 pF)KICOEFFICIENT TO OBTAIN OUTPUT PULSE WIDTH) 0.9 V_{CC} = 5 V 0.8 Ta = 25°C 0.7 =KCTRT(tw 0.6 0.5 0.4 0.3 0.2 0. 103

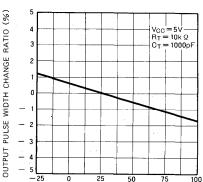
EXTERNAL TIMING CAPACITANCE CT(pF)

CHANGE RATIO OF OUTPUT PULSE VS POWER SUPPLY VOLTAGE



POWER SUPPLY VOLTAGE VCC(V)

CHANGE RATIO OF OUTPUT PULSE vs AMBIENT TEMPERATURE



AMBIENT TEMPERATURE $T_a(^{\circ}C)$

DESCRIPTION

The M74LS123P is a semiconductor integrated circuit containing two retriggerable monostable multivibrator circuits with direct reset inputs.

FEATURES

- Long pulse widths can be generated using the retriggerable function
- Output pulses can be stopped at any time with direct reset inputs
- A, B complementary inputs provided
- High breakdown input voltage $(V_1 \ge 15V)$
- Q and Q outputs provided
- Wide operating temperature range (T_a=-20~+75°C)

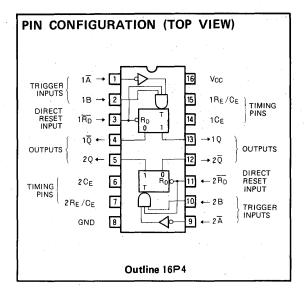
APPLICATION

General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

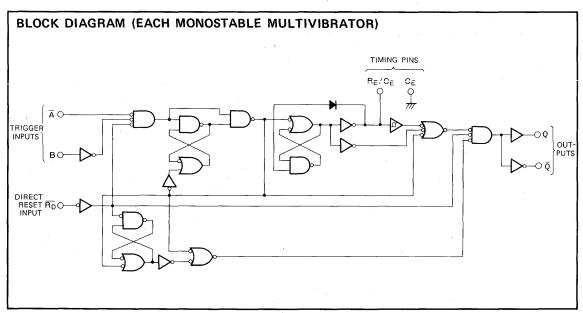
Positive pulses appear in output Q and negative pulses in output \overline{Q} by connecting external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E , as shown in Fig. 1 on the next page, and by applying a trigger from input \overline{A} or B. (Fig. 2(a)) The width tw of the pulses appearing in the outputs is set by R_T and C_T . When \overline{A} changes from high to low or when B changes from low to high, the trigger is applied.

The retriggerable function is used to obtain long output pulse widths and when the trigger is applied from \overline{A} or B immediately before the output pulse is completed, the

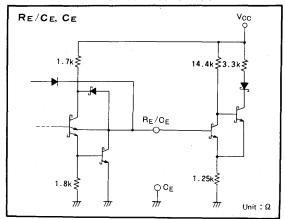


output pulse width can be extended. (Fig. 2(b))

Q can be reset immediately low and \overline{Q} high by setting direct reset input $\overline{R_D}$ low irrespective of the status of the outputs. The output pulse width can therefore be made as short as preferred by the $\overline{R_D}$ signal. (Fig. 2(c)) When $\overline{R_D}$ changes from low to high with \overline{A} at low and B at high, the trigger is applied and the status of Q and \overline{Q} changes.



TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

R _D	Ā	В	Q	Q,
L	X	X	L	Н
×	Н	X	L	Н
X	X	L	L	н
н	L	1		T
Н	Ţ	н	J	T
1	L	Н		7

Note 1. ↑: Transition from low to high. (positive edge triggering)

1: Transition from high to low. (negative edge triggering)

__: Positive one-shot operation.

□ : Negative one-shot operation.

X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and capacitor C_T are connected to timing pins R_E/C_E and C_E. Connect the positive to the R_E/C_E side and the negative to the C_E side when using C_T with polarity. In this case, it is not necessary to connect a switching diode required with the same type of TTL IC. With malfunctions caused by noise, connect CE to the GND line (neighboring on pin 8) as shown by the dotted line in Fig. 1.

To pin R_E/C_E

Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins RE/CE and CE

2. Output pulse width tw

The output pulse width tw is set by RT and CT

2-1. When CT is greater than 1000pF

 $tw=0.45 \cdot R_T \cdot C_T \text{ (ns)} \times (1 \pm 0.1)$

Refer to K-C_T characteristics indicated in TYPICAL CHARACTERISTICS for value of K. (No change is brought to K by value of RT.)

 R_{T} is measured in kilohms and C_{T} in picofarads Depending on the product, fluctuations in the order of 3/-10%may occur.

R_T is measured in kilohms and C_T in picofarads

2-2. When CT is equal to or less than 1000pF Refer to the output pulse width versus-C_T, R_T given in the typical characteristics.

3. Output pulse width control

The output pulse width can be controlled in 3 ways by using, or not using, the trigger signal and $\overline{R_D}$ signal.

3-1. Normal use

This is the normal method of use as a regular monostable multivibrator such as that shown in Fig. 2(a) and the output pulse width tw can be set as for the formula and figure in section 2 above.

3-2. Extension of output pulse width with retrigger func-

As shown in Fig. 2(b), the output pulse width can be extended as desired by applying a trigger pulse before the output pulse is completed.

3-3. Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig. 2(c), the output pulse which has been generated by the trigger signal can be terminated with the RD signal and it is possible to shorten its width as required.

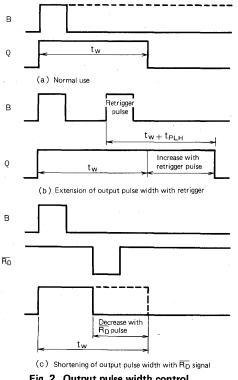


Fig. 2 Output pulse width control

4. Precautions with use

- 4-1. Apply the retrigger pulse after a wait of 0.22C_T (ns) upon application of the trigger pulse. C_T is measured in picofarads. The retrigger pulse during this period is ineffective.
- 4-2. In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible and avoid signal wires which may be conducive to noise.
- 4-3. Connect an external capacitor of 0.01~0.1μF with good high-frequency characteristics between pins V_{CC} and GND.
- 4-4. The output pulse is generated when the power is switched on.

ABSOLUTE MAXIMUM RATINGS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supplý voltage		$-0.5 \sim +7$	V
Vı	Input voltage		-0.5 ~ + 15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		−65 ~ + 150	င

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Paramat	Parameter		Limits				
Symbol		ei	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
	Low-level output current	V _{OL} ≦0.4V	0		4	mΑ		
loL		V _{OL} ≤0.5V	0		8	mΑ		
RT	External timing resistance		5	***************************************	260	kΩ		
Ст	External timing capacitance			No	ne	I.		
CR	RE/CE pin wiring capacitance				50	pF		

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 \,^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			11.5
Зуппоот	l arameter	rest conditions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V.I _{IC} =-18mA			-1.5	٧
VoH	High-level output voltage	$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-400\mu A$	2.7	3.5		V
V _{OL}	Low-level output voltage	V _{CC} =4.75V		0.25 0.35	0.4	V
Ін	High-level input current	V _{CC} =5.25V, V _I =2.7V			20	μΑ
		V _{CC} =5.25V, V _I =10V			0.1	mΑ
lı∟	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.4	m A
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	- 20		-100	mΑ
loc	Supply current	V _{CC} =5.25V (Note 3)		12	20	mΑ

All typical values are at V_{CC}=5V, T_a=25°C.

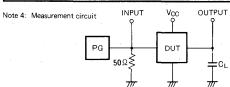


Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with R_E/C_E and C_E open, 4.5V applied to $\overline{R_D}$, \overline{A} and B and \overline{A} set from 0V momentarily to 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_a = 25^{\circ}\text{C}$, unless otherwise noted)

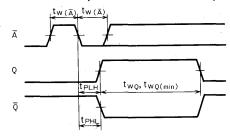
Symbol	Parameter	Test conditions	Limits			11.24
Symbol	Parameter	lest conditions	. Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time, from input \overline{A} to output Q			19	33	ns
t _{PLH}	Low-to-high-level output propagation time, from input B to output Q	1		20	44	ns
tphL	High-to-low-level output propagation time, from input \overline{A} to output \overline{Q}	C _T = 0 pF		21	45	ns
t _{PHL}	High-to-low-level output propagation time, from input B to output $\overline{\overline{Q}}$	$R_T = 5 k \Omega$		23	56	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q	C _L =15 pF (Note 4)		18	27	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output \overline{Q}			23	45	ns
twQ (min)	Minimum output pulse width, from inputs A . B to output Q	1.		66	200	ns
t _{wQ}	Output pulse width, from inputs $\overline{\mathbf{A}}$. $\overline{\mathbf{B}}$ to output \mathbf{Q}	$C_T = 1000 pF$, $R_T = 10 k \Omega$ $C_L = 15 pF$ (Note 4)	4	4.55	5	μs

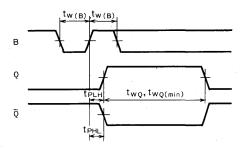


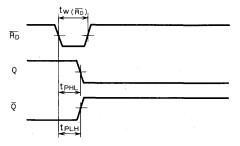
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz (100kHz with t_{WQ} measurement), t_r =6ns, t_i =6ns, t_w \ge 40ns, V_P =3 V_{PP} , Z_Q =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC} = 5 \text{ V}$. $Ta = 25^{\circ}\text{C}$. unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Symbol		rest conditions	Min	Тур	Max	Gnit
t _{W(A)}	Trigger input A pulse width		40	15		ns
t _{W(B)}	Trigger input B pulse width		40	10		ns
t _{W (RD)}	Direct reset input pulse width RD		40	15		ns



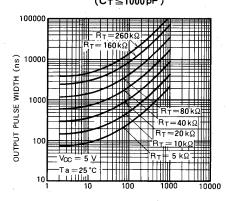




0.1

0L

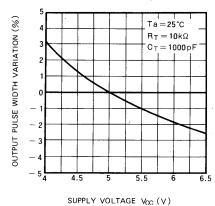
TYPICAL CHARACTERISTICS OUTPUT PULSE WIDTH VS CT, RT (CT≤1000pF)



EXTERNAL CAPACITANCE CT (pF)

Note 5. Error within ±20% of output width given in the figure above.

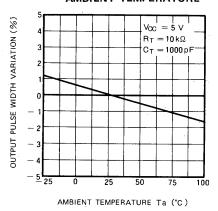
OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



K VS CT (C > 1000 pF)WIDTH) PULSE 0.9 0.8 Ta = 25°C KICOEFFICIENT TO OBTAIN OUTPUT 0.7 0.6 0.5 0.4 0.3 0.2

EXTERNAL TIMING CAPACITANCE CT(pF)

OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS125AP is a semiconductor integrated circuit containing 4 buffers with 3-state outputs and is provided with an output control input \overline{OC} which is independent for each buffer.

FEATURES

- Provided with output control input independent for each of 4 circuits
- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 52mW typical)
- High speed (tpd = 8ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

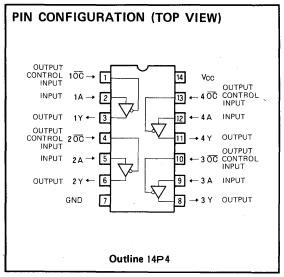
When \overline{OC} is low, high appears in the output Y if input A is high and low appears if A is low. When \overline{OC} is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

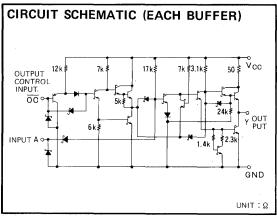
FUNCTION TABLE (Note 1)

ōō	- A	Υ
L	L	L
L	Н	н
Н	X	Z

Note 1: X : irrelevant

Z: high-impedance





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65-+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

			Limits				
Symbol	Parame	Parameter		Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA	
		V _{OL} ≤0.4V	0		12	m,A	
loL	Low-level output current	V ₀ L≦0.5V	0		24	mA	

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

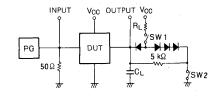
Combal	/mbol Parameter	Tost con-	Test conditions -		Limits		
Symbol	rarameter	Test con-			Тур*	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
.,	High-level output voltage	V _{CC} =4.75V, V ₁ =0.8	V _{CC} =4.75V, V ₁ =0.8V				
V _{он}	High-level output voltage	$V_1 = 2V$, $I_{OH} = -2.6m$	Α	2.4	3.1		V
\/-·	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 12 mA		0.25	0.4	V
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24 mA		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I (OC)	=2V, V ₀ =2.4V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I (OC)	=2V, V ₀ =0.4V			-20	μA
L	tileb ballians and	V _{CC} =5.25V, V _I =2.7	V			20	μА
liн	High-level input current	V _{CC} =5.25V, V _I =10V	1			0.1	mA
lı_	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 40		- 225	mA
locz	Supply current, all outputs off	V _{CC} =5.25V, V _I =0V	. V _{1 (0C)} =4.5V		11	20	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

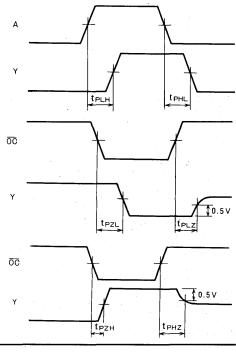
Olsl	0	Test conditions	Limits .			l l - i -
Symbol	Parameter	rest conditions .	Min	Тур	Max	, Unit
t _{PLH}	Low-to-high-level,	C _L =45pF		7	15	ns
tpHL	high-to-low-level output propagation time, from input A to output Y	(Note 3)		10	18.	ns
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		12	20	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	25	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		13	20	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)		13	20	ns

Note 3: Measurement circuit



Parameter	SW 1	SW2
t _{PZH}	Open .	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) All diodes are switching diodes ($t_{rr} = \leq 4ns$)
- (3) C_L includes probe and jig capacitance





Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

M74LS126AP

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS126AP is a semiconductor integrated circuit containing 4 buffers with 3-state outputs and is provided with an output control input OC which is independent for each buffer.

FEATURES

- Provided with output control input independent for each of 4 circuits
- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (P_d = 59mW typical)
- High speed (tpd ≈ 10ns typical)
- Wide operating temperature range (T_a = 20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

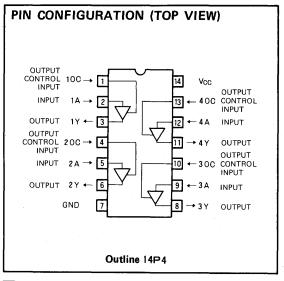
When OC is high, high appears in the output Y if input A is high and low appears if A is low. When OC is low, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

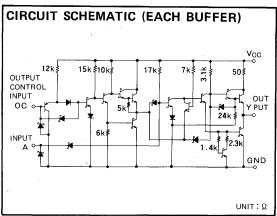
FUNCTION TABLE (Note 1)

OC	Α	Υ
н	L	L
н	Н	н
L.	Х	Z

Note 1: X: irrelevant

Z: high-impedance





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
Vı .	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		 -20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D			Unit		
Symbol	Parameter		Min	Тур	Max	Oint
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA
		V _{OL} ≤0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

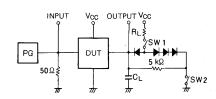
C		T	Tost conditions		Limits		Linta
Symbol	Parameter	Test conditions		Min	Тур 🛊	Max Unit	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	. V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18 mA	-		-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-2.6m		2.4	3.1		. V
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
		V _I =0.8V, V _I =2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _{I(OC)} =	$0.8V, V_0=2.4V$			20	μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V, V _{I(OC)} =	0.8V, V ₀ =0.4V			-20	μA
Luci	High-level input current	V _{CC} =5.25V, V _I =2.7	V -			20	μΑ
Тін	righ-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
l _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 40		- 225	mA
locz	Supply current, all outputs off	V _{CC} =5.25V, V _I =0V			12	22	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V \cdot T_a = 25^{\circ}C$, unless otherwise noted)

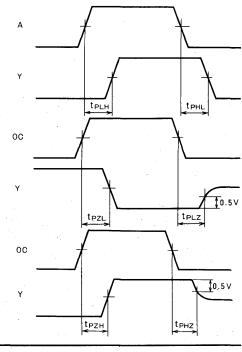
Symbol	Symbol Parameter	Test conditions		Limits		
Syllibol	Faranteter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level,	O AFRE (Note 3)		7	15	ns
t _{PHL}	high-to-low-level output propagation time, from input A to output Y	C _L =45pF (Note 3)		10	18	ns
tpzH	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		14	25	ns
tezL	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		16	35	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		16	25	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		12	25	ns

Note 3: Measurement circuit



Parameter	SW1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) CL includes probe and jig capacitance



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS132P is a semiconductor integrated circuit containing four 2-input positive-logic NAND gates having a Schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin
- High breakdown input voltage (V_I ≥ 15V)
- Low power dissipation (P_d = 35.2mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75 \circ C$)

APPLICATION

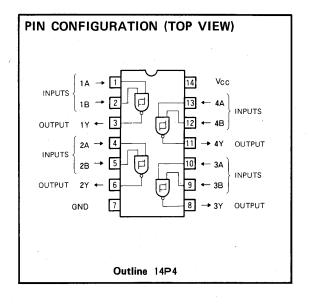
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.8V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in a shaped waveform output without causing oscillation.

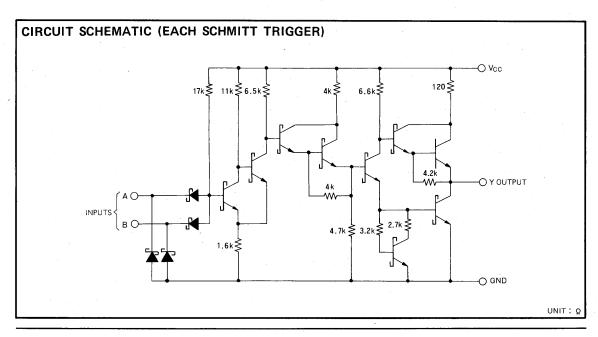
When inputs A and B are high, output Y is low, and when either or both inputs are low, Y is high.

Refer to M74LS14P for the typical characteristics.



FUNCTION TABLE

A	В	Y
L	L	н
Н	L	н
L	Н	Н
Н	н.	L



QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

ABSOLUTE MAXIMUM RATINGS (Ta = $-20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V ₁ .	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	rc
Tstg	Storage temperature range		-65~+150	°C .

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

	_		Limits			Links	
Symbol	mbol Parameter		Miņ	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
		V _{OL} ≤0.4V	V _{OL} ≤0.4V	0		4	mA
OL	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

	Parameter Test conditions			Limits			Unit
Symbol	Parameter	rest conditions		Min	Typ *	Max	Unit
V _T +	Positive-going threshold voltage	V _{CC} =5V		1.4	1.6	1.9	٧
V _T –	Negative-going threshold voltage	V _{CC} =5V		0.5	0.8	1	٧
V _T + V _T	Hysteresis width	V _{CC} =5V		0.4	0.8		V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} = - 18mA				1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V, V_{I} = 0$ $I_{OH} = -400 \mu A$	0.5V	2.7	3.4		٧
	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL		V _I = 1.9V	I _{OL} =8mA		0.35	0.5	V
IT+	Input current at positive-going threshold	$V_{CC}=5V$, $V_1=V_T$	+		-0.14		mA
I _T _	Input current at negative-going threshold	$V_{CC}=5V$, $V_{J}=V_{T}$	_		-0.18		mA
1	Lijoh lavel izavet avraget	V _{CC} =5.25V V _I =2.7V	,			20	μА
ИН	High-level input current	V _{CC} =5.25V V _I =10V				0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =	0.4V			-0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	=0V	- 20		- 100	mA
Госн	Supply current, all outputs high	V _{CC} =5.25V, V _I =	:0V		5.9	11	mA
Iccl	Supply current, all outputs low	V _{CC} =5.25V, V _I =	4.5V		8.2	- 14	mA

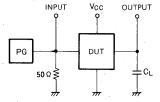
^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25\%$, unless otherwise noted)

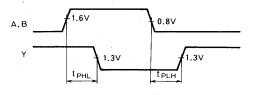
Symbol	Parameter	Test conditions		Limits		
Symbol	Symbol	rest conditions	Min	Тур	Max	· Unit
t _{PLH}	Low-to-high-level output propagation time	O — 15 p = (Note 2)		12	22	ns
t _{PHL}	High-to-low-level output propagation time	C _L = 15pF (Note 2)		14	22	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics:
 - PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM



M74LS133P

SINGLE 13-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS133P is a semiconductor integrated circuit containing one 13-input positive-logic NAND gate, usable as a negative logic NOR gate.

FEATURES

- High breakdown input voltage (V₁ ≥ 15V)
- Low power dissipation (P_d = 2.5mW typical)
- High speed (tpd = 11ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

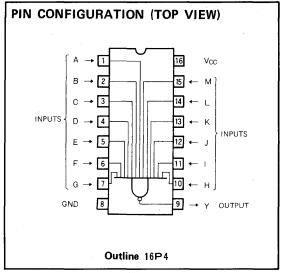
The use of PNP transistors for the inputs and active pull-up transistors for the outputs enables input high breakdown voltage, high speed, low power dissipation and high fan-out.

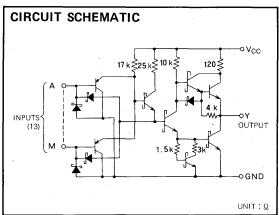
When inputs A through M are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

Α	N	Υ
L	L	Н
Н	L	Н
L	н	H
Н	Н	L

 $N = B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	· v
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	.V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

SINGLE 13-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D		Limits			Unit	
	raramet	Parameter			Max	Utill	
Voc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≥2.7V	0		-400°	μΑ	
		V ₀ L≦0.4V	0		4	mA	
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

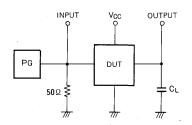
Symbol	Parameter	T	Total constitution		Limits		
Symbol .	Parameter Test conditions		onditions	Min	Typ *	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_{I} = 0.8V$ $I_{OH} = -400\mu A$		2.7	3.4		V
	Louvieus	V _{CC} = 4.75 V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V ₁ =2V	I _{OL} =8mA		0.35	.0.5	٠.٨
	Dief level in	V _{CC} =5.25V, V _I =2	2.7V			20	μΑ
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =1	10V			0.1	mA
1 _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0	V _{CC} =5.25V, V _I =0.4V			0.4	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =	0V	-20		100	mΑ
Icch	Supply current, all inputs high	V _{CC} =5.25V. V _I =0	OV.		0.35	0.5	mA
Iccl	Supply current, all inputs low	V _{CC} =5.25V. V _I =0	Open		0.6	1.1	mA

 $[\]pmb{*}$: All typical values are at $\,V_{CC}\!=\!5V$, $\,T_{a}\!=\!25^{\circ}\!C$

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

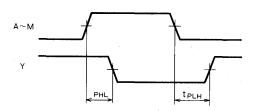
Sv	Symbol Parameter	Test conditions		Limits		Unit	
		rest conditions	Min	Тур	Max	Unit	
tr	PLH	Low-to-high-level/high-to-low-level	0 15-54) 0		6	15	ns
tr	PHL	output propagation time	C _L = 15 pF (Note 2)		16	38	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



PRECAUTION FOR USE

Connect pins not being used to the V_{CC} supply voltage.

Note 1: All measurements should be done quickly.

MITSUBISHI LSTTLs

M74LS136P

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS136P is a semiconductor integrated circuit containing 4 dual-input exclusive-OR gates with open collector output.

FEATURES

- Usable in wire-AND connection
- High breakdown output voltage ($V_0 \ge 7V$)
- Low power dissipation (P_d = 30.5mW typical)
- High speed (tpd = 13ns typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

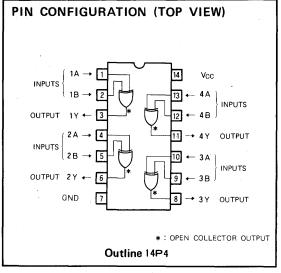
FUNCTIONAL DESCRIPTION

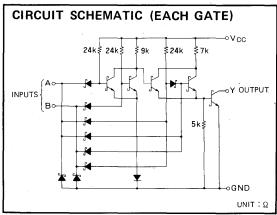
With the use of open collector output, the high-level output impedance can be freely selected by means of an external resistor. This make possible use in the wire-AND, which has been impossible with conventional gates.

When both inputs A and B are high or both low, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

Α	В	Υ
L	Г	L
н	Ĺ	Н
L	Н	н
Ħ	I	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Limits	Unit
Vcc	Supply voltage			-0.5~+7	
VI	Input voltage			-0.5~+15	V
Vo	Output voltage	High-level state		-0.5~+7	V
Topr	Operating free-air ambient temperature range			−20~+75	°C
Tstg	Storage temperature range			-65 - + 150	°C



QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	D		Unit			
Symbol	Paramet	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5 . 25	٧
Іон	High-level output current	V ₀ = 5.5V	0		100	μА
:		V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Constant					Limits			
Symbol	Parameter	lest cond	Test conditions			Max	Unit	
VIH	High-level input voltage						V	
VIL	Low-level input voltage					0.8	V	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	٧	
	I the base of the second	V _{CC} =4.75V. V _I =0.	$V_{CC}=4.75V$, $V_1=0.8V$ $V_1=2V$, $V_0=5.5V$			100		
Іон	High-level output current	$V_1 = 2V$, $V_0 = 5.5V$				100	μА	
.,		V _{CC} = 4.75 V	I _{OL} =4mA		0.25	0.4	V	
V _{OL}	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	V	
` .	History and the second	V _{CC} =5.25V, V _I =2.	7V			40	μΑ	
ІІН	High-level input current	V _{CC} =5.25V. V _I =10	V			0.2	mA	
l _{IL}	Low-level input current	V _{CC} =5.25V. V _I =0.	V _{CC} =5.25V. V _I =0.4V			-0.8	mA	
loc	Supply current	V _{CC} =5.25V (Note 1)		1	6.1	10	mA	

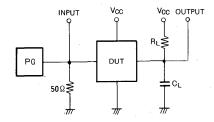
^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: I_{CC} is measured with all inputs grounded.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

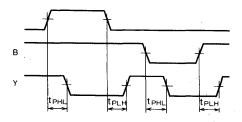
Symbol	Parameter	Test conditions		Limits			
Symbol	Tarameter	lest conditions	Min	Тур	Max	Unit	
tpLH	Low-to-high-level, high-to-low-level output propagation	R _L = 2 kΩ		14	30	ns	
tpHL	time,	C _L = 15 pF Other input low (Note 2)		14	30	ns	
tpLH	Low-to-high-level, high-to-low-level output propagation	$R_L = 2 k\Omega$		12	30	ns	
tpHL	time,	C _L = 15 pF Other input high (Note 2)		12	30	ns	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P.P}$, Z_Q = 50Ω

(2) C_L includes probe and jig capacitance.



MITSUBISHI LSTTLS M74LS137P

3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74LS137P is a semiconductor integrated circuit containing a 3-line-to-8-line decoder/multiplexer function with address latch.

FEATURES

- Address latch capability with latch enable input
- Easy cascade connection with two enable inputs
- Wide operating temperature range (Ta: −20 − +75°C)

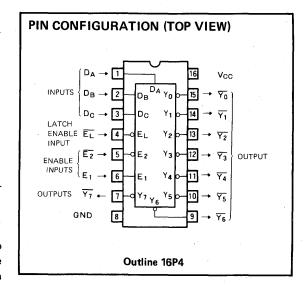
APPLICATIONS

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTIONS

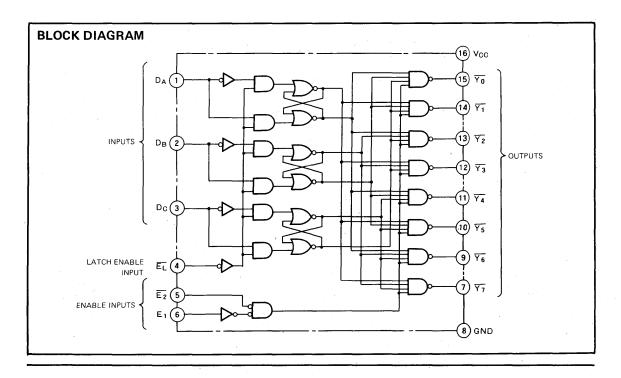
When latch enable input $\overline{E_L}$ is low, the data applied to inputs $D_A - D_C$ are read into the latch; when it is high, the device operates as a decoder/demultiplexer with a function that retains the data

When the device is used as a decoder and inputs D_A-D_C are designated with a 3-bit binary code, one output among outputs $\overline{Y_0}-\overline{Y_7}$ corresponding to the numerical value is set low and the other seven outputs are all set high. In this case, enable input $\overline{E_1}$ is set high and enable input $\overline{E_2}$ is set low. When E_1 and $\overline{E_2}$ are subject to any other conditions, the outputs are set high regardless of the status of D_A-D_C . (Refer to application examples)



When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making E_1 and \overline{E}_2 the data inputs and D_A-D_C the selection inputs.

This IC is the same as the M74LS138P except that it features a latch function in inputs $D_A\!-\!D_C$.



3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

FUNCTION TABLE

EL	Εı	Ε̈́2	Dc	DB	DΔ	۱×۶	<u>Y</u> 1	Y ₂	Y ₃	$\overline{Y_4}$	$\overline{Y_5}$	Y ₆	Y ₇
×	х	Н	Х	х	Х	Ξ	Н	Н	Н	Н	Н	Ŧ	H
×	L	х	Х	х	Х	Ι	Н	Н	Н	Н	Н	Н	H
L	Н	L	L	L	L	L	Н	Н	Н	Н	Ι	I	Н
┌	Н	L	L	L	Ι	Ι	L	н	Ή	Н	I	Н	Τ
L	Н	L	L	Н	Г	Ι	Η,	Ļ	Н	Н	Ι	π	H
L	Н	L	L	Η	Н	Η	Н	Н	L	Н	Ι	Ξ	Ι
L	I	L	I	L	Γ	H	Ι	Η	H	اد	Ι	I	Н
L	I	L	I	٦	Ι	Ι	Н	Η	Н	Ι	١	I	н
L	Н	L	Н	Н	L	Н	Н	Η,	Н	Н	Н	L	Н
L	н	L	Η	Η	Н	Ι	Н	H ·	Н	Η	Н	Η	L
Н	Ι	L	×	X	×	Output corresponding to stored address, L; all other, H.							

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	, . °C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter		11.25			
Зульы	raiameter	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
1.0	Low-level output current	V _{OL} ≤0.4V	0		4	mA
'0	Low-level output current		0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

0						Limits		
Symbol	Parameter		Test condition	Min	Тур*	Max	Unit	
VIH	High-level input voltage	,		2			٧	
VIL	Low-level input voltage					0.8	٧	
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18m	n A			-1.5	٧
VoH	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		٧
V _{OL}	Low-level output voltage		$V_{CC}=4.75V$ $V_{I}=0.8V, V_{I}=2V$	I _{OL} =4mA		0.25 0.35	0.4	V V
l _{IH}	High-level input current	:-1	V _{CC} =5.25V, V _I =2.7V V _{CC} =5.25V, V _I =10V	•			20 0.1	μA mA
I _{IL}	Low-level input current	E _L , E ₁ , E ₂	V _{CC} =5.25V, V _I =0.4V				- 0.4 - 0.2	mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		- 20		-100	mΑ
lcc .	Supply current		V _{CC} =5.25V (Note 3)	-		. 11	18	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

Note 3: Supply current should be measured with all inputs grounded.



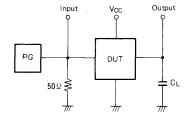
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	0			Test conditions		Limits		
Symbol	Parameter	rarameter rest conditions				Тур	Max	Unit
t _{PLH}	Low-to-high, high-to-low output		2			8	17	
t _{PHL}	propagation time, from inputs D_A , D_B , D_C to outputs $\overline{Y_0} - \overline{Y_7}$		4			15	38	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from inputs DA, DB,	stages	3			10	24	
t _{PHL}	D_C to outputs $\overline{Y_0} - \overline{Y_7}$	gate st	3			13	29	ns
t _{PLH}	Low-to-high, high-to-low output	ay ge	2	C ₁ = 15pF (Note 4)		9	21	
t _{PHL}	propagation time, from input E_2 to outputs $\overline{Y}_0 - \overline{Y}_7$	of delay	2	CL= 15pr (Note 4)		10	27	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from input E ₁		3			10	21	
t _{PHL}	to outputs $\overline{Y_0} - \overline{Y_7}$	Vumber	3			12	27	ns
t _{PLH}	Low-to-high, high-to-low output	_	3			13	27	
t _{PHL}	propagation time, from input E_L to outputs $\overline{Y_0} = \overline{Y_7}$		4			18	38	ns

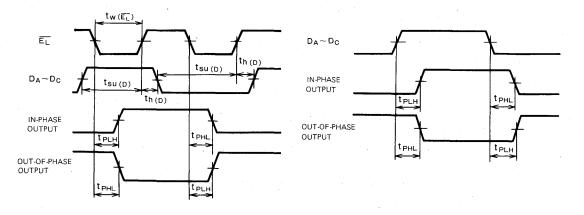
Note 4: Measurement circuit



- The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_r = 6ns$, $t_w = 500ns$, $V_P = 3V_{P,P}$, $Z_0 = 500ns$.
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

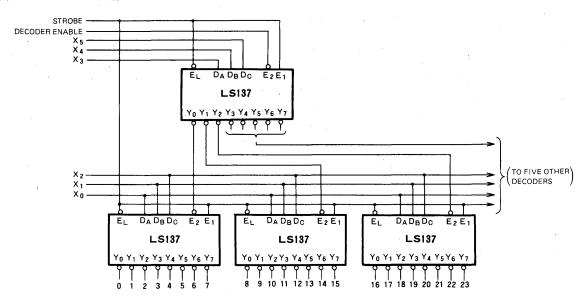
				Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
tw(EL)	Latch enable EL pulse width		15	4		ns	
t _{su(D)}	Setup time D _A - D _C to $\overline{E_L}$		10	3		ns	
t _{h(D)}	Hold time D _A D _C to E _L		10	0		ns	



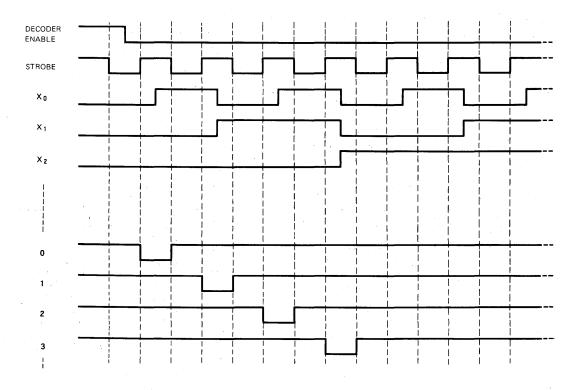
3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

APPLICATION EXAMPLES (6-bit 2-line-to-64-line decoder with address latch)

(a) CIRCUIT DIAGRAM



(b) FUNCTION WAVEFORM



3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS138P is a semiconductor integrated circuit consisting of a 3-bit binary-octal decoder/demultiplexer with enable inputs.

FEATURES

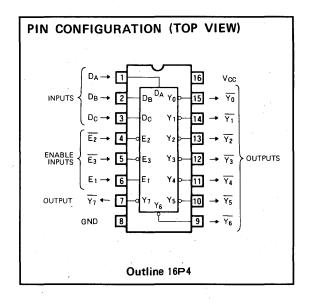
- 3 classes of enable inputs
- 4 to 16 decorder/demultiplexer functions are provided without use of external components.
- Wide operating temperature range (T_a = -20 ~ +75°C)

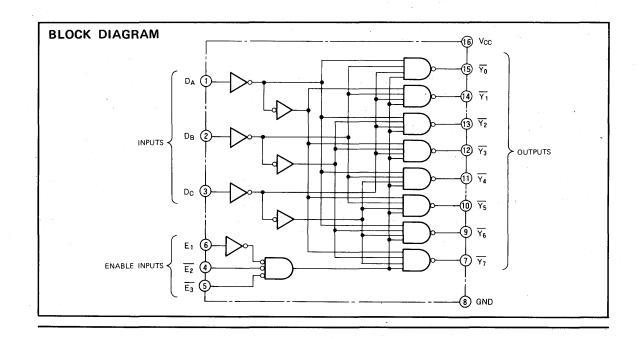
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

For use as a decoder, specify inputs D_A , D_B , and D_C in 3-bit binary code. In the case of decoding function, the E_1 is kept in high state while \overline{E}_2 and \overline{E}_3 are kept low. If E_1 , \overline{E}_2 and \overline{E}_3 are not in these conditions, all the outputs become high, irrespective of the status of $D_A \sim D_C$. For use as a demultiplexer, \overline{E}_1 , \overline{E}_2 and E_3 are used as data inputs and D_A , D_B , and D_C as selection inputs. This forms a 1-line to 8-line demultiplexer.





M74LS138P

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

E ₁	Ēχ	Dc	DB	DA	$\overline{Y_0}$	$\overline{Y_1}$	Y ₂	<u>Y</u> 3	<u>Y</u> 4	Y ₅	Y ₆	$\overline{Y_7}$
X	Н	X	Х	Х	Н	Н	н	Н	н.	Н	н	I.
L	Х	×	X	Х	н	н	Н	Н	·H	Н	н	Н
н	L	L	L	L	L	Н	н	Н	н	н	н	H
Н	L	L	·L	Н	Н	L	Н	н	Н	Н	Н	н
·H	, L	L	Н	L	Н	Н	L	н	Н	H	н	н
Н	L	L	Н	н	н	н	Н	L	Н	н	· н	Н
Н	L	H	L	L	Н	Н	Н	Н	L	Н	н	н
н	L	н	L	Н	H	Н	н	н	Ι	٦	н	Н
н	L	H	٠н	L ,	Н	Н	Н	Н	Н	Н	L	Н
Н	L	Н	н	н	н	Н	Н	Н	н	н	н	L

Note 1: $\overline{E_X} = \overline{E_2} + \overline{E_3}$ X: irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	. V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		- 65 +- 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol			Limits		Unit	
Symbol	Parame	Parameter		Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	B	Test con	Test conditions		Limits		
	Parameter	l est cond			Тур*	Max	Unit
ViH	High-level input voltage		2			V	
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
VoH	High-level output voltage	$V_{CC} = 4.75V$, $V_1 = 0.8V$ $V_1 = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		٧
	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
VoL		$V_{I} = 0.8V, V_{I} = 2V$	I _{OL} =8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.	V _{CC} =5.25V, V _I =2.7V			20	μА
Ιн		V _{CC} =5.25V, V _I =10V				0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V _{CC} =5.25V, V _O =0V			- 100	mA
loc	Supply current	V _{CC} =5.25V (Note 3)		6.3	10	mA	

* : All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all output off-state.

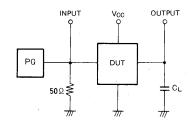


M74LS138P

SWITCHING CHARACTERISTICS ($V_{CO}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	0	Test conditions		Limits			
	Parameter		Min	Тур	Max	Unit	
.t _{PLH}	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	delay gate stages			9	20	ns
t _{PHL}		2			12	41	ns
tpLH		delay gate stages			16	27	ns
t _{PHL}		3	O 45 - 5 (Nove 4)		14	39	ns
t _{PLH}		delay gate stages	C _L = 15 pF (Note 4)		10	18	ns
t _{PHL}		2	,		15	32	ns
tPLH		delay gate stages			8	26	ns
t _{PHL}		·		15	38	ns	

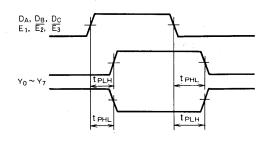
Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- (2) C_L includes probe and jig capacitance.

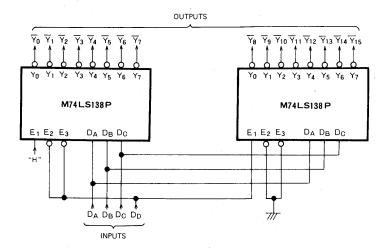
TIMING DIAGRAM (Reference level = 1.3V)

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER



APPLICATION EXAMPLE

4-line to 16-line decorder/demultiplexer



DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS139P is a semiconductor integrated circuit containing two 2-bit 2-line-to-4-line decoders/demultiplexers with separate enable inputs.

FEATURES

- Enable inputs provided
- Two circuits completely separate
- Wide operating temperature range (T_a=-20~+75°C)

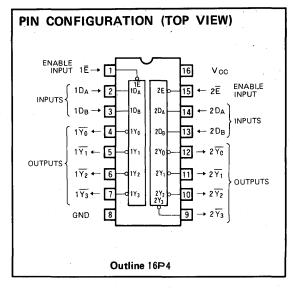
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

For use as a decoder, when inputs D_A and D_B are specified in 2-bit binary code, the output corresponding to the number among $\overline{Y_0}{\sim}\overline{Y_3}$ is set low and all the other 3 outputs are set high. The enable inputs \overline{E} are kept low. When inputs \overline{E} are high, all the outputs are set high irrespective of the status of D_A and D_B .

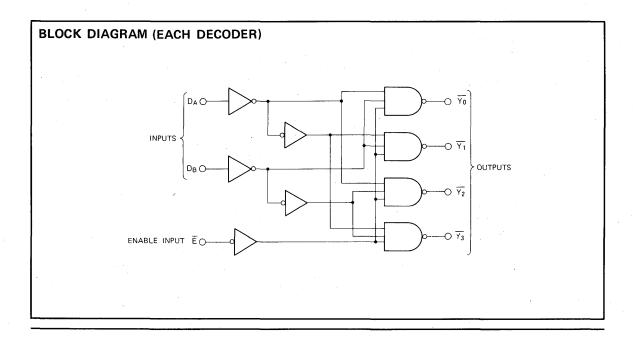
For use as a 1-line-4-line demultiplexer, make inputs \overline{E} the data inputs and D_A and D_B the selection inputs.



FUNCTION TABLE (Note 1)

Ē	DB	DA	$\overline{Y_0}$	<u> </u>	$\overline{Y_2}$	Ϋ́з
Н	X	X	Н	Н	Н	Н
L	L	L	L	Н	Н	Н
L	L	Н	Н	L	н	н
L	н	L	н	н	L	Н
. L	Н	Н	Н	Н	Н	L

Note 1: X : Irrelevant



DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75$ °C, unless otherwise ntoed)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
Vi	Input voltage		-0.5~+15	V	
Vo	Output voltage	High-level state	-0.5~ Vcc	V	
Topr	Operating free-air ambient temperature range		20~+75	°C	
Tstg	Storage temperature range		-65~ +150	°C	

. RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	D			11.2		
	Parameter	Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
		V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current V _{OL} ≤0.5V		0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Total	Tost conditions		Limits		
Symbol		Test conditions		Min	Typ *	Max	Unit
ViH	High-level input voltage		2			V	
VIL	Low-level input voltage				0.8	V	
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-			-1.5	V	
.,	High-level output voltage	$V_{CC} = 4.75V, V_1 = 0$.8V	2.7	2.4		V
V _{OH}		V _I =2V, I _{OH} =-400	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		V
	Low-level output voltage	V _{GC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
V _{OL}		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	٧
	Diet I I in .	V _{CC} =5.25V, V _I =2.	7V			20	μΑ
Ιн	High-level input current	V _{CC} =5.25V, V _I =10	V _{CC} =5.25V, V _I =10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 20		100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			6.8	11	mΑ

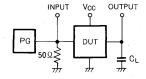
^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

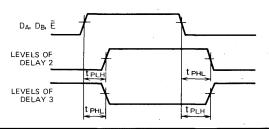
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
Symbol			rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs DA, DB to outputs $Y_0 - \overline{Y_7}$ delay gate stages	dealy gate stages			8	20	ns
t _{PHL}		2			15	33	ns
t _{PLH}		delay gate stages			10	29	ns
t _{PHL}		3	C _L = 15 pF (Note 4)		15	38	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				8	24	ns
t _{PHL}	time, from input \overline{E} to outputs $\overline{Y_0} - \overline{Y_7}$				12	32	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_{P-P} , Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance



Note 3: I_{CC} is measured with the outputs in the enable state.

M74LS145P

BCD-TO-DECIMAL DECODER/DRIVER

DESCRIPTION

The M74LS145P is a semiconductor integrated circuit provided with BCD-to-decimal decoder/driver function and open collector outputs.

FEATURES

- High output current (I_O=80mA with V_{OL}≤3V;
 I_O= 24mA with V_O≤0.5V)
- High output breakdown voltage (V_O ≥15V)
- All outputs high with reactive input
- Wide operating temperature range (T_a=-20~+75°C)

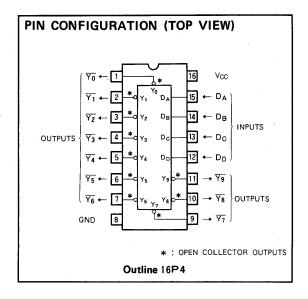
APPLICATION

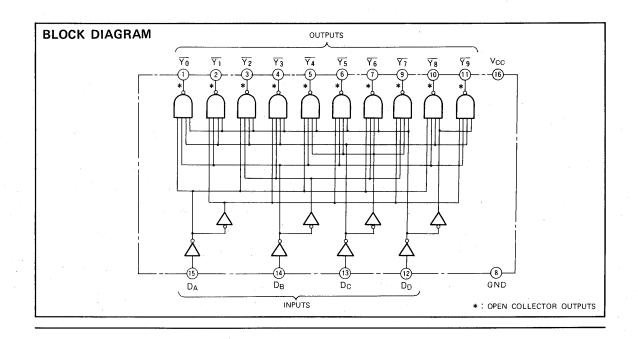
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When inputs D_A , D_B , D_C and D_D are designated with a BCD code in this decoder/driver, the $\overline{Y_0} \sim \overline{Y_9}$ output corresponding to the number is set low while the other 9 outputs are set high. When a binary number of 10 or more is applied to $D_A \sim D_D$, all the outputs are set high.

The outputs are open collector types with a breakdown voltage of 15V and an I_{OL} of 80mA (with $V_{OL} \le 3V$) This device is therefore suitable for use as an LSTTL/MOS interface, display tube and relay driver.





BCD-TO-DECIMAL DECODER/DRIVER

FUNCTION TABLE

Decimal number	D_{D}	D _C	DB	D _A	Y ₀	$\overline{Y_1}$	Y ₂	Y 3	<u>Y</u> 4	Y ₅	Y ₆	<u>Y</u> 7	Y ₈	√ Y 9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	н
1	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	н	Н	н
2	L	L	Н	L	н	н	L	Η	н	Н	Н	Н	Н	Н
3	L	L	Н	Η	Н	Н	Н	┙	н	Н	Н	Н	Н	н
4	L	н	L	L	н	Н	Н	н	L	н	н	н	Н	Н
5	L	Н	L	н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	Н	н	Н	н	н	н	L	н	Н	Н
7	L	н	Н	н	Н	Н	Н	н	Н	Н	Н	L	Н	Н
8	Н	L	L	L	Н	Н	Н	Н	н	Н	Н	н	L	н
9	Н	L	L	Н	н	Н	Н	н	н	Н	Н	Н	Н	L
10	н	L	Н	L	н	Н	Н	Н	н	н	Н	. н	Н	н
. 11	Н	L	Н	н	н	Н	н	Н	Н	Н	٠Н	Н	н	Н
12	Н	Н	L	L	н	н	н	Н	н	н	н	Н	н	Н
13	Н	н	L	Н	н	I	Н	н	I	Н	Н	Н	Н	Н
14	Н	н	н	L	Τ	н	н	Н	н	н	н	Н	Н	Н
15	Н	Н	Н	Н	Н	Н	H.	Н	Η	Н	Н	Н	Н	Н

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+15	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet			Limits	Unit	
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} =15V	0		250	μА
		V ₀ ∟≤0.4V	0		12	mΑ
loL	Low-level output current	V ₀ L≦0.5V	0	1000	24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Completed	D	Tarkarand			Limits		11.5
Symbol	Parameter	Test cond	tions	Min	Typ*	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V.1 _{IC} =-	-18mA			-1.5	٧
Іон	High-level output voltage	$V_{CC} = 4.75V \cdot V_1 = 0$ $V_1 = 2V \cdot V_0 = 15V$.8V			250	μА
		Vcc=4.75V	I _{OL} = 12 mA		0.25	0.4	V
VoL	Low-level output voltage	$V_{CC}=4.75V$ $V_{I}=0.8V, V_{I}=2V$	I _{OL} =24 mA		0.35	0.5	V
	·	V ₁ =0.8V, V ₁ =2V	I _{OL} = 80mA		2.3	3	V
		V _{CC} =5.25V, V _I =2.	7V			20	μА
liH	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA
liE	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
Icc	Supply current	V _{CC} =5.25V (Note	1)	1	7	13	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

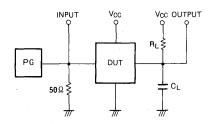
Note 1: I_{CC} is measured with $D_A\!\sim\!D_D$ at 0V.

BCD-TO-DECIMAL DECODER/DRIVER

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

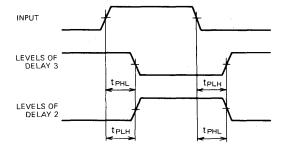
Symbol	Parameter		Test conditions		Limits		Unit
- Cymbol			rest conditions	Min	Тур	Max	Onit
t _{PLH}		delay gate stages			27	50	ns
t _{PHL}	Low-to-high-level, high-to-low-level	2	D 0550 0 -45mE (Nov. 2)		17	50	ns
t _{PLH}	output propagation time	delay gate stages	R _L =665Ω, C _L =45pF (Note 2)		27	50	ns
t _{PHL}		3	÷		17	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_{P-P} , Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference=1.3V)



MITSUBISHI LSTTLS M74LS147P

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

DESCRIPTION

The M74LS147P is a semiconductor integrated circuit containing a 10-line BCD encoder with a priority function.

FEATURES

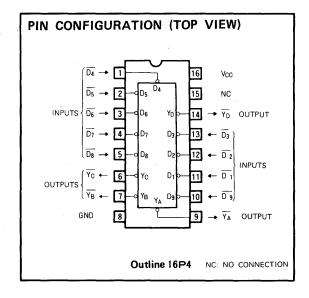
- · Priority decoding of the data inputs
- Data inputs and outputs both active-low
- Wide operating temperature range (T_a = -20 ~ +75°C)

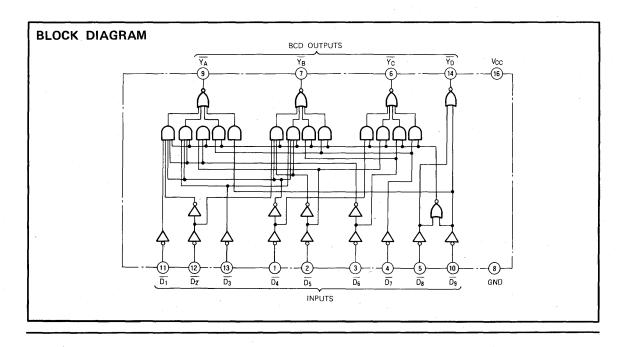
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions to encode a pulse entered through one of the nine input pins $(\overline{D_1} \sim \overline{D_9})$ into a BCD code by producing an inverted signal (based on input) at output $\overline{Y_A} \sim \overline{Y_D}$. The encoder handles all inputs in a priority sequence, so that when two or more are present at input at the same time, the signal present at the highest priority pin will be encoded. $\overline{D_0}$ does not exist as an input, and when all inputs are at high-level, all outputs will also be high-level, yielding a 0 output. Ideally suited for use as a keyboard encoder or range selector.





10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

FUNCTION TABLE (Note 1)

D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D7	D8	D ₉	ΥD	Yo	ŸΒ	ŸΑ
Н	Н	н .	Н	Н	Н	Н	Н	Н	Н	H	Н	Н
Х	Х	X	X	X	Х	X	х	L	L	н	Н	L
×	X	X	X.	X	х	X	L	н	L	н	Н	Н
Х	Х	Х	Х	X	×	L	Н	н	Н	L	L	L
×	X	X	X	Х	L	Н	Н	Н	Н	L	L .	Н
X	X	X	X	L	Н	T	. Н	Н	Н	L.	Н	L
Х	Х	X	Ľ	H	Н	Н	Н	Н	Н	L	Н	н
Х	X	L	Н	Н	н	Н	Н	H	Н	н	L	L
- X	L	Н	Н	Н	H.	H	Н	Н	н	Н	L,	н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	L

Note 1. X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5∼+15	V
Vo	Output voltage	High-level output	-0.5 ~ V _{CC}	V
Topr	Operating free-air ambient temperature range		- 20 ~ + 75	°C
Tstg	Storage temperature range		- 65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D			Limits		
Symbol	Paramete	er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mA
lor.	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Task Co.	altata		Limits			
Зуппон	rarameter	Test Con	aitions	Min	Typ *	Max	Unit	
ViH	High-level input voltage			2			V	
VIL	Low-level input voltage					0.8	V	
Vic	Input clamp voltage	Vcc=4.75V, IIC=-	- 18mA			-1.5	٧	
Voн	High-level output voltage	V _{CC} =4.75V, V _I =0. V _I =2V, I _{OH} =-400		2.7	3.4		٧	
VoL	Low-level output voltage	Vcc=4.75V	IoL=4mA		0.25	0.4	V	
VOL	2000-level output voltage	V _I =0.8V, V _I =2V	loL = 8mA		0.35	0.5	V	
lin	High-level input current	Vcc=5.25V, Vi=2.	7V			20	μА	
'III	rightever input current	V _{CC} =5.25V, V _I =10	V			0.1	mA	
lıL.	Low-level input current	Vcc=5.25V, Vi=0.	4V			-0.4	mA	
los	Short-circuit output current (Note 2)	Vcc=5.25V, Vo=0	V	-20		— 100	mA	
loc1	Supply current	Vcc=5.25V (Note 3)			12	20	mA	
ICC2	Supply current	Vcc=5.25V (Note 4)			10	17	mA	

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

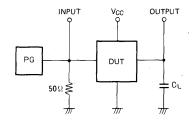
^{3.} I_{CC1} is measured with $\overline{D_7}$ at OV, and all other inputs open.

^{4.} I_{CC2} is measured with all inputs open.

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

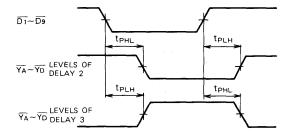
Symbol	Parameter	Test Conditions		Limits		Unit
Symbol	, aratheter	rest Conditions	Min	Тур	Max	Offic
tpLH	Low-to-high-level, high-to-low-level output propagation time,			9	18	ns
tpHL	from input $\overline{D_1} \sim \overline{D_9}$ to output $\overline{Y_A} \sim \overline{Y_D}$ (levels of delay 2)	C ₁ = 15pF (Note 5)		14	18	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time,			25	33	ns
tpHL	from input $\overline{D_1} \sim \overline{D_9}$ to output $\overline{Y_A} \sim \overline{Y_D}$ (levels of delay 3)			15	23	ns

Note 5. Measurement Circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, $Z_0 = 50\Omega$. (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



8-LINE TO 3-LINE PRIORITY ENCODER

DESCRIPTION

The M74LS148P is a semiconductor integrated circuit provided with an 8-line to 3-line priority encoder function and priority sequence function.

FEATURES

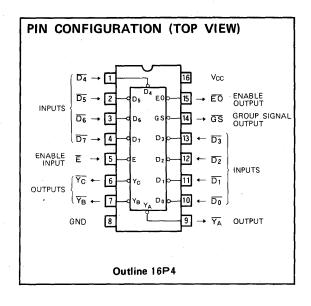
- Priority decoding of the data input
- Easy expansion of the number of input bit
- Wide operating temperature range (T_a=-20~+75°C)

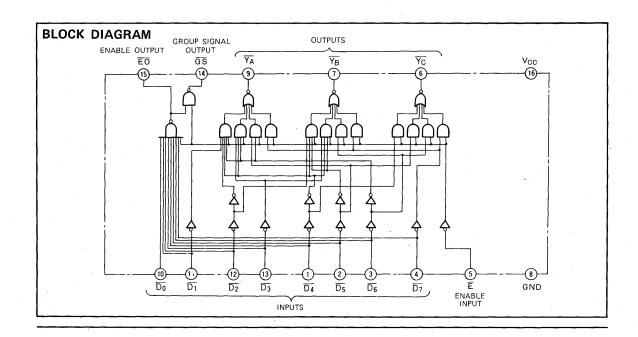
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When signals are applied to one of this encoder's eight inputs $\overline{D_0}{}^{\sim}\overline{D_7}$, the 3-bit binary number corresponding to the input pin appears at outputs $\overline{Y_A}{}^{\sim}\overline{Y_C}$. Since priority is given to each input, the highest-level input pin signal is encoded when more than one signals are applied simultaneously. The number of input data can easily be increased as shown in the application example using the enable input \overline{E} , enable output $\overline{E}\overline{O}$ and group signal output \overline{GS} . This device is suitable for use as a keyboard encoder or for range selection.





8-LINE TO 3-LINE PRIORITY ENCODER

FUNCTION TABLE (Note 1)

Ē	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	YC	Ϋ́Β	Ϋ́Α	GS	ΕO
Н	×	×	×	Х	X	X	X	X	Н	Н	н	Н	Н
L	Н	Н	н	н.	Н	н	н	н	Н	. н	н	н	L
L	×	×	×	Х	×	Х	×	L	L	L	L	L	н
L	X	X	Х	Х	Х	Х	L	н	L	L	н	L	н
L	· X	×	×	X	X	L	н	н	L	Н	L	L	н
L	×	X	X	Х	L	Н	н	н	L	Н	н	L	н
L	X	×	×	٠ ـ	Н	н.	н	н	Н	L	L	L	Н
L	X	×	L	Н	Н	Н	н	н	Н	L	Н	L	н
L	×	L	н	Н	н	н	н	н	н	н	L	L	н
L	L	Н	Н	Н	н	н	н	н	Н	Н	Н	L.	н

Note 1 X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5 ∼+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parame		Unit			
Symbol	rarame	ter .	Min Tyr		Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
-		V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V ₀ ∟≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	tor	Test condit	tions		Limits		Unit
Symbol	rarame	ter	rest condit	tions	Min	Тур 🛊	Max	Unit
V _{IH}	High-level input voltage				2			V
VIIL	Low-level input voltage			*			0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
V _{OH}	High-level output voltage		$V_{OC}=4.75V, V_{I}=0.8$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V	IoL 4mA		0.25	. 0.4	V
VOL	2011 love output vortage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} 8mA		0.35	0.5	V
		D ₀ , E	V _{CC} =5,25V, V _I =2,7				20	
·I _{IH}	High-level input current	$\overline{D_1} \sim \overline{D_7}$	VCC-5.25V, VI-2.1	v			40	μΑ
TH	r ngir-lever input current	D ₀ , E	V 5 05V V 10V				0.1	mΑ
		$\overline{D_1} \sim \overline{D_7}$	V _{CC} =5.25V, V _I =10V				0.2	.IIIA
l _{IL}	Low-level input current	D₀, Ē	V _{CC} =5.25V, V _I =0.4				-0.4	mA.
III.	Low level input current	$\overline{D_1} \sim \overline{D_7}$	VCC-5.25V, VI=0.4	· V			-0.8	11112
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0\	/	-20		- 100	m A
1001	Supply current		V _{CC} =5.25V (Note 3)			12	20	mA
I _{CC2}	Supply current		V _{CC} =5.25V (Note 4)			10	17	mA

All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with $\overline{D_7}$ and \overline{E} at 0V and with all other inputs open.

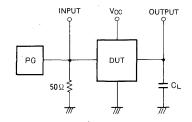
Note 4: I_{CC2} is measured with all inputs open.

8-LINE TO 3-LINE PRIORITY ENCODER

SWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

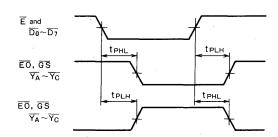
0	•	T		Limits		11.5
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	18	ns
t _{PHL}	time, from inputs $\overline{D_1} \sim \overline{D_7}$ to outputs $\overline{Y_A} \sim \overline{Y_C}$ (levels of delay 2)			14	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D_1} \sim \overline{D_7}$ to outputs $\overline{Y_A} \sim \overline{Y_C}$			15	36	ns
t PHL	(levels of delay 3)			18	29	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	18	ns
t PHL	time, from inputs $\overline{D_0} \sim \overline{D_7}$ to output \overline{EO} (levels of delay 3)	C _L =15pF (Note 5)		24	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D_0} \sim \overline{D_7}$ to output \overline{GS}			31	55	ns
t _{PHL}	(levels of delay 2)			8	21	. ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	25	ns
t _{PHL}	time, from input \overline{E} to outputs $\overline{Y_A} \sim \overline{Y_C}$ (levels of delay 2)			14	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	17	ns
t _{PHL}	time, from input E to output GS (levels of delay 2)			13	36	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output E O			11	21	ns
t _{PHL}	(levels of delay 2)			27	35	ns

Note 5: Measurement circuit



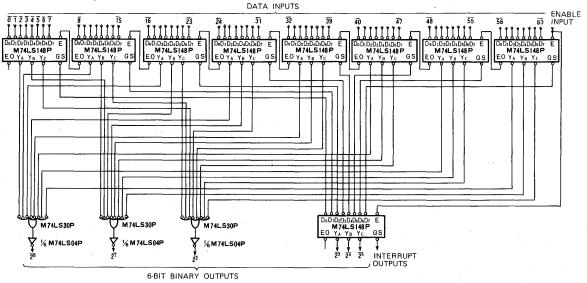
- (1) The pulse generator (PG) has the following characteristics: $PRR=1MHz,\,t_r=6ns,\,t_f=6ns,\,t_w=500ns,\,V_P=3V_{P,P},\,Z_O=50\Omega.$
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

64-line/4-bit binary encoder



Expansion is possible up to 2ⁿ bits in accordance with the above application example.

MITSUBISHI LSTTLS M74LS151P

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS151P is a semiconductor integrated circuit containing an 8-line to 1-line data selector/multiplexer function.

FEATURES

- Strobe input provided
- Complementary output provided
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

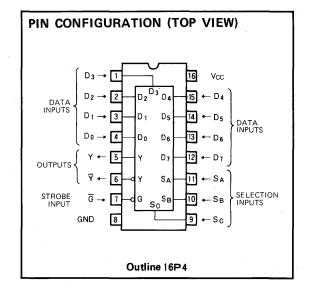
APPLICATION

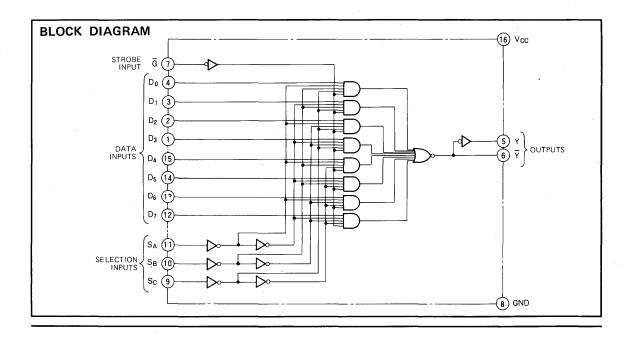
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has a data selector function which provides 1-line selection of 8 input signals and a multiplexer function which converts the 8-bit parallel data into serial data. When 8-line signals are applied to the data inputs and 1 data is specified from among the 8 data from selection inputs S_A , S_B and S_C , the input signal is output at Y and the inverted signal from output \overline{Y} . By applying 8-bit parallel data to $D_0{\sim}D_7$ and connecting a synchronous octal counter output to S_A , S_B and S_C , the data appear in Y in $D_0{\sim}D_7$ order and in \overline{Y} in $\overline{D_0}{\sim}\overline{D_7}$ order as synchronized with the clock pulse. When strobe input \overline{G} is set high, Y is set low and \overline{Y} high.

M74LS151P has the same functions and pin connections as M74LS251P but the latter is provided with 3-state outputs.





8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

FUNCTION TABLE (Note 1)

Sc	SB	SA	G	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	Y	7
. x	X	X	Н	Х	×	×	×	×	×	X	×	L	H
L.	L	Ļ	L	L	×	Х	×	×	×	X	×	L	н
L	L	L	L	Н	×	X	X	X	X	×	×	н	L
L	L	н	. L	×	L	Х	X	×	×	×	×	L	Н
L	L	н	L	×	Н	X	Х	Х	х	X	X	н	L
L	Н	L	. L	×	Х	L	Х	×	Х	х	X	,L	Н
L	н	L	L	×	×	Н	×	×	×	×	×	Н	L
L	н	н	L	×	×	×	L	×	х	х	×	L	I
L	Н	Н	L	×	X	X	Н	×	×	X	×	Н	Γ
ı H	L	L	L	Х	Х	X	×	L	Х	х	×	· L	H
н	L	L	L	Х	Х	Х	Х	Н	Х	X	×	н	L
н	L	н	L	×	×	×	×	×	L	X	×	L	I
Н	L	Н	L	X	×	×	Х	×	Н	X	X	н	L
Н	Н	L	L	X	×	X	×	×	Х	L	X	L	Н
H.	н	L	L	Х	Х	X	Х	Х	Х	Н	Х	н	L
н	Н	Н	L	×	X	×	Х	×	Х	Х	L	L	Н
Н	Н	н	L	Х	X	Х	Х	×	Х	Х	Н	Н	L

Note 1 X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbot	Parameter		11-14			
Symbol	rarameter	Min	Тур	Max	Ųnit	
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
	Low-level output current	V _{OL} ,≤0.4V	0		4	mΑ
loL	Low-level output current	V ₀ L≦0.5V	0		8	mΑ

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

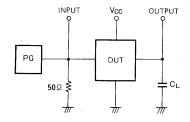
Constant	Parameter	Test cond	litions			Unit	
Symbol	rarameter	rest conc	rest conditions			Max	Unit
ViH	High-level input voltage	7 .		2			V
VIL	Low-level input voltage					0.8	٧
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
	High-level output voltage	V _{CC} =4.75V, V _I =0.8V		2.7	2.4		
∨он	VoH High-level output voltage	V _I =2V , I _{OH} = -400,	$V_1 = 2V \cdot I_{0H} = -400 \mu A$		3.4		V
		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
V_{OL}	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.	7V			20	μА
Іін	nigh-level input current	V _{CC} =5.25V, V _I =10	v .			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V ₁ =0.4	4 V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	/	- 20		- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3) ,		6	10	mA

^{* :} All typical values are at V_{CC} =5V, T_a =25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

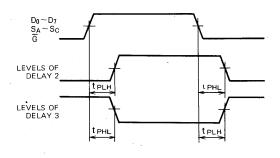
Symbol	Parameter	Total		Limits		11-2-
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	23	ns
tpHL	time, from inputs S_A , S_B , S_C to output \overline{Y}			15	32	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			22	43	ns
tphL	time, from inputs SA, SB, SC to output Y			16	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	·		10	24	ns
tphL	time, from input $\overline{\mathbf{G}}$ to output $\overline{\mathbf{Y}}$	C ₁ = 15 pF (Note 4)		14	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL TSPF (Note 4)		21	42	ns
t _{PHL}	time, from input G to output Y			16	32	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	21	ns
t _{PHL}	time, from inputs $D_0 \sim D_7$ to output \overline{Y}			8	20	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	1		17	32	ns
tpHL	time, from inputs D ₀ ~D ₇ to output Y	·		12	26	ns

Note 4: Measurement circuit



- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P, P, Z_O = 50Ω.
- (2) CL includes probe and jig capacitance.

TIMING DIAGRAM (Reference=1.3V)



Note 2: All measurements should be done quickly.

Note 3: I_{CC} is measured with all inputs at 4.5V

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS153P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits.

FEATURES

- Strobe inputs provided independently for each circuit
- Selection inputs common to both circuits
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

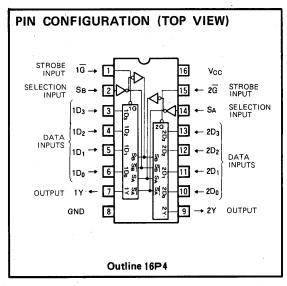
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 2-line to 1-line selection of 4 pairs of input signal using two multiplexer circuits which convert the 4-bit parallel data into serial data with time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 and 1 data is specified from among the data by selection inputs S_A and S_B , the input signal is output at Y. By applying 4-bit parallel data to D_0 , D_1 , D_2 and D_3 , and connecting a synchronous divide-by-4 counter output to S_A and S_B , the D_0 , D_1 , D_2 and D_3 data appear in the order of D_0 , D_1 , D_2 and D_3 synchronized with the clock pulse. S_A and S_B are common to both circuits while strobe inputs $1\overline{G}$ and $2\overline{G}$ are independent. When $1\overline{G}$ and $2\overline{G}$ are set high, 1Y and 2Y are set low irrespective of the status of the input.

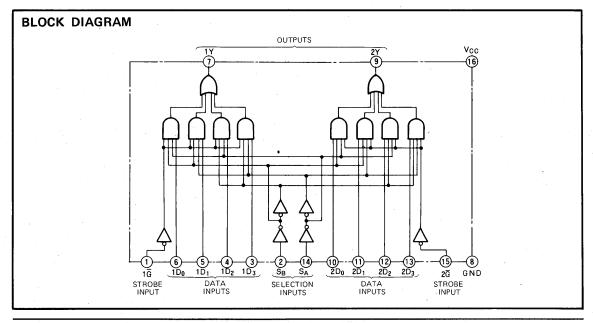
M74LS153P has the same functions and pin connections as M74LS253P but the latter is provided with 3-state outputs.



FUNCTION TABLE (Note 1)

S _B	SA	. D0	D ₁	D ₂	D ₃	G	Υ
×	Х	Х	Х	×	X	Н	١
L	L	L	×	×	×	L	L
L	L	Н	Х	×	×	L	н
L	H	×	L	×	×	L	L
L	Н	×	н	×	×	L	Ħ
Н	L	×	×	L	×	L	L
Н	L	×	.×	н.	×	L	Н
Н	н	х	Х	×	L	· L.	L
Н	н	X	Х	Х	Н	L	H

Note 1 X: Irrelevant



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5∼ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°°

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

	Parameter			Limits				
Symbol				Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Пон	High-level output current	V _{OH} ≥2.7V	0		-400	μА		
	Low-level output current	V _{OL} ≤0.4V	0		4	mA		
lor	Low-level output current	V _{OL} ≤0.5V	0		- 8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

	6	T	Mat			Unit	
Symbol	Parameter	l est cond	Test conditions		Typ *	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage				0.8	V	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1			- 1.5	V	
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.8	V	2.7	3.4		
Vон	VOH High-level output voltage	V _I = 2 V, I _{OH} = -400	$V_1 = 2 V, I_{OH} = -400 \mu A$		3.4		, V
· .	Low-level output voltage	V _{CC} = 4.75V	I _{OL} = 4 mA		0.25	0.4	٧
VoL	Low-level output vortage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μА
Iн	High-level input current	$V_{CC} = 5.25V, V_I = 10V$,			0.1	mA
h _L	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 \	/ .	- 20		— 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			6.2	10	mA

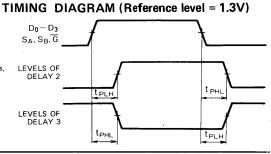
^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, Ta=25%, unless otherwise noted)

Cumbal	Daramatan	Test conditions		Unit		
Symbol	Parameter	rest conditions	Min	Тур	Max	Offic
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	15	ns
t _{PHL}	time, from inputs $D_0 \sim D_3$ to output Y			12	26	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	29	ns
tehl	time, from inputs SA, SB to output Y	C _L =15pF		13	38	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 4)		12	24	ns
t _{PHL}	time, from input $\overline{\mathbf{G}}$ to output \mathbf{Y}			12	32	ns

Note 4: Measurement circuit

INPUT VCC OUTPUT (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6$ ns, $t_f = 6$ ns, $t_w = 500$ ns, $v_P = 3v_{P,P}$, $Z_O = 50\Omega$. (2) CL includes probe and jig capacitance.



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS155P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers.

FEATURES

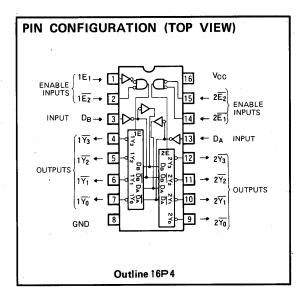
- Low output impedance
- Enable inputs provided
- 8-bit output decoder/demultiplexer functions are provided without the use of external components
- Wide operating temperature range (T_a = -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

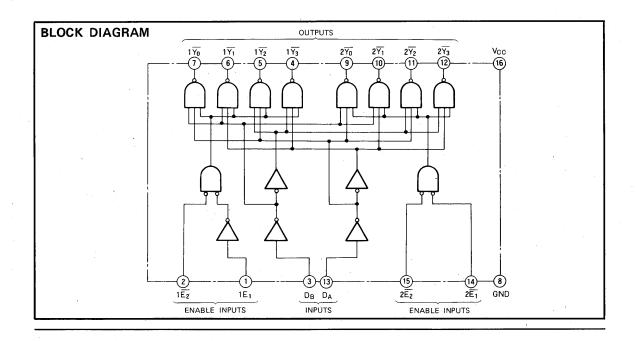
FUNCTIONAL DESCRIPTION

When a 2-bit binary number is decoded in quaternary numbers and the 2-bit binary number is applied to inputs D_A and D_B , the corresponding $\overline{Y_0} {\sim} \overline{Y_3}$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2\overline{E_1}$ are kept high and low, respectively, and enable inputs $1\overline{E_2}$ and $2\overline{E_2}$ are kept low. When $1\overline{E_2}$ and $2\overline{E_2}$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2\overline{E_2}$ are connected and by applying the third bit binary number, the outputs appear in $2\overline{Y_0} {\sim} 2\overline{Y_3}$ and $1\overline{Y_0} {\sim} 1\overline{Y_3}$, in accordance with the function table.



For use as a 1-line to 4-line demultiplexer, the outputs appear in $\overline{Y_0} \sim \overline{Y_3}$ by making $1E_1$ and $2\overline{E_1}$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $2\overline{E_1}$ are connected to make them the third bit selection input and $1\overline{E_2}$ and $2\overline{E_2}$ are connected to make the data inputs so that the outputs appear in $2\overline{Y_0} \sim 2\overline{Y_3}$ and $1\overline{Y_0} \sim 1\overline{Y_3}$.

M74LS155P has the same functions and pin connections as M74LS255P but the latter is provided with open collector outputs.



DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line to 4-line demultiplexer)

Dв	D_A	1Ē2	1E 1	1 7 0	1 V 1	1Y2	1 7 3
Х	Х	Η	Х	Ϊ	Н	Н	Н
١	L	L	H	L	Н	Н	Н
L	Н	Ļ	н	Н	L	Н	Н
Н	L	L	н	н	Н	L	Н
Н	Н	L	Н	Н	Н	Н	L
Х	х	X	L	Н	Н	Н	Н

	DΒ	D_A	2Ē2	2E ₁	2Ÿ0	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$
	X	Х	Н	Х	Ι	Н	Н	I
i	L	L	L	Ĺ	J	Н	Н	Η
1	١	Η	L	Ţ.	Ι	L	Н	I
	н	L	L	L	Ħ.	H	L	н
	Ι	Н	L	L	Ι	Н	Н	Г
į	×	Х	Х	Н	Ι	Н	Н	н

(3-bit binary to 8-line decoder/1 line to 8-line demultiplexer)

Dc	D _B	D_{A}	E	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$	$1\overline{Y_0}$	$1\overline{Y_1}$	$1\overline{Y_2}$	1 Y 3
Х	Х	Х	Ι	Ξ	Η,	Η	Н	Н	Н	н	Н
J	∟	L	٦	L	Н	Ĥ	Н	н	Ħ	Н	Н
١	∟	Η	٦	Н	L	Н	Н	Н	Ħ	н	Н
٦	Н	L	Γ	н	н	L	Н	Н	н	н	Н
٦	Н	Н	Γ	Н	н	Н	L	Н	H	Н	Н
н	L	L	Г	н	н	Ħ	Н	L	н	н	н
Н	L	н	L	Н	Н	Н	Н	Н	L	Н	Н
Η	Н	L	L	Н	Н	Н	н	Н	Н	L	Н
Н	Н	Н	L	Н	Н	н	н	Н	Н	Н	Ľ

Note 1 X : Irrelevant

 D_C : Pin connecting $1E_1$ and $2\overline{E_1}$ E: Pin connecting 1E2 and 2E2

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 \,^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~ +75	℃ .
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

				Limits				
Symbol	Paramete	er	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≥2.7V	. 0		-400	μΑ		
		V _{OL} ≦0.4V	0		4	mΑ		
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

0 1 1	D	Total condi	*!		Limits		11-14
Symbol	Parameter	Test condi	tions	Min	Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage				0.8	V	
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1			- 1.5	V	
V _{OH}	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu$	2.7	3.4		V	
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	Low-level output vortage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V V _I =2.7V				20	μΑ
l _{iH}	High-level input current	V _{CC} = 5.25V V _I = 10V				0.1	mA
Iд	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _C =0V		-20		- 100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			6.1	10	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

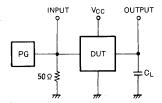
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time Note 3: I_{CC} is measured with inputs $1\overline{E_2}$, $2\overline{E_1}$ and $2\overline{E_2}$ at 0V and with D_A, D_B and $1E_1$ at 4.5V

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

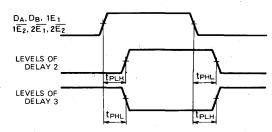
Constant	Parameter		Test conditions			Unit		
Symbol	Farameter		rest conditions	Min	Тур	Max	Oline	
tpLH		delay gate stages				8	15	ns
t _{PHL}	Low-to-high-level, high-to-low-level	2	The second secon			15	30	ns
t _{PLH}	output propagation time, from inputs D_{Δ} , D_{B} to outputs $\overline{Y_{0}} \sim \overline{Y_{3}}$	delay gate stages				10	26	ns
t _{PHL}	7 7 7 7 7 7	3	0 -45-5 (N4)			15	- 30	ns
tpLH	Low-to-high-level, high-to-low-level ou	tput propagation	C _L = 15 pF (Note 4)	,		8	15	ns
t _{PHL}	time, from inputs 1E2, 2E1, 2E2 to	outputs $\overline{Y_0} \sim \overline{Y_3}$. 11	30	ns
tpLH	Low-to-high-level, high-to-low-level ou	tput propagation		•		17	27	ns
t _{PHL}	time, from input 1E ₁ to outputs 1Y ₀	~ 1 √ 3				15	27	ns

Note 4: Measurement circuit



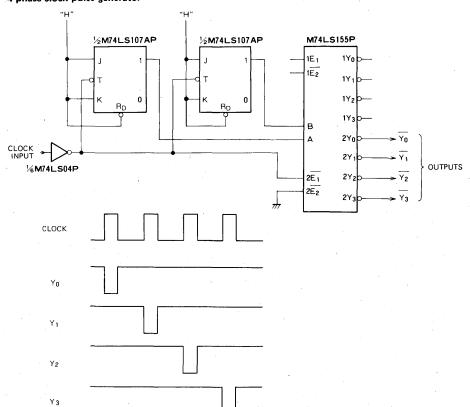
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_Q =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-phase clock pulse generator



M74LS156P

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS156P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers with open collector outputs

FEATURES

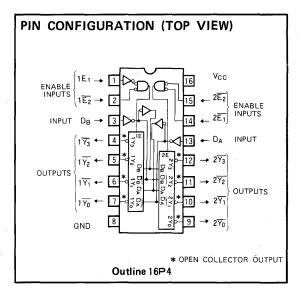
- Usable in AND Tie connection
- Enable inputs provided
- 8-bit output decoder/demultiplexer function is provided without the use of external components
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

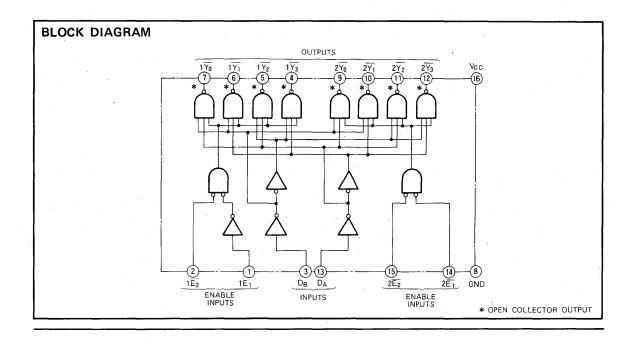
FUNCTIONAL DESCRIPTION

When a 2-bit binary number is decoded as a quaternary number and the 2-bit binary number is applied to inputs D_A and D_B , the corresponding $\overline{Y_0} {\sim} \overline{Y_3}$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2\overline{E_1}$ are kept high and low, respectively, and enable inputs $1\overline{E_2}$ and $2\overline{E_2}$ are kept low. When $1\overline{E_2}$ and $2\overline{E_2}$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2\overline{E_2}$ are connected and by applying the third bit binary number to them, the outputs appear in $2\overline{Y_0}{\sim}2\overline{Y_3}$ and $1\overline{Y_0}{\sim}1\overline{Y_3}$, in accordance with the function table.



For use as a 1-line to 4-line demultiplexer, the outputs appear in $\overline{Y_0} \sim \overline{Y_3}$ by making $1E_1$ and $2\overline{E_1}$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $1\overline{E_1}$ are connected to be made the third bit selection input and $1\overline{E_2}$ and $2\overline{E_2}$ are connected to be made the data inputs so that the outputs appear in $2\overline{Y_0} \sim 2\overline{Y_3}$ and $1\overline{Y_0} \sim 1\overline{Y_3}$.

M74LS156P has the same functions and pin connections as M74LS155P but the latter is provided with active pull-up resistor outputs.



DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line to 4-line demultiplexer)

D_B	D_A	1E ₂	1E ₁	1Y0	1 7 1	1Y2	1 Y 3
Х	Х	Н	Х	Ι	Н	Н	Η
L	L	L	Η	١.	Н	н	н
L	Н	L	Н	Ι	L	Н	Η´
Н	٦	∟	I	Η	Н	٦	н
Н	Ι	L	Н	Ι	Н	I	┙
Х	X	Х	L	I	Н	Ξ	Н

DΒ	DA	2E2	2E ₁	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$
Х	X	Н	X	Ι	н	Н	Н
١	L	L	Γ	١	Н	н	н
∟.	Н	L	٦	Ι	L	Н	Н
Ι	L	L	L	I	Ι	L	н
Ι	Н	L	L	Η	Н	Н	L
×	Х	Х	Н	Ι	I	Н	Н

(3-bit binary to 8-line decoder/1 line to 8 line demultiplexer)

Dс	Dв	DΔ	Ē	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$	1 Y 0	$1\overline{Y_1}$	1Ŷ2	1 Y 3
Х	Х	Х	I	Ι	Н	н	Н	Н	Н	Н	Ι
L	٦	٦	٦	L	н	н	Η	Η	н	н	I.
L	L	Н	L	Н	L	Н	Н	Η	Н	н	Η
L	Н	L	L	Η	н.	L	Н	Н	н	н	н
L	Η	Н	L	Н	н	Н	L	Н	Ι	н	Ι
Н	L	L	L	Η	H	н	Н	٦	Н	н	Η
Н	L	I	L	Н	Н	Н	Н	Ħ	L	н	I
Н	Τ	L	L	Η	Н	Н	Ι	Η	Н	L	Н
Н	π	н	L	Η	Н	Н	Ξ	Ή	Η	Η	L

Note 1 X : Irrelevant

 D_C : Pin connecting $1E_1$ and $2\overline{E_1}$ \overline{E} : Pin connecting $1\overline{E_2}$ and $2\overline{E_2}$

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5-+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

0	Parameter			Limits			
Symbol	raramet	i alametei			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _O =5.5V	0		100	μА	
	OL Low-level output current	V _{OL} ≤0.4V	0		4	mA	
10L		V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75 °C, unless otherwise noted)

Complete		Tout and	Test conditions		Limits		
Symbol	Parameter	rest cond			Typ *	Max	Unit
ViH	High-level input voltage	`		2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} = - 18mA			- 1.5	V
I _{OH}	High-level output current	$V_{CC}=4.75V, V_{I}=0.8$ $V_{I}=2V, V_{O}=5.5V$	$V_{CC}=4.75V, V_1=0.8V$ $V_1=2V, V_0=5.5V$			100	μΑ
, Vol	Low-level output voltage	$V_{CC} = 4.75V$ $V_{I} = 0.8V, V_{I} = 2V$	I _{OL} =4mA		0.25	0.4	V
	High level is put oursest	V _{CC} =5.25V, V _I =2.7			0.33	20	<u>μ</u> Α
liH	High-level input current	V _{CC} =5.25V, V _I =10V	V _{CC} =5.25V, V _I =10V			0.1	mA
THE .	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mA
Icc	Supply current	V _{CC} =5.25V (Note 2)			6.1	10	mA

* : All typical values are at V_{CC}= 5V, T_a= 25°C.

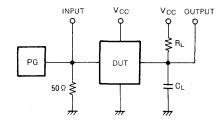
Note 2: I_{CC} is measured with inputs $1\overline{E_2}$, $2\overline{E_1}$ and $2\overline{E_2}$ at 0V and with D_A , D_B and $1E_1$ at 4.5V

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

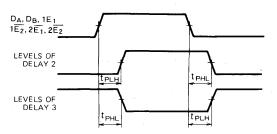
	Parameter [*]		. Test conditions	Limits			Unit
Symbol			rest conditions	Min	Тур	Max	Oilit
t _{PLH}		delay gate stages			18	40	ns
t _{PHL}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A , D_B to outputs $\overline{Y_0} \sim \overline{Y_3}$	2			18	51	ns
t _{PLH}		delay gate stages	$R_1 = 2k\Omega$		20	46	ns
t _{PHL}		3	$C_1 = 15pF$		18	51	ns
tpLH	Low-to-high-level, high-to-low-level or	utput propagation	(Note 3)	,	16	40	ns
t _{PHL}	time, from inputs 1E2, 2E1, 2E2 t	to outputs $\overline{Y_0} {\sim} \overline{Y_3}$	(Note 3)		20	51	ns
telh	Low-to-high-level, high-to-low-level or	utput propagation			20	48	ns
t _{PHL}	time, from input 1E $_1$ to outputs $1\overline{Y}_0$	$\sim 1\overline{Y_3}$			25	48	ns

Note 3: Measurement circuit



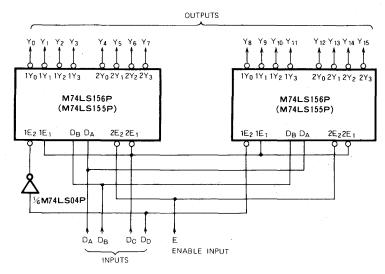
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-bit binary/hexadecimal decoder/demultiplexer



M74LS157P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

DESCRIPTION

The M74LS157P is a semiconductor integrated circuit containing four 1-line to 2-line data selector/multiplexer circuits.

FEATURES

- Common strobe input for all 4 circuits
- Common select input for all 4 circuits
- · Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

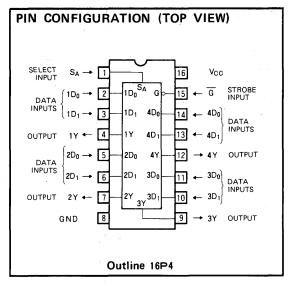
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has 4 circuits, each of which has a data selection function which selects one-line out of a 2-line signal and a multiplexing function to convert 2-bit parallel data into serial data by time sharing. When 2-line signals are fed to at inputs D_0 and D_1 and one of these is specified by the selection input S_A , the specified input signal is selected taken from output Y. The S_A and strobe inputs are common to all 4 circuits. When \overline{G} is high, all the outputs, 1Y, 2Y, 3Y, and 4Y are low, regardless of the inputs.

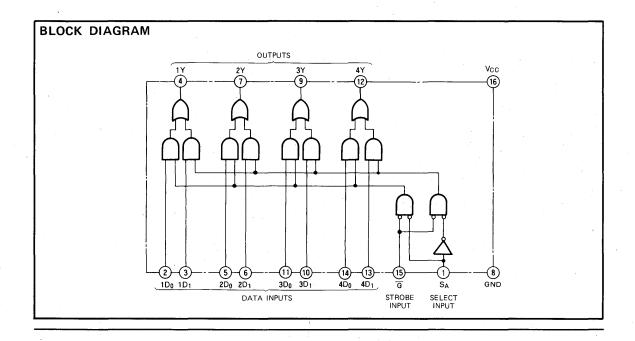
M74LS157P has the same functions and pin connections as M74LS257P but the latter is provided with 3-state outputs,



FUNCTION TABLE (Note 1)

G	SA	D ₀	D ₁	Υ
Н	×	×	×	L
L	L	L	×	L
L	L	Н	Х	Н
L	н	Х	L	L
L	Н	Х	Н	Н

Note 1: X: irrelevant



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5 ~ V _{CC}	v
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65-+150	င

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter					
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

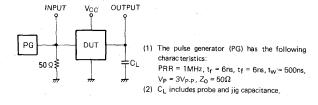
ELECTRICAL CHARACTERISTICS (Ta = −20~ +75°C, unless otherwise noted)

Symbol	Paramete	_	T	Test conditions		Limits		Unit	
Symbol	Paramete	r	l est cond	itions	Min	Typ*	Max	Onit	
ViH	High-level input voltage				2			V	
VIL	Low-level input voltage			•			0.8	V	
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			~ 1.5	V	
	Ulinto Inc. of a second include		V _{CC} =4.75V, V _I =0.8	V	2.7	3.4			
VoH	High-level output voltage		$V_1 = 2V$, $I_{OH} = -400 \mu A$		2.7	3.4		\ \	
1/-	VoL Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V	
VOL			$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V	
		D ₀ , D ₁	V _{CC} =5.25V	V _{CC} =5.25V			20	μΑ	
	High-level input current	SA, G	V₁=2.7V		40		40		
Iн	High-level input current	D ₀ , D ₁	V _{CC} =5.25V				0.1	^	
		SA, G	V _i =10V				0.2	mA	
lu.	Low lovel input surrent	D ₀ , D ₁	V _{CC} =5.25V				-0.4		
'11_	Low-level input current	Low-level input current SA, G	V₁=0.4V				-0.8	mA	
los	Short-circuit output current (I	Note 2)	V _{CC} =5.25V, V _O = 0 V		20		- 100	m A	
lcc	Supply current		V _{CC} =5.25V (Note 3)			9.7	16	mΑ	

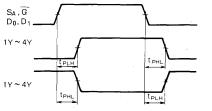
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
	Taranster	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	14	ns
t _{PHL}	time, from input D ₀ , D ₁ to output Y			9	14	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			11	23	ns
tehl	time, from input SA to output Y			14	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		12	20	ns
tphL	time, from input G to output Y			12	21	ns

Note 4: Measurement circuit



TIMING DIAGRAM (Reference level = 1.3V)



f * : All typical values are at V_{CC} = 5V, Ta = 25°C. Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 4.5V.

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

DESCRIPTION

The M74LS158P is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits.

FEATURES

- Converted outputs provided
- Strobe inputs provided independently for each circuits
- Selection inputs common to four circuits
- Low output impedance
- Wide operating temperature range (T_a=-20~+75°C)

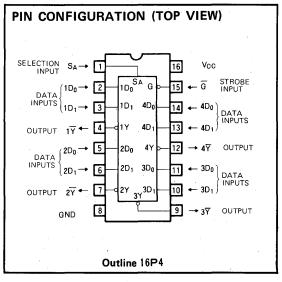
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 2-line to 1-line selection for 4 pairs of signals using four multiplexer circuits which convert the 2-bit parallel data into serial data with time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1 and 1 data is specified from among the data from selection input S_A , the input signal is inverted and can be output at \overline{Y} . By applying 2-bit parallel data to D_0 and D_1 , and connecting a binary counter output to S_A , the D_0 and D_1 data are inverted and appear in the order to D_0 and D_1 synchronized with the clock pulse. S_A and strobe input \overline{G} are common to all four circuits. When \overline{G} is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are set high irrespective of the status of the inputs.

M74LS158P has the same functions and pin connections

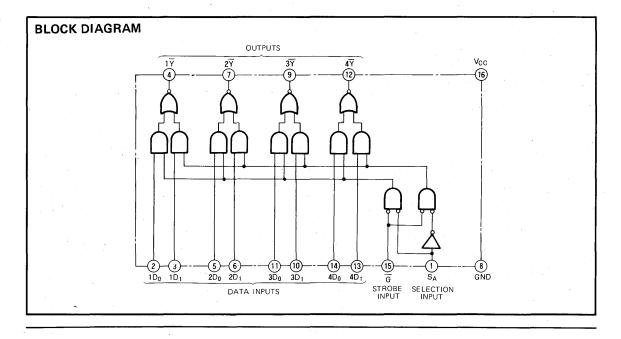


FUNCTION TABLE (Note 1)

G	SA	Dο	D ₁	Ÿ
н	Х	Х	Х	Н
L	L	L	Х	Н
L	L	Н	X	L
L	Н	Х	L	Н
L	н	X -	н	L

Note 1 X: Irrelevant

as M74LS258P but the latter is provided with 3-state outputs,



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		−20~+75	℃
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 - +75 %, unless otherwise noted)

Symbol	Parameter			Unit		
Symbol	ratameter				Max	Unit
V _{CC}	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μА
, .		V _{OL} ≤0.4V	0		4	mΑ
1 OL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Paramete		Test condi			Limits		44.55
Symbol	raramete	31	rest condi	Test conditions		Typ ★	Max	Unit
VIH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage	Low-level input voltage		,			0.8	V
Vic	Input clamp voltage	Input clamp voltage		8mA			- 1.5	V
\/.	High-level output voltage		V _{CC} =4.75V, V _I =0.8	V	2.7			
VoH	High-level output voltage		$V_1 = 2V$, $I_{OH} = -400\mu$	$V_1 = 2V$, $I_{OH} = -400 \mu A$		3.4		٧,
\/-	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		D ₀ , D ₁	V _{CC} =5.25V				20	
1	High-level input current	SA, G	V _I =2.7V			-	40	μΑ
Іін	riiginieveriiipat current	D ₀ , D ₁	V _{CC} =5.25V				0.1	
		SA, G	V ₁ = 10 V				0.2	mΑ
,	Low-level input current	D ₀ , D ₁	V _{CC} =5.25V				-0.4	mA
l _{IL}	Eow-lever input current	SA, G	V _i =0.4V				-0.8	IIIA
los	Short-circuit output current (f	Note 2)	V _{CC} =5.25V, V _O = 0 V		-20		- 100	mA
Іссн	High level Supply current		V _{CC} =5.25V (Note 3)			4.8	8	mΑ
_lccL	Low-level supply current V _{CC} =5.25V (Note 4)			6.5	11	mA		

^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

SWITCHING CHARACTERISTICS (VCC=5V, Ta=25 $^{\circ}$ C, unless otherwise noted)

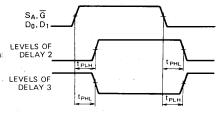
		Total		Unit		
Symbol	Parameter I.	Test conditions	Min	Тур	Max	Oiiit
tpLH	Low-to-high-level, high-to-low-level output propagation			5	12	ns
t _{PHL}	time, from inputs D_0 , D_1 to output \overline{Y}			5	12	ns
tplh	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 5)		9	20	ns ,
t _{PHL}	time, from input SA to output Y			10	24	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			8	17	ns
tphL	time, from input \overline{G} to output \overline{Y}			- 8	18	ns

, Note 5: Measurement circuit

INPUT Vcc OUTPUT PG DUT CL (1)

(1) The pulse generator (GP) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_P .P, Z_O = 50 Ω .

(2) CL includes probe and jig capacitance.



TIMING DIAGRAM (Reference level = 1.3V)

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time. Note 3: Icc is measured with all inputs at 4.5V.

Note 4: The supply current should be measured with $1D_0\sim4D_0$ at 4.5V and the other inputs at 0V.

DESCRIPTION

The M74LS160AP is a semiconductor integrated circuit containing a presettable synchronous decade counter function with a direct reset input.

FEATURES

- Direct reset and synchronous preset inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

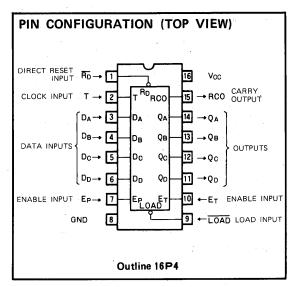
FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input T, the number of count pulses appears as a BCD code in the outputs Q_A , Q_B , Q_C and Q_D synchronized with the count pulse. Counting is done when T changes from low to high.

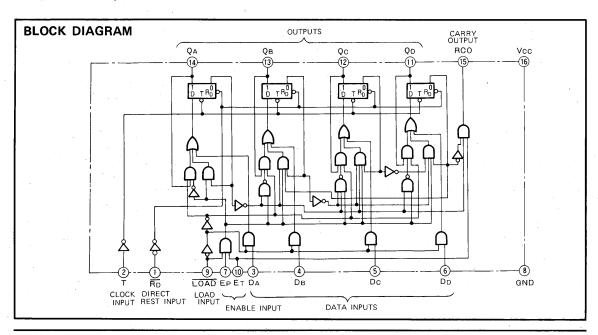
Presetting is performed to synchronize the count pulse. When data are applied to the data inputs D_A , D_B , D_C and D_D , the load input \overline{LOAD} is made low and T is changed from low to high, the signals D_A , D_B , D_C and D_D appear at the Q_A , Q_B , Q_C and Q_D outputs, respectively, regardless of the status of enable inputs E_P and E_T , thereby presetting the counter.

When the counter is preset to a numerical value of 10 or more, counting proceeds in accordance with the status transition diagram.

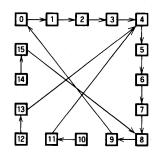
Resetting is asynchronous. Q_A , Q_B , Q_C and Q_D are set low by setting direct reset input $\overline{R_D}$ low, regardless of the status of the other inputs.



Carry output RCO is high only when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. E_P , E_T and RCO are used for synchronous counter cascade connection and for configuration of a divide-by- 10^n counter. (Refer to the application examples.)



STATE DIAGRAM



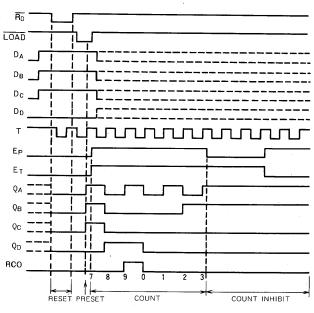
FUNCTION TABLE (Note 1)

RD	LOAD	ΕT	Еρ	T	QΔ	Qв	Qc	QD	RCO				
L	Х	Х	Х	X	٦	L	L	L	Γ				
Н	L	L	X	1								n-	Г
Н	L	н	Х	1	DA	DB	Dc	D _D	L*				
Н	н	н	Н	1		L*							
Н	н	L	Х	X	Inhibit				L				
Н	н	H	L	Х	Inhibit				L*				

Note 1. \uparrow : Transition from low to high (positive edge trigger)

X : Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	٧
. Vi	Input voltage		-0.5~+15	1 V
· Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter			Limits				
Symbol	, raidinetes		Min	Тур	Max	Unit			
Vcc	Supply voltage		4.75	5	5.25	V			
ЮН	High-level output current	V ₀ ≥2.7V	0		-400	μА			
I _{OL} Low-level output current	Low land output ourrent	V _{OL} ≦0.4V	0		4	mA			
	V _{OL} ≤0.5V		0		8	mA			

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Complete			Test condi	tions		Limits		11-1-
Symbol	Parame	ter	rest condi	tions	Min	Typ∗	Max	Unit
ViH	High-level input voltage				2			٧
VIL	Low-level input voltage	w-level input voltage					0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA		-	-1.5	٧
V _{OH}	High-level output voltage	High-level output voltage		BV A	2.7	3.4		٧
	Low-level output voltage		V _{OC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V. V _I =2V	I _{OL} =8mA		0.35	0.5	V
		DA, DB, DC, DD, EP					20	
		LOAD, T, ET	V _{CC} =5.25V, V _I =2.7V				40	μA
	High-level input current	RD	1			20	l	
, liH	High-lever input corrent	DA, DB, DC, DD, EP					0.1	
		LOAD, T, ET	V _{CC} =5.25V, V _I =10\	/			0.2	mA.
		R _D	1			0.1		
-		Da, DB, Dc, DD, Ep					-0.4	
1 ₁ L	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4	IV			-0.8	mA
		RD	1				-0.4	
los .	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mΑ
Іссн	Supply current, all outputs h	igh	V _{CC} =5.25V (Note 3)			18	31	mA
ICCL	Supply current, all outputs lo	w ·	V _{CC} =5.25V (Note 4)			19	32	mA

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions			Unit	
Symbol	Tarafrictor	rest conditions	Min	Тур	Max	Oint
f _{max}	Maximum clock frequency		25	5 5		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation time,			20	35	ns
t PHL	from input T to output RCO			20	35	ns
t _{PLH}	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t PHL	(when \overline{LOAD} is high), from input T to outputs Q_A , Q_B , Q_C , Q_D	$C_L = 15pF$		16	27	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns
t PHL	(when \overline{LOAD} is low), from input T to outputs Q_A , Q_B , Q_C , Q_D			16	27	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time,			8	14	ns
t _{PHL}	from input E _T to output RCO			8	14	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ outputs Q_A , Q_B , Q_C , Q_D	V		1.5	28	ns

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

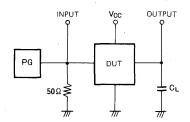
Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	lest conditions	Min	Тур	Max	
t _{W(TH)}	Clock input T high pulse width		25	7		ns
t _{W(TL)}	Clock input T low pulse width		25	6		ns
tw(RD)	Direct reset RD pulse width		20	6		ns
tr	Clock pulse rise time			400	- 100	ns
t _{SU(D)}	Setup time DA~DD to T		20	3		ns
t _{SU(LOAD}	Setup time LOAD to T (Note 8)		20	6		ns
t _{SU(E)}	Setup time Ep, ET to T		20	-8		ns
t _h (D)	Hold time D _A ~D _D to T		3	0		ns
th(LOAD)	Hold time LOAD to T (Note 8)		3	- 3		ns
t _{h(E)}	Hold time Ep, ET to T		3	3		ns
trec(R₀)	Recovery time RD to T		15	6		ns

Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CCH} is measured with D_A, D_B, D_C, D_D, E_P, E_T, and R_D at 4.5V, LOAD at 0V, and T set from 0V to 4.5VA

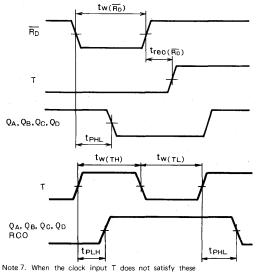
Note 4. I_{CCL} is measured with D_A, D_B, D_C, D_D, E_P, E_T and R_D, LOAD at 0V and T set from 0V to 4.5V.

Note 5. Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



Note 7. When the clock input T does not satisfy these standards, an incorrect counting operation may result.

Note 8. When the load input TOAD setup time and hold time are not satisfied, the incorrect data may be preset. (When LOAD changes within ±5ns of the TOAD input transition from low to high, presetting may be made to low when the data input is high.)

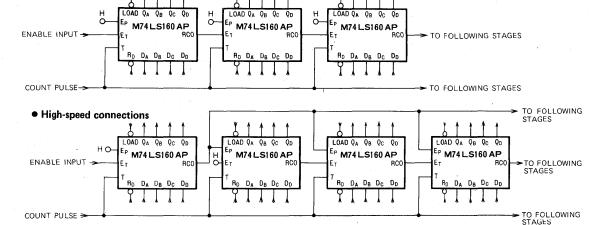
Ет .RCO **t**PLH tphi DA, DB, DC, DD LOAD th(D) t_{su(D)} t_{su(D)} th(D) tsu(LOAD) th(LOAD) tsu(LOAD) th(LOAD) Ep, ET $t_{su(E)} t_{h(E)}$ tsu(E) th(E) Note 6. The shaded areas indicate when the input is per-

Note 6. The shaded areas indicate when the input is permited to change for predictable output performance.

APPLICATION EXAMPLE

Cascade-connected divided-by-10ⁿ counter

Low-speed connections



M74LS161AP

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

DESCRIPTION

The M74LS161AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with direct reset input.

FEATURES

- Direct reset and synchronous preset inputs
- Enable input and carry output for cascaded operation
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20 ~ 75°C)

APPLICATION

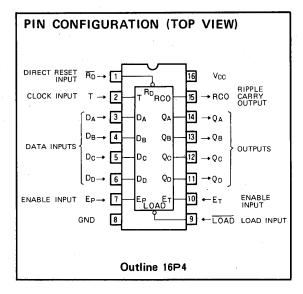
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPITON

When a counting pulse is applied to the T input, the 4-bit binary representation of the count is output at Q_A , Q_B , Q_C and Q_D in synchronization with the count pulse. Counting is done on the transition of the T input signal from low to high.

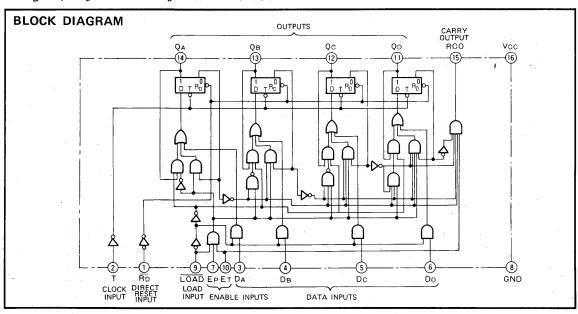
Presetting is accomplished in synchronization with the counting pulse. When preset data is applied to the $D_A,\,D_B,\,D_C$ and D_D inputs, the load input \overline{LOAD} is made low, and T is changed from low to high, this data will appear in the $Q_A,\,Q_B,\,Q_C$ and Q_D outputs, respectively regardless of the status of the enable inputs E_P and $E_T,$ thereby presetting counter.

Resetting is performed asynchronously by setting the direct reset input \overline{R}_D to low at which time the Q_A , Q_B , Q_C and Q_D outputs go to low-level regardless of the states of



the other inputs.

The ripple carry output RCO is high only when all Q outputs and E_T are high. The two enable inputs E_P and E_T and the RCO carry output can be used to form an n-bit synchronous counter by means of cascade connection of several ICs (refer to the application example for the M74LS160AP).



SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

FUNCTION TABLE (Note 1)

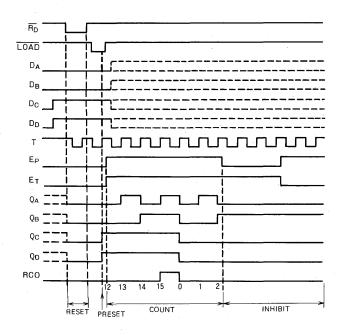
RD	LOAD	Ε _T	EР	Т	QΔ	Qв	Q _C	QD	RCO
L	X	×	Х	×	. L	L	L	L	L
Н	L	L	Х	1	η.	D-	n.	DD	L
н	L	Н	Х	1.	D _A D _B		D _C	00	L*
Н	н	Н	н	1	Cour	it			L*
Н	Н	L	Х	×	Inhibit			Г	
Н	н	Н	L	X	Inhib	oit			L*

Note 1: ↑: Indicates a transition from low to high (positive edge triggering).

* : RCO is normally low but is high when all Q outputs and E_T are high simultaneously, i.e., RCO = Q_A · Q_B · Q_C · Q_D · E_T

V · irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
Vı	Input voltage		-0.5~+15	V	
Vo	Output voltage	High-level state	-0.5~V _{CC}	·V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°C	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	1	Unit			
Symbol	Talametel			Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	1 1	V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol			Test conditi			Limits		
Symbol	Parame	er	rest conditi	ons .	Min	Тур*	Max	Unit .
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} = 4.75V , I _{IC} = -1	8 mA			-1.5	٧
VoH	High-level output voltage	High-level output voltage		V 4	2.7	3.4		V
	Low-level output voltage		V _{CC} = 4.75V	I _{OL} = 4mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V. V _I =2V	I _{OL} = 8mA		0.35	0.5	V
		DA, DB, DC, DD, EP					20	
		LOAD, T, ET	V _{CC} =5.25V, V _I =2.7V	V			40	μΑ
	High-level input current	RD					20	
ин	riginievei impat current	DA, DB, DC, DD, EP					0.1	
		LOAD, T, ET	V _{CC} = 5.25V, V _I = 10V				0.2	mA
		RD	1			0.1		
		Da, DB, Dc, DD, EP			1		-0.4	
IIL	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4V	v			-0.8	mA
	J	RD					-0.4	
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		20	-	- 100	mΑ
Іссн	Supply current, all outputs hi	gh	V _{CC} =5.25V (Note 3)			18	31	mA
Iccl	Supply current, all outputs lo	w	V _{CC} = 5.25 V (Note 4)			19	32	mA

 $[\]boldsymbol{*}$: Typical values are for $V_{CC}\text{=}5V$ and $T_{a}\text{=}25^{\circ}C$

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

$\textbf{SWITCHING} \ \ \textbf{CHARACTERISTICS} \ (V_{CC} = 5V \ , \ T_a = 25^{\circ}C \ , \ \ \text{unless otherwise noted})$

Symbol	Parameter	Test conditions			Unit	
Symbol	· r aranneter	rest conditions	Min	Тур	Max	J
fmax	Maximum clock frequency		25	- 55		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation time,			20	35	ns
t PHL	from input T to output RCO			20	35	ns
t PLH	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t ÞHL	(when \overline{LOAD} is high), from input T to outputs Q_A , Q_B , Q_C , Q_D	C _L = 15pF		16	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns
t _{PHL}	(when LOAD is low), from input T to outputs QA, QB, QC, QD			16	27	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time,			8	14	ns
t PHL	from input E _T to output RCO			8	14	. ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{RD} outputs Q_A , Q_B , Q_C , Q_D			15	28	ns

TIMING REQUIREMENTS (Vcc = 5V. Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Tour one the	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Unit
t _{w(TH)}	Clock input T high pulse width		25	7	,	ns
tw(TL)	Clock input T low pulse width		25	6		ns
tw(RD)	Direct reset RD pulse width		20	6		ns
t _r	Clock pulse rise time			400	100	ns
t _{SU(D)}	Setup time DA~DD to T	•	20	3		ns
t _{SU(LOAD}	Setup time LOAD to T (Note 8)		20	6		ns
t _{SU(E)}	Setup time Ep, ET to T		20	8		ns
t _h (D)	Hold time DA~DD to T		3	0		ns
t _h (LOAD)	Hold time LOAD to T (Note 8)		3	- 3		ns
t _{h(E)}	Hold time Ep, ET to T		3	-3		ns
trec(RD)	Recovery time RD to T		15	6		ns

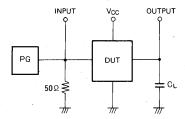
^{3:} Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T and R

at 4.5V and the LOAD input at 0V, changing the T input from 0V to 4.5V.

^{4:} Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T, R_D and LOAD at 0V, changing the T input from 0V to 4.5V.

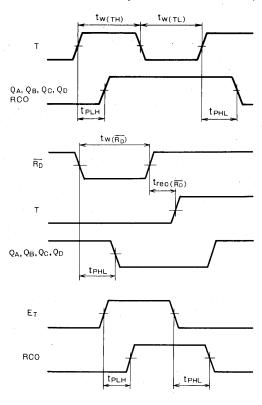
SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

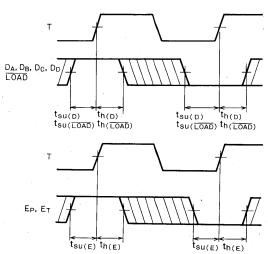
Note 5: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

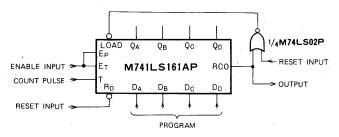
TIMING DIAGRAM (Reference level = 1.3V)





Note 6. The shaded area indicates the period within which switching may take place.

APPLICATION EXAMPLE Programmable divider



Note 7: Reset is performed by applying countpulse with reset input high. $\overline{R_D}$ pin cannot be used since $Q_A \sim Q_D$ should be set low.

Da.	DB	Do	DD	Divide rate
L	L	L	L,	1/16
Н	L	L	L	1/15
ĻL	н	L	Γ	1/14
Н	Н	L	Г	1/13
L	L	Н	٦	1/12
H	L	н	L	1/11
L	Н	н	L	1/10
. н	Η	Н	L	1/9
L	L	L	Η	1/8
Η.	L	L	Ħ	1/7
L	Н	L	Н	1/6
H	Н	L	Η	1/5
L	L	Н	Н	1/4
Н	L	Н	Н	1/3
L	Н	Н.	Н	1/2

DESCRIPTION

The M74LS162AP is a semiconductor integrated circuit containing a synchronous presettable decade counter function with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

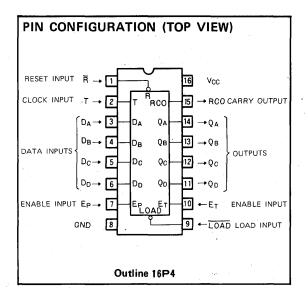
FUNCTIONAL DESCRIPTION

When the count pulses are applied to clock input T, the number of count pulses appears as a BCD code in the outputs Q_A , Q_B , Q_C , Q_D synchronized with the count pulses. Counting is done when T changes from low to high.

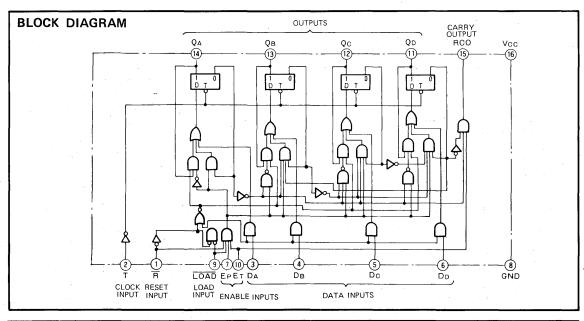
Presetting is performed to synchronize the count pulse. When data are applied to the data inputs D_A , D_B , D_C and D_D , the load input \overline{LOAD} is made low and T is changed from low to high, the signals D_A , D_B , D_C and D_D appear at the Q_A , Q_B , Q_C and Q_D outputs, respectively, regardless of the status of enable inputs E_P and E_T , thereby presetting the counter. When the counter is preset to a numerical value of 10 or more, counting proceeds in accordance with the status transition diagram.

Resetting is synchronized with the count pulses. Q_A , Q_B , Q_C and Q_D are set low by setting reset input \overline{R} low and by changing T from low to high.

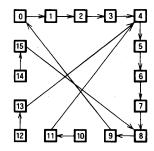
Carry output RCO is high only when QA is high, QB is



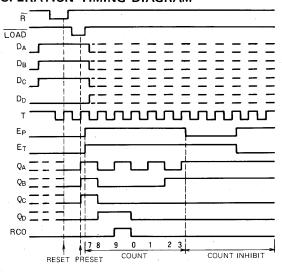
low, Q_C is low, Q_D is high and E_T is high. E_P , E_T and RCO are used for synchronous counter cascade connection and for configuration of an n-bit counter. (Refer to the application examples of the M74LS160AP.)



STATE DIAGRAM



OPERATION TIMING DIAGRAM



FUNCTION TABLE (Note 1)

R	LOAD	Ет	Еp	T	QΔ	Qв	Qc	QD	RCO
L	Х	Х	- X	1	∟	L	L	L	٦
Н	L	L	Х	1	п.	DB	Dc	D-	L
Н	L	Н	X	1	DA	DB	DU	DD	L*
Ĥ	Н	Н	Н	1	Count				∟*
Н	Н	L	Х	Х		Inh	ibit		Γ
Н	Н	Н	L	Χ	Inhibit				∟*

- Note 1 † : Transition from low to high (positive edge trigger)
 - *: RCO is normally low but is high when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. Therefore, RCO = $Q_A \cdot Q_B \cdot Q_C \cdot Q_D$
 - X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = 20 - +75%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
٧ı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	τ
Tstg	Storage temperature range		-65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

		***		Limits		11.7	
Symbol	Parameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
I _{OH}	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ	
		V _{OL} ≦0.4V	0		4	mA	
IOL	Low-level output current VoL≤0.5V		0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	D	Test conditions		Limits				
	Parameter		l est cond.	itions	Min	Тур*	Max	Unit
ViH	High-level input voltage				2			
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} =4.75V, V _I =0. V _I =2V, I _{OH} =-400		2.7	3.4		٧
····	Low-level output voltage		V _{CC} = 4.75V	I _{OL} = 4 mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V.V _I =2V	I _{OL} = 8 mA		0.35	0.5	V
	High-level input current High-level input current DA, DB, DC, DD, EP LOAD, T, ET R DA, DB, DC, DD, EP LOAD, T, ET R	DA, DB, DC, DD, EP					. 20	
		LOAD, T, ET	V _{CC} =5.25V, V _I =2.7V				40	μΑ
		R					40	
ин		DA, DB, DC, DD, EP	V _{CC} =5.25V. V _I =10V				0.1	mA
		LOAD, T, ET					0.2	
			·			0.2		
		Da, DB, Dc, DD, Ep					-0.4	
l _I L	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4V				-0.8	mA
		R]				-0.8	
los	Short-circuit output current	Short-circuit output current (Note 2)			20		– 100	mA
Іссн	Supply current, all outputs h	gh	V _{CC} =5.25V (Note 3)			18	31	mA
ICCL	Supply current, all outputs lo	w	V _{CC} = 5.25 V (Note 4)			19	32	mA

^{* :} All typical values are at Vcc = 5V, Ta = 25°C.

Note 2. All typical values are at VCC = 0V, 1a = 20 C.

Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CCH} is measured with D_A, D_B, D_C, D_D, E_P, E_T, and R

at 4.5V, LOAD at 0V, then 4.5V applied to T input.

Note 4. I_{CCL} is measured with D_A, D_B, D_C, D_D, E_P, E_T and R

to COAD at 0V and T set from 0V to 4.5V.

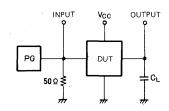
SWITCHING CHARACTERISTICS ($V_{CC}=.5 \text{ V}$, $Ta=25 ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter Test conditions	Limits			Unit	
Symbol	rarametel	l est conditions	Min	Тур	Max	Omit
fmax	Maximum clock frequency		25	55		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			20	35	ns
t PHL				20	35	ns
t pLH	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns
t PHL	(when LOAD is high), from input T to outputs QA, QB, QC, QD	$C_L = 15pF$		16	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns
t PHĽ	(when LOAD is low), from input T to outputs Q _A , Q _B , Q _C , Q _D			16	27	ns
t plh	Low-to-high-level, high-to-low-level output propagation time,			8	14	ns
t PHL	from input E _T to output RCO			8	14	ns

TIMING REQUIREMENT (V_{CC} = 5 V, Ta=25°C, unless otherwise noted)

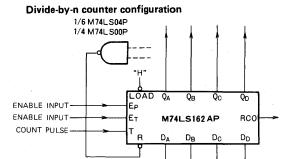
Symbol	Parameter	Test conditions		Limits		
Symbol		rest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input Thigh pulse width		25	7		ns
tw(TL)	Clock input T low pulse width		25	6		ns
tr	Clock pulse rise time			400	100	ns
t _{su(D)}	Setup time DA~DD to T		20	3		ns
tsu(LOAD)	Setup time LOAD to T (Note 8)		20	6		ns
tsu(A)	Setup time R to T		20	11		ns
t _{su(E)}	Setup time Ep, E _T to T		20	8		ns
th(D)	Hold time DA~DD to T		3	0		ns
th(LOAD)	Hold time LOAD to T (Note 8)		3	- 3		ns
th(R)	Hold time R to T		3	- 8	1	ns
th(E)	Hold time Ep, E _T to T		3	- 5	i	ns

Note 5. Measurement circuit



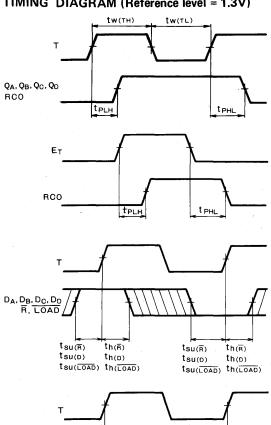
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f ≈ 6ns, t_W = 500ns, $VP = 3V_{P-P}$, $Zo = 50\Omega$.
- (2) C_L includes probe and jig capacitance

APPLICATION EXAMPLES



Divide-by-n counter	Pins connected to gate input
Ternary counter	Qв
Divide-by 5 counter	Qc
Divide-by-6 counter	QA, QC
Divide-by-7 counter	Q _B , Q _C
Divide-by-9 counter	QD

TIMING DIAGRAM (Reference level = 1.3V)



T		
Ep, ET	f//////	\mathcal{I}
tsu(E)	t _{h(E)}	su(E) th(E)

Note 6. The shaded areas indicate when the input is permited to change for predictable output performance.

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS163AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs.
- · Cascade connected enable input and carry output.
- High speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

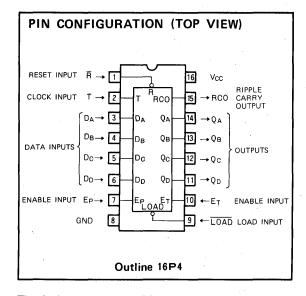
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

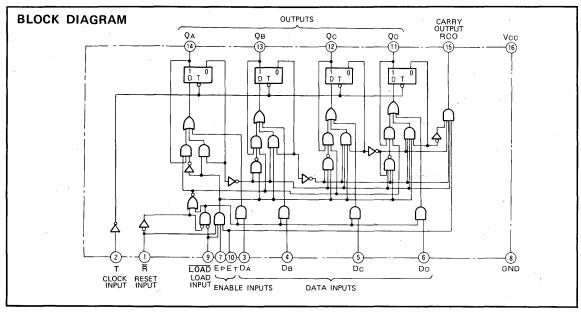
When count pulses are applied to the clock input T, the number of count pulses appears as a 4-bit binary code in the outputs Ω_A , Ω_B , Ω_C , and Ω_D synchronized with the count pulses. Counting is done when T changes from low to high.

Presetting is performed to synchronize the count pulse. When data is applied to the data inputs D_A , D_B , D_C and D_D , the load input \overline{LOAD} is made low, and T is changed from low to high, the signals D_A , D_B , D_C , and D_D appear at the Q_A , Q_B , Q_C , and Q_D outputs, respectively, regardless of the status of the enable inputs E_P and E_T , thereby presetting the counter.

Reset is performed, synchronized with the count pulse. When the reset input \overline{R} is made low, and T is changed from low to high, Q_A , Q_B , Q_C , and Q_D will be low.



The ripple carry output RCO is high only when $Q_A = Q_B = Q_C = Q_D = \text{high and } E_T = \text{high. } E_P, E_T \text{ and RCO}$ are used when the counter is cascade connected in a synchronous manner to from an n-bit counter. (See the M74LS160AP application example).



FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

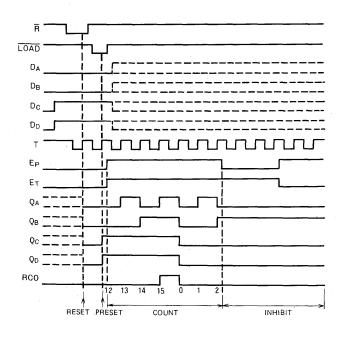
R	LOAD	Ετ	EР	Т	QA.	Qв	Qc	QD	RCO		
L	X	Х	Х	1	L	L	L	L	L		
Н	L	L	X	1					_	η.	L
I	L	Н	X	1	DA	DB	Dc	DD	L*		
Н	Н	Н	н	1	Coun	L*					
Ι	Н	L	×	X	Inhibit				L		
Н	Н	Н	L	X	Inhibit				L*		

Note 1: ↑: transition from low to high level

RCO output is normally low-level, but RCO output is high-level when E_T input is high-level while the counter is in its maximum count state (HHHH).

X : irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5∼+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	· V
Topr	Operating free-air ambient temperature range		-20~+75	℃ .
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol						
Syllibol	Paramet	er	Min	Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mA
lor	Low-level output current	V _{OL} ≦0.5V	0		8	mA

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parame	•••	Test condit	tions	1	Limits		l'
Symbol	Parame .	ter	, rest condit	LIONS	Min	Typ ≭	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	٧
Voн	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-400μ		2.7	3.4	,	٧
	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	.0.4	٧
VoL	Low-level output voltage		V _I =0.8V, V _I =2V	I _{OL} = 8mA		0.35	0.5	٧
		DA, DB, DC, DD, EP				20		
	1	LOAD, T, ET	V _{CC} =5.25V. V _I =2.7V				40	μА
	Mich level in the second	R				40		
I _{IH}	High-level input current	DA, DB, DC, DD, EP	V _{CC} =5.25V, V _I =10V				0.1	mA
		LOAD, T, ET					0.2	
		R					0.2	
		Da, DB, Dc, DD, EP					-0.4	
l _{IL}	Low-level input current	LOAD, T, ET	V _{CC} =5.25V, V _I =0.4	V,			-0.8	mA
	1	R					-0.8	
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V		20		- 100	mA
Госн	Supply current, all outputs hi	gh	V _{CC} =5.25V (Note 3)			18	31	mA
Iccl	Supply current, all outputs lo	w	V _{CC} = 5.25 V (Note 4)			19	32	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: I_{CCH} is measured with D_A, D_B, D_C, D_D, E_T, \overline{R} inputs at 4.5V, LOAD inputg rounded and a momentary ground, then 4.5V, applied to T input. 4: I_{CCL} is measured with D_A, D_B, D_C, D_D, E_T, \overline{R} , LOAD inputs grounded and a momentary ground, then 4.5V, applied to T input.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

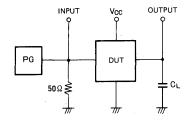
Symbol	Parameter	Test conditions		Limits			
Symbol	a arrieter	rest conditions	Min	Тур	Max	Unit	
f _{max}	Maximum clock frequency		25	55		MHz	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,			20	35	ns	
t PHL	from input T to output RCO			20	35	ns	
t _{PLH}	Lwo-to-high-level, high-to-low-level output propagation time			12	24	ns	
t _{PHL}	(when LOAD is high), from input T to outputs QA, QB, QC, QD	$C_L = 15pF$		16	27	ns	
t PLH	Low-to-high-level, high-to-low-level output propagation time	(Note 5)		12	24	ns	
t PHL	(when LOAD is low), from input T to outputs Q _A , Q _B , Q _C , Q _D			16	27	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,			8	14	ns	
t PHL	from input E _T to output RCO			8	14	ns	

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Task and distant	Limits			Unit
Symbol	rarameter	Test conditions	Min	Тур	Max	
t _{w(TH)}	Clock input T high pulse width		25	7		ns
tw(TL)	Clock input T low pulse width		25	.6		ns
tr	Clock pulse rise time	,		400	100	ns
t _{SU(D)}	Setup time DA~DD to T		20	3		ns
tsu(LOAD)	Setup time LOAD to T (Note 7)	1.	20	6		ns
tsu(R)	Setup time R to T		20	. 11		ns
t _{SU(E)}	Setup time Ep, ET to T		20	8		ns
t _{h(D)}	Hold time $D_A \sim D_D$ to T	1	3	0		ns
th(LOAD)	Hold time LOAD to T (Note 7)	A	3	- 3		ns
t _{h(R)}	Hold time R to T		3	- 8		ns
t _h (E)	Hold time Ep, ET to T		3	- 5		กร

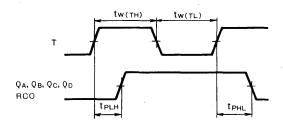
FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

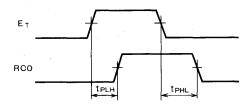
Note 5: Measurement circuit

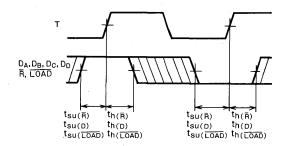


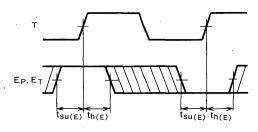
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_{P-P} , Z_O = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





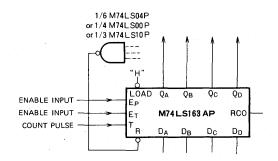




Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Variable modulo counter



Divide rate	Outputs connect to inputs of GATE
. 3	QB
5	Q _C
6	QA. QC
7	Q _B , Q _C
9	Q _D
10	QA, QD
11	Q _B , Q _D
12	QA, QB, QD
13	Q _C , Q _D
14	QA. QC. QD
15	QB, QC, QD

M74LS164P

8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The M74LS164P is a semiconductor integrated circuit containing an 8-bit serial input-serial/parallel output shift register function with direct reset input.

FEATURES

- Serial input-serial/parallel output
- Direct reset input provided
- 8-bit for high space factor
- Input load factor of 1 for each input
- Wide operating temperature range (T_a= −20~+75°C)

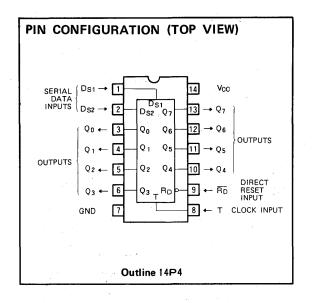
APPLICATION

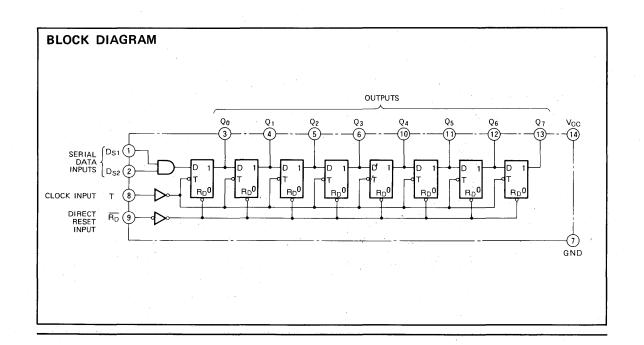
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is configured with 9 D-type edge-triggered flip-flops and the serial data inputs D_{S1} and D_{S2} logic product $D_{S1} \times D_{S2}$ represents the first-stage flip-flop data input. Outputs $Q_0 \sim Q_7$ are taken out from the flip-flop Q outputs. When D_{S1} and D_{S2} are both high and the clock pulse is applied to T, the high signal is shifted in sequence into Q_0 , Q_1 ... Q_7 . When either D_{S1} or D_{S2} or both are low and the clock pulse is applied to T, the low signal is shifted into Q_0 , Q_1 ... Q_7 in sequence. Shifting is performed when T changes from low to high.

When the direct reset input R_D is set low, all the outputs are reset low irrespective of the other input signals. $\overline{R_D}$ should be kept at high when using this device as a shift register.





8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

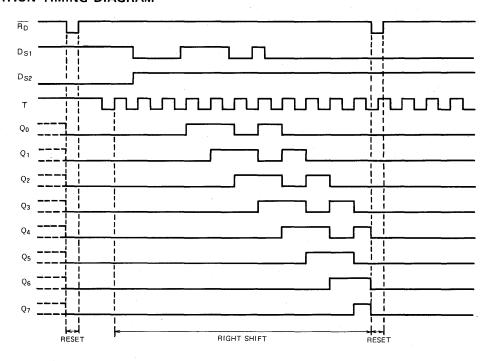
Operational mode	R _D	Т	D _{S1}	D _{S2}	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Reset	L	×	×	×	L	L	L	L	L	L	L	L
	Н	1	L	L	L	Q ₀	Q ₁ 0	Q2 ⁰	Q_3^0	Q ₄ 0	Q ₅ ⁰	Q ₆ 0
Right shift	Н	1	Н	L	L	Q ₀ ⁰	Q ₁ 0	Q_2^0	Q ₃ ⁰	Q_4^0	Q5 ⁰	Q ₆ 0
Night Shift	Н	1	L	н	L.	Q ₀ 0	Q ₁ 0	Q_2^0	Q ₃ ⁰	Q_4^0	Q ₅ ⁰	Q ₆ ⁰
	Н	1	Н	Н	Н	Q ₀ 0	Q ₁ 0	Q_2^0	Q3 ⁰	Q4 ⁰	Q ₅ ⁰	Q ₆ 0

Note 1 ↑: Transition from low to high (positive edge trigger)

Q0: Level of output before the change from low to high

X : irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		−65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet			10-7		
Symbol	raramet	:	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
I _{OL} L		V _{OL} ≦0.4V	0		4	mA
	Low-level output current	0		8	mA	

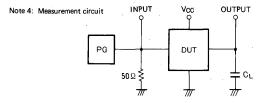
8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

0					11-14		
Symbol	Parameter	lest cond	Test conditions			Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{1C} =-	V _{CC} =4.75V, I _{1C} =-18mA			-1.5	V
VoH	High-level output voltage	"" '	$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-400\mu A$		3.5		V
VoL	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
IIH	High-level input current	V _{CC} =5.25V, V _I =2.	V _{CC} =5.25V, V _I =2.7V			20	μA
'IH	i ngri-level input current	V _{CC} =5.25V, V _I =10	V _{CC} =5.25V, V _I =10V		,	0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	V _{CC} =5.25V, V _I =0.4V		7	-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V _{CC} =5.25V, V _O =0V		_	- 100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)		16	27	mA

SWITCHING CHARACTERISTICS ($V_{CO}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			
Symbol	Farameter	rest conditions	Min	Тур	Max	Unit	
f _{max}	Maximum clock frequency		25	50		MHz	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			13	27	ns	
t _{PHL}	time, from input T to outputs Q ₀ ~Q ₇	C _L =15pF		14	32	ns	
tpHL	Low-to-high-level, high-to-low-level output propagation time, input Rp to outputs Q0 ~ O7	(Note 4)		18	36	ns	

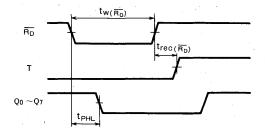


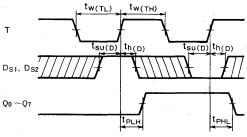
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_{P-P} , Z_0 =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

C	Parameter	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		20	8		ns
tw(TL)	Clock input T low pulse width		20	10		ns
tw(RD)	Direct reset RD pulse width		20	. 9		ns
tsu(D)	Setup time D _{S1} , D _{S2} to T	· ·	15	3		ns
th(D)	Hold time D _{S1} , D _{S2} to T		5	2		ns
trec (RD)	Recovery time RD to T	1	20	-1		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.



^{* :} All typical values are at V_{CC}=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with D_{S1} and D_{S2} at 0V, 4.5V applied to T after $\overline{R_D}$ has been set from 0V to 4.5V.

M74LS165AP

8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

DESCRIPTION

The M74LS165AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input — serial output shift register function.

FEATURES

- Parallel-to-serial data conversion
- Direct overriding load (data) input
- Clock inhibit input
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment

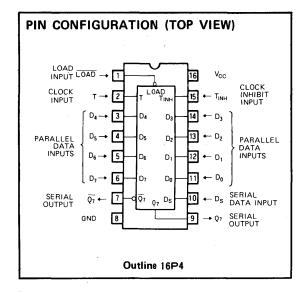
FUNCTIONAL DESCRIPTION

This device is configured from eight R-S-T flip-flop circuits and is designed to accept serial data input through $D_{\rm S}$, or parallel data input through $D_0 \sim D_7$.

When D_S is used as the input, a clock pulse is applied to clock input T when load input \overline{LOAD} is high-level and the clock inhibit input T_{INH} is low-level.

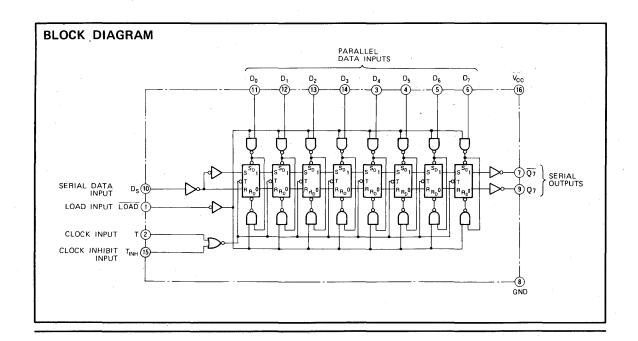
Shift operations are initiated upon T transiting from low to high, and the data present at D_S appears as an output pulse from Q_7 , $\overline{Q_7}$ of the 8th flip-flop circuit. The output at $\overline{Q_7}$ is always an inverted value of that present at Q_7 .

When $D_0 \sim D_7$ is used as the input, \overline{LOAD} is active-low. Since $D_0 \sim D_7$ are entered at the direct-set, direct-reset input of each flip-flop, read is executed regardless of the status of other inputs.



Care should be exercised to prevent the recording of erroneous data caused by a change in the value of $D_0 \sim D_7$ when \overline{LOAD} switches from low to high-value. Also, when T_{INH} is high, a shift operation will not be effected with clock pulse input. When T is low-level, and T_{INH} transits from low to high, a 1-bit shift operation will be executed.

M74LS165AP is an enhanced-performance version of M74LS165P having modified switching characteristics.



8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

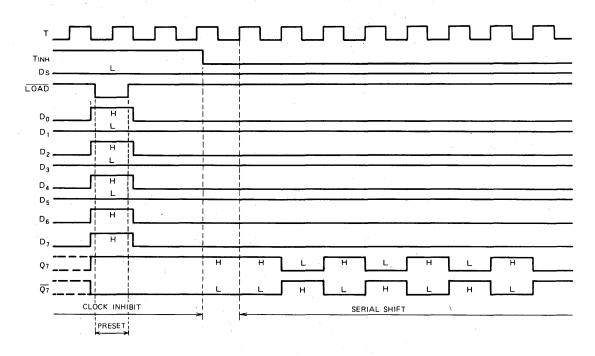
		Inputs		1	Internal	Outputs	Output
LOAD	TINH	Ţ	Ds	D ₀ …D ₇	Qo	Q ₁	Q7
L	×	×	×	D ₀ ···D ₇	D ₀	D ₁	D ₇
н	L	L	x	х	Q ₀ 0	Q1 ⁰	Q7 ⁰
H	L	1	Н	×	н	Q ₀ 0	Q6 ⁰
Н	L,	1	L	х	L	Qo ^o	Q ₆ 0
Н	Н	X	X	x	Q ₀ 0	Q ₁ 0	Q7 ⁰

Note 1. X : Irrelevant

† : Transition from low to high (positive edge trigger)

 Q^0 : Status of output before \uparrow of T

TIMING DIAGRAM



8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5 - Vcc	V
Topr	Operating free-air ambient temperature range		-20 - + 75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

S	Parameter					
Symbol	raramete	Tarameter			Max	Unit
Vcc	Supply voltage		4.75	5	5 . 25	V
Іон	High-level output current	V _{0H} ≥2.7V	0		- 400	μА
		V _{OL} ≤ 0.4 V	0		4	mA
lor 1	Low-level output current	V _O ∟≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	.			Limits		
Зутью	raiametei	Test condi	tions	Min	Тур*	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	· V
Vic	Input clamp voltage	Vcc=4.75V, lic=-	Voc=4.75V, lic=-18mA			-1.5	V
Voн	High-level output voltage	$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-400\mu A$		2.7	3.5		· V
VoL	Low-level output voltage	Vcc=4.75V Vi=0.8V , Vi=2V	IOL=4mA		0.25	0.4	V
	High-level input current	$V_{CC} = 5.25V, V_1 = 2.$			0.33	20	μА
HII	right-level input current	$V_{CC} = 5.25 \text{ V}, V_1 = 10$	$V_{CC} = 5.25 \text{ V}, V_{I} = 10 \text{ V}$			0.1	mA
liL	Low-level input current	$V_{CC} = 5.25 \text{V}, V_{I} = 0.4 \text{V}$				-0.4	mA
los	Short-circuit output current (Note 3)	Vcc=5.25V, Vo=0\	/	-20		— 100	mA
lcc	Supply current	Vcc=5.25V (Note 4)	,		18	. 30	mA

* . All typical values are at V_{CC} = 5V, T_a = 25°C. Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

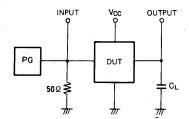
SWITCHING CHARACTERISTICS (Vcc=5V, $T_a=25$ °C, unless otherwise noted)

Symbol	Parameter	T		Limits			
Symbol	i arameter		Min	Тур	Max	Unit	
fmax	Maximum clock frequency	,		25	38		MHz
t PLH	Low-to-high-level, high-to-low-level output propagation				17	35	ns
t PHL	time, from input \overline{LOAD} to outputs Q_7 and \overline{Q}_7				20	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0 45.5	•		14	25	ns
t PHL	time, from input T to outputs Q_7 and $\overline{Q_7}$	CL ≈ 15pF			13	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 4)			9	25 -	ns
t _{PHL}	time, from input D ₇ to output Q ₇				20	30	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				16	30	ns
t PHL	time, from input D_7 to output $\overline{Q_7}$				12	25	ns

With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the LOAD input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

Note 4. Measurement Circuit

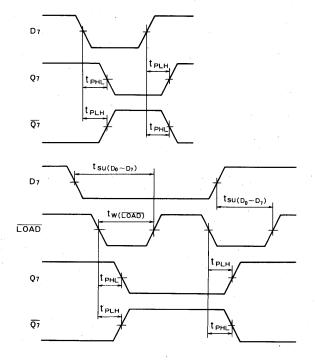


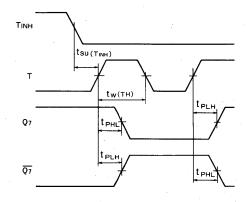
- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P,P},
 Z_o = 50Ω.
 C_L includes probe and jig capacitance.

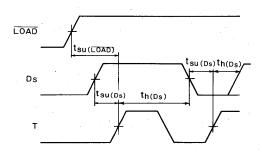
TIMING REQUIREMENTS (Vcc=5V, Ta=25°C, unless otherwise noted)

	Parameter	Test conditions		Unit		
Symbol	, arameter	lest conditions	Min	Тур	Max	Unit
tw(T)	Clock pulse width		25	13	`.	ns
tw (LOAD)	LOAD low-level pulse width]	15	12		ns
tsu (TiNH)	Setup time T _{INH} to T]	30	13		ns
tsu (D ₀ ~D ₇)	Setup time D ₀ ~ D ₇ to LOAD		10	9		ns
t _{su (Ds)}	Setup time D _S to T		20	8		ns
tsu (LOAD)	Setup time LOAD to T		45	0		ns
th	Hold time	1	0	0		ns

TIMING DIAGRAM (Reference level = 1.3V)







MT4LS166AP

8-BIT SHIFT REGISTER

DESCRIPTION

The M74LS166AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input — serial output shift register function.

FEATURES

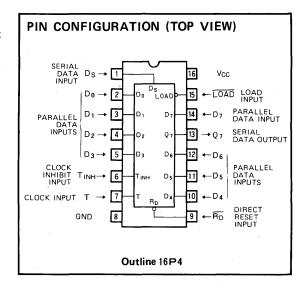
- Parallel-to-serial conversion
- Clock inhibit input
- Direct overriding reset
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

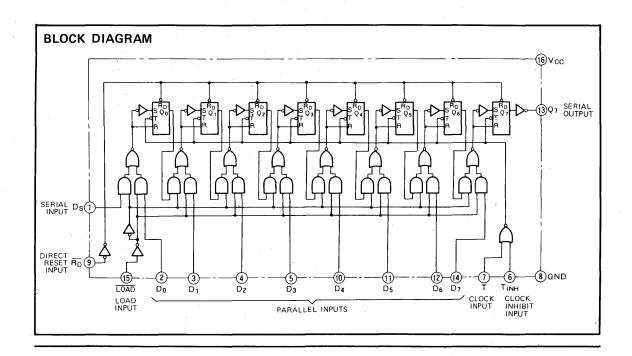
FUNCTIONAL DESCRIPTION

Parallel or serial input mode is selected via the load input $\overline{\text{LOAD}}$ signal. When $\overline{\text{LOAD}}$ is high-level, serial input enables the serial data input and couples the eight flip-flop for serial shifting with each clock pulse. Conversely, when $\overline{\text{LOAD}}$ is low-level, parallel data inputs $D_0 \sim D_7$ are enabled and synchronous loading occurs on the next clock pulse. While during parallel loading, serial data flow in inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either low enable the clock inputs high inhibits clocking; holding either low enable the clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other



clock input. The clock-inhibit input should be change to the high level only while the clock input is high. The buffered, direct reset input $\overline{R_D}$ overrides all other inputs, including the clock, and sets all flip-flop to zero.

M74LS166AP has been improved to resolve timing problems on $\overline{\text{LOAD}}$ input signal switching that occurred in the M74LS166P. Serial output Q7 has also been provided with a buffer to reduce noise, resulting in a change in specifications.



MITSUBISHI LSTTLs **M74LS166AP**

8-BIT SHIFT REGISTER

FUNCTION TABLE (Note 1)

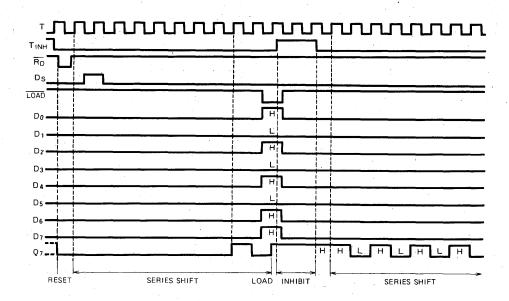
		t,	n				t _{n+1}	<i>a</i> .
		_	-		Parallel Inputs	Interna	outputs	^
RD	LOAD	TINH		Ds	D ₀ ···D ₇	Qo	Q ₁	Q ₇
L	X	×	X	х	. x	L	L.	L
н	×	L	L	Х	. X	Q ₀₀	Q ₁₀	Q70
Н	L	L	1	Х	D ₀ D ₇	Do	D ₁	D ₇
Ι	н	L	<u> </u>	. н	х	Н	Qon	Q _{6n}
Н	Н	L	. 1	L	X	L :	Qon	Q _{6n}
Н	x	Н	1	Х	X	Q ₀₀	Q _{1n}	Q ₇₀

Note 1. X : Irrelevant

 \uparrow : Transition from low to high (positive edge trigger) $D_0\sim D_7$: Indicates status prior to clock pulse at input D_0 thru D_7 . Indicates initial status of output Q_0 thru Q_7 . Indicates initial status of output Q_0 thru Q_7 . Indicates status of Q_0 thru Q_7 immediately prior to clock input

t_{n+1}: Bit time after one clocking transition,

TIMING DIAGRAM



MITSUBISHI LSTTLS M74LS166AP

8-BIT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level output	-0.5 ~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			-	Unit	
Symbol	Farameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ
1 -	Low-level output current	V _{OL} ≤0.4V	0		4	mA
IOL	FBM-level output current	V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Toot condition		Limits			Unit
Symbol	Parameter	Test condition	rest conditions			Max	Unit
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	٧
Voн	High-level output voltage	V _{CC} =4.75V, V _I =0.8V			2.5		
	Triginevel output vortage	$V_1 = 2V, I_{OH} = -400 \mu A$	•	2.7	3.5		٧
		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	V
		V _{CC} =5.25V, V _I =2.7V				20	μА
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
LIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA.
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 20		-100	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			20	32	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a\approx 25^{\circ}C$, unless otherwise noted)

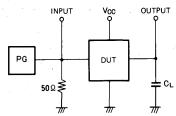
Combal	Parameter	Too and the		Unit		
Symbol	Farameter	Test conditions	Min	Тур	Max	Oint
f _{max}	Maximum clock frequency		25	38		MHz
t _{PHL}	High-to-low-level output propagation time, from input $$\rm R^{-}_{\rm D}$$ to output ${\rm Q}_{\rm 2}$	C _L = 15pF (Note 5)		18	30	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			10	20	ns
t _{PHL}	time, from input T to output Q ₇			12	25	ns

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

8-BIT SHIFT REGISTER

Note 4. Measurement circuit

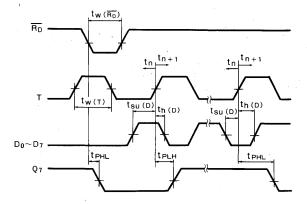


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_t = 6ns, t_t = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
 (2) C_L includes jig and probe capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Offic
tw _(T)	Clock pulse width		20	14		ns
tw(RD)	Reset pulse width		20	8		ns
tsu (D)	Setup time D _S , D ₀ ~D ₇ to T	7	20	. 12		ns
tsu(LOAD)	Setup time LOAD to T	7	30	12		ns
t _h	Hold time all inputs to T	7	0	-10		ns

TIMING DIAGRAM (Reference level = 1.3V)



TEST CONDITION TABLE

Data input for test	LOAD	Output tested	Bit time
D ₇	0V	Q ₇	t _{n+1}
Ds	4.5V	Q7	t _{n+8}

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS170P is a semiconductor integrated circuit containing a 4-word by 4-bit register file function with open collector outputs.

FEATURES

- Separate read and write addresses for simultaneous data
- Read and write enable inputs provided
- Easy expansion of memory capacity using enable inputs
- Usable in AND-Tie connection (open collector outputs)
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

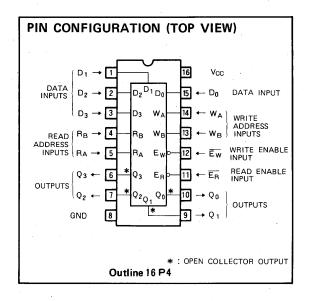
General purpose, for use in industrial and consumer equipment,

FUNCTIONAL DESCRIPTION

This device contains 16 D-type latches as memory elements. Separate read and write inputs, both address and enable, allow simultaneous read and write operation, thereby enabling readout of other word contents during writing and writing into other words during readout resulting in increased speed. Open collector outputs make it possible to

The open collector outputs permit wire-AND connections for 256 outputs and expansion up to 1024 words.

M74LS170P has the same functions and pin connections as M74LS670P but the latter is provided with 3-state outputs.

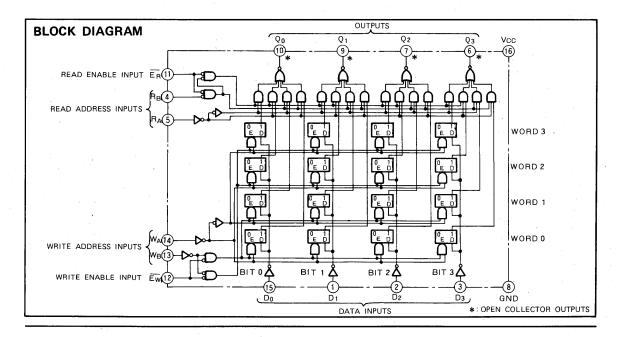


Writing Method

Writing into the bits is performed by specifying the words with address inputs W_A and W_B and by applying the data to data inputs D_0 , D_1 , D_2 and D_3 . The write enable input $\overline{E_W}$ is set low. No writing is performed when $\overline{E_W}$ is set high.

Readout Method

When the words are specified by read address inputs R_A and R_B , the contents of the stored bits appear in outputs Q_0 , Q_1 , Q_2 and Q_3 . Read enable input $\overline{E_R}$ is set low. When $\overline{E_R}$ is set high, all the outputs are set high.



4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1) ,

Writing Method

14/	14/	Ew		Word						
WA	WB	Ew	0	1	2	3				
Х	×	Н	Q ⁰	Q ⁰	Q ⁰	Qū				
L	L	L	Q=D	Q ⁰	Q ⁰	Q ⁰				
Н	L	L	Q ⁰	Q=D	Q ⁰	Q0				
L	н	L	Q0	Q0	Q=D	Q0				
Н	Н	L	Q ⁰	Q ⁰	Q ⁰	Q=D				

Readout Method

RA	R _B	ĒR	Q ₀	Q ₁	Q ₂	Q ₃
Х	X	Н	Н	H	Н	Н
L	L	L	W ₀ B ₀	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃
Н	L	Γ	W ₁ B ₀	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃
L	Н	Ţ	W ₂ B ₀	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃
Н	H	L	W ₃ B ₀	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃

Note 1 Q⁰: No change in word contents.

Q = D: Data input contents are written into specified word.

W_XB_Y: Indicates word X and bit Y contents

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	,V
Vi	Input voltage		- 0.5~ + 15	·V
Vo	Output voltage	High-level state	-0.5~+7	٧
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Limits			
Symbol	Paramete	Min	Min	Тур	Max 5.25	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _O =5.5V	0		100	μА
	1 11 11	V _{OL} ≤0.4V	0		4	mA
lor	Low-level output current	V _{OL} ≦0.5V	. 0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parama	Parameter Test conditions			Limits	100	Unit	
Symbol	Parame			tions	Min	Typ ★ Max		
VIH	High-level input voltage							V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
Гон	High-level output current		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, V_{O}=5.5V$				100	μΑ
1/	Voi Low-level output voltage	-	V _{OC} =4.75V	I _{OL} = 4mA		0.25	0.4	V
Vol. Low-level output voltage		I _{OL} = 8mA		0.35	0.5	V		
		ER, Ew				40		
l _{IH}	High-level input current	Other inputs	$V_{CC} = 5.25V, V_{I} = 2.7$	V _{CC} =5.25V, V _I =2.7V			20	μA
'IH	r ngr-lever input current	ER, EW					0.2	
		Other inputs	$V_{CC} = 5.25V, V_I = 10V$	'			0.1	mĄ
hL.	Low-level input current	ER, Ew	V 5.05V V 0.				-0.8	
IIL COM-level miput	25. icvoi riiput current	Other inputs	$V_{CC} = 5.25V, V_{I} = 0.4V$				-0.4	mA
Icc	Supply current		V _{CC} =5.25V (Note 2)			25	40	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.

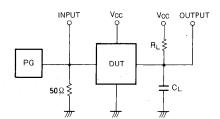
Note 2: I_{CC} is measured with W_A , W_B , R_A and R_B at 0V and with $D_0 \sim D_4$, $\overline{E_R}$ and $\overline{E_W}$ at 4.5V.

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol		lest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation			13	30	ns
tpHL	time, from input ER to outputs Q ₀ , Q ₁ , Q ₂ , Q ₃			11	30	ns .
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	,		16	40	ns
t _{PHL}	time, from inputs R_A , R_B to outputs Q_0 , Q_1 , Q_2 , Q_3	$R_{L} = 2 k\Omega$		15	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O _L =15pF (Note 3)		16	45	ns
t _{PHL}	time, from input $\overline{\mathbb{E}_W}$ to outputs Q ₀ , Q ₁ , Q ₂ , Q ₃			16	40	'ns
tpLH	Low-to-high-level, high-to-low-level output propagation time	•		15	45	ns
t _{PHL}	from inputs D_0 , D_1 , D_2 , D_3 to outputs Q_0 , Q_1 , Q_2 , Q_3	<u> </u>		15	35	ns

Note 3: Measurement circuit



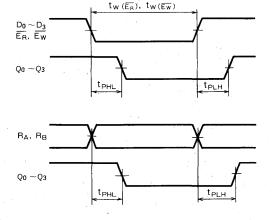
- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

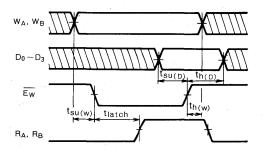
TIMING REQUIREMENTS (V_{CC}=5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
эушьог	ratameter	rest conditions	Min	Тур	'Max '	Onit
tw(ER)	Read enable input E _R pulse width		25	9		ns
tw(Ew)	Wright enable input E _W pulse width		25	9		ns
t _{su(D)}	D ₀ ~ D ₃ setup time with respect to $\overline{E_W}$		10	5		ns
t _{su(W)}	WA, WB setup time with respect to EW		15	– 2		ns
th(D)	D ₀ - D ₃ hold time with respect to E _W		15	0		ns
th(W)	WA, WB hold time with respect to EW	· ·	5	– 2		ns
tlatch	D ₀ ~D ₃ latch time (note 4)		25	5		ns

Note 4: t_{LATCH} is the time required for storage when data is changed.

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

DESCRIPTION

The M74LS173AP is a semiconductor integrated circuit containing a 4-bit register with 3-state outputs.

FEATURES

- Data can be held irrespective of number of clock pulses
- Data are non-destructible with 3-state outputs
- Positive edge-triggering
- Direct reset input provided
- Easy bit expansion
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

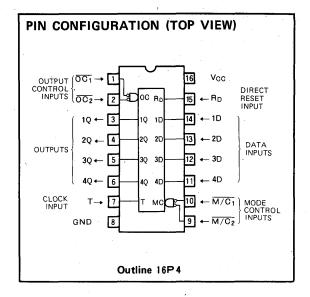
APPLICATION

General purpose, for use in industrial and consumer equipment,

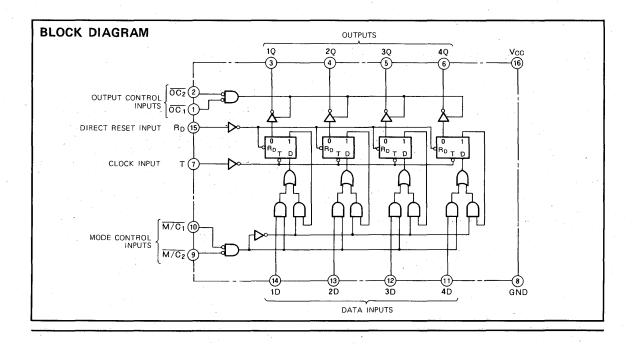
FUNCTIONAL DESCRIPTION

This device contains 4 edge-triggered D-type flip-flop circuits and direct reset input R_D and clock input T common to all circuits. When T changes from low to high, the information of data inputs 1D \sim 4D immediately before the change appears in outputs 1Q \sim 4Q respectively in accordance with the function table.

When R_D is set high with mode control inputs $\overline{M/C_1}$ and $\overline{M/C_2}$ low, all the flip-flop outputs are low irrespective of the other inputs. When $\overline{M/C_1}$ or $\overline{M/C_2}$ is high, $1Q \sim 4Q$



hold the status established when $\overline{M/C_1}$ and $\overline{M/C_2}$ are low, irrespective of the other signals. When $\overline{OC_1}$ or $\overline{OC_2}$ is high, $1Q \sim 4Q$ are all put in the high-impedance state. In this case, the internal flip-flop status does not change because of the $\overline{OC_1}$ and $\overline{OC_2}$ input change. For use as a D-type flip-flop, set $\overline{M/C_1}$, $\overline{M/C_2}$, $\overline{OC_1}$ and $\overline{OC_2}$ all low.



FUNCTION TABLE (Note 1)

RD	Т	M/C ₁	M/C ₂	D	Q
Н	×	X	×	Х	L
L	L	×	×	X	Q ⁰
L	1	Н	×	Х	Q ⁰
L	. 1	×	Н	X	Q ⁰
L	1	L	L	L	L
L	1	L	L	Н	Н

Note 1 High-impedance state when $\overline{OC_1}$ and/or $\overline{OC_2}$ are high.

† : Transition from low to high (positive edge trigger)

X : Irrelevan

 $Q^{\,0}$: Level of Q before the indicated steady-state input conditions were

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
Vı	Input voltage			-0.5~+15	V
Vo	Output voltage	Off-state		-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		***************************************	-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim \pm 75^{\circ}C$, unless otherwise noted)

Symbol	Paramete		11.25			
Symbol	raramete		Min	Тур	Max	Unit
Voc	Supply voltage	-	4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mΑ
		V _{OL} ≦0.4V	0		12	mA
loL	Low-level output current	V _{0L} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - \pm 75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test soud	tions		Limits		Unit
Зуптьог	rarameter .	Test condi	Test conditions		Тур 🛪	Max	Unit
VIH	High-level input voltage			2			V
. VIL	Low-level input voltage	-				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC} = 4.75V \cdot V_{I} = 0.8V$ $V_{I} = 2V \cdot I_{OH} = -2.6mA$		3.1	·	٧
VoL	Low-level output voltage	$V_{CC} = 4.75V$ $V_{I} = 0.8V, V_{I} = 2V$	I _{OL} = 12 mA		0.25	0.4	V
łozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V				20	. μΑ
lozL	Off-state low-level output current	V _{CC} 5.25V, V _I =2V	. Vo=0.4V			- 20	μА
1	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μА
lін	High-level input current	V _{CC} =5.25V, V _I =10V	<i>,</i> .			0.1	mA
1 _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V ₀ =0V	V _{CC} =5.25V, V _O =0V			- 130	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)	V _{CC} =5.25V (Note 3)		17	30	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured after $\overline{M/C_1}$, $\overline{M/C_2}$, 1D 4D and $\overline{OC_2}$ have been set to 0V, T and $\overline{OC_1}$ to 4.5V and R_D from 0V to 4.5V.



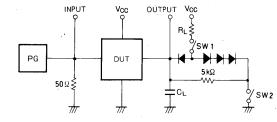
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, runless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit	
Symbol	r aratifeter	rest conditions	rest conditions		Тур	Max	Unit	
fmax	Maximum clock frequency			30	35		MHz	
t _{PHL}	High-to-low-level output propagation time, from input R_D to output Q	C _L =45pF	(Note 4)		21	35	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	1			20	25	ns	
t _{PHL}	time from input T to output				26	30	ns	
t _{PZH}	Output enable time to high-level	O. 45-F B -6670	(0) ()		.14	23	ns	
t _{PZL}	Output enable time to low-level	$C_L=45pF, R_L=667\Omega$	(Note 4)		.15	27 .	ns	
t _{PHZ}	Output disable time from high-level	0 - Fr F B 6670	(Note 4)		11	17 .	ņs	
t _{PLZ}	Output disable time from low-level	$C_L=5pF,R_L=667\Omega$	(Note 4)		9	17	ns	

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Total and distance		Limits		
Symbol	- I aramoter	Test conditions	Min	Тур	Max	Unit
tw(T)	Clock input T pulse width		20	4		ns
tsu (D)	Setup time 1D ~ 4D to T		17	3		ns
t _{h (D)}	Hold time 1D ~ 4D to T		6	3		ns
t _{su(M/C)}	Setup time M/C ₁ , M/C ₂ to T		35	20		ns
th(M/C)	Hold time M/C ₁ , M/C ₂ to T	- }	0	- 12		ns
tw(RD)	Direct reset R _D pulse width	1	20	10		ns
trec	Recovery time RD to T	1	15	12		ns

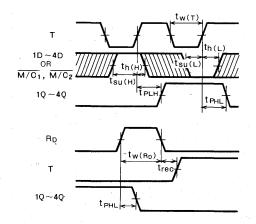
Note 4: Measurement circuit

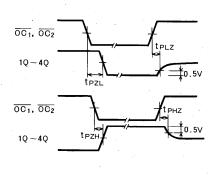


SW 1	SW2
Open	Closed
Closed	Open
Closed	Closed
Closed	Closed
	Open Closed Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$.
- (3) C_Lincludes probe and jig capacitance.

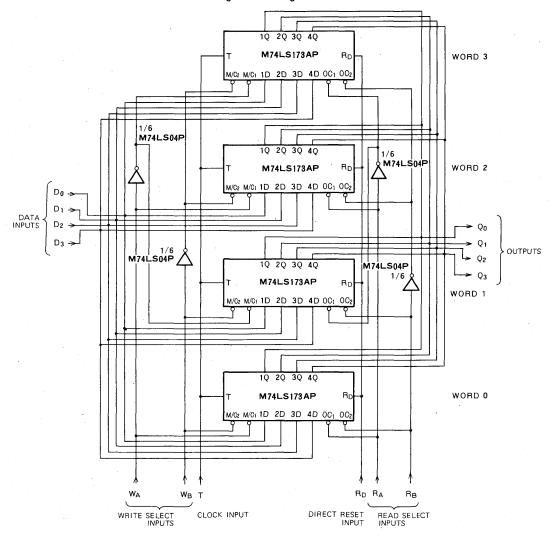
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Shown below is a schematic of a 4-bit x 4-word register file using the M74LS173AP.



Writing method

W _B	W _A	WORD				
**B		0	1	2	3	
L	L	Q = D	Q ⁰	Q ⁰	Q ⁰	
L	н	Q ⁰	Q = D	O ₀	.Q ⁰	
Η	L	Q ⁰	Q ⁰	Q=D	Q ⁰	
Н	н	Q ⁰	Q ⁰	Q ⁰	Q = D	

Readout method

RB	RA	Qo	Q1	02	Q3
L	L	W_0D_0	W ₀ D ₁	W ₀ D ₂	W ₀ D ₃
L	Н	W ₁ D ₀	W ₁ D ₁	W ₁ D ₂	W ₁ D ₃
Н	L	W ₂ D ₀	W ₂ D ₁	W ₂ D ₂	W ₂ D ₃
Н	Н	W ₃ D ₀	W ₃ D ₁	W ₃ D ₂	W ₃ D ₃

HEX D-TYPE FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS174P is a semiconductor integrated circuit containing 6 D-type edge-triggered flip-flop circuits with common clock input T and direct reset input $\overline{R_D}$ as well as discrete data input D.

FEATURES

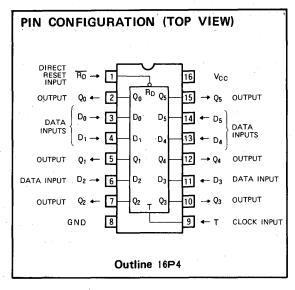
- Positive edge-triggering
- Common clock and direct reset inputs for all 6 circuits
- Q and Q outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change appears in the output Q in accordance with the function table. When $\overline{R_D}$ is low, all Q are low, regardless of the status of the other input signals. For use as a D-type flip-flop, keep $\overline{R_D}$ high.



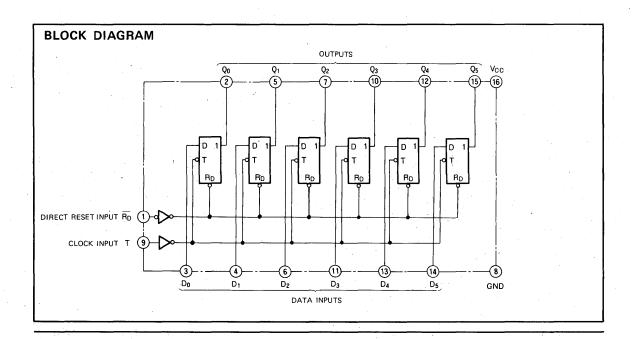
FUNCTION TABLE (Note 1)

RD	Т	.D	Q
L	Х	Х	L
Н	1	Н	Н
Н	1	L	L
Н	L	Х	Q ⁰

Note 1: ↑: transition from low to high level

Q⁰: level of Q before the indicated steady-state input conditions were established

X : irrelevant



HEX D-TYPE FLIP FLOPS WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5~+7	V
V, .	Input voltage		-0.5~+15	V.
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = ~20 ~ +75 °C, unless otherwise noted)

Cumbal	Parameter			Unit		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		- 400	μА
	Low-level output current	V _{OL} ≦0.4V	0		4	mA
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA .

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

		T	*!	-	Limits		Unit	
Symbol	Parameter	Test condi	tions	Min	Typ*	Max	Offic	
ViH	High-level input voltage			2			V	
VIL	Low-level input voltage					0.8	V	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5	V	
.,	High-level output voltage	V _{CC} =4.75V, V _I =0.8	V · .	2.7	2.4			
V _{OH} .	High-level output voltage	$V_1 = 2 \text{ V}, I_{OH} = -400 \text{ A}$	ıΑ	2.7	3.4		V	
		V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	٧	
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA.		0.35	0.5	V	
	High-level input current	V _{CC} =5.25V, V _I =2.7	V			20	μА	
Ьн	High-lever input current	V _{CC} =5.25V, V _I =10V	'			0.1	mÀ	
lıL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA.	
los	Short-circuit output current Note 2	V _{CC} =5.25V, V _O = 0 \	/	-20		- 100	mA .	
Icc	Supply current	V _{CC} =5.25V (Note 3)			16	26	mA	

 $[\]star$: All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

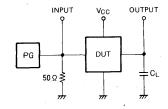
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with D, $\overline{R_D}$ inputs at 4.5V and a momentary ground, then 4.5V, applied to T input

SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}, T_a = 25 ^{\circ}\text{C}, \text{ unless otherwise noted}$)

C introd	Parameter	T	Limits			Unit
Symbol	rarameter	Test conditions	Min	Тур	Max	Onit
fmax	Maximum clock frequency		30	47		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	30	ns
t _{PHL}	time, from input T to output Q	C _L = 15pF (Note 4)		10	30	ns
t _{PHL}	High-to-low-level output propagation time, from input RD to output Q			11	35	ns

Note 4: Measurement circuit



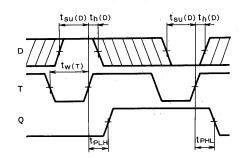
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_0 = 50Ω
- (2) C_L includes probe and jig capacitance.

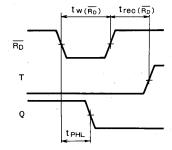
HEX D-TYPE FLIP FLOPS WITH RESET

TIMING REQUIREMENTS ($V_{CC} = 5 \text{ V}$, $T_a = 25 \text{ C}$, unless otherwise noted)

	Parameter	Test conditions -	Limits			Unit
Symbol	Parameter		Min	Тур	Max	Unit
t _W (T)	Clock input T pulse width		20	4		ns
tw (RD)	Reset input RD pulse width	·	20	6		· ns
t _{su(D)}	Setup time D to T		20	2		ns
th(D)	Hold time D to T		5	0		ns
trec(RD)	Recovery time RD to T		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

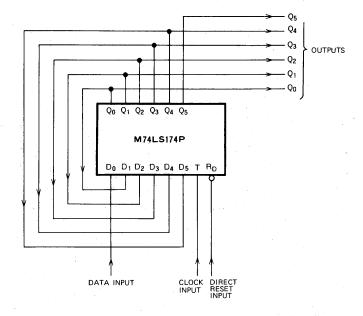




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

6-bit shift register



MITSUBISHI LSTTLs

M74LS175P

QUADRUPLE D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS175P is a semiconductor integrated circuit containing 4 positive edge-triggered D-type flip-flops with common clock input T and direct reset input \overline{R}_D and discrete data inputs D.

FEATURES

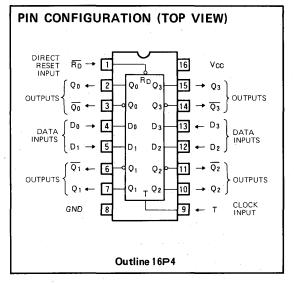
- Positive edge-triggering
- Clock and direct reset inputs common to 4 circuits
- Q and Q outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and \overline{Q} in accordance with the function table. By setting $\overline{R_D}$ low, all the Q and \overline{Q} outputs are set low and high, respectively, irrespective of the status of the other inputs signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.

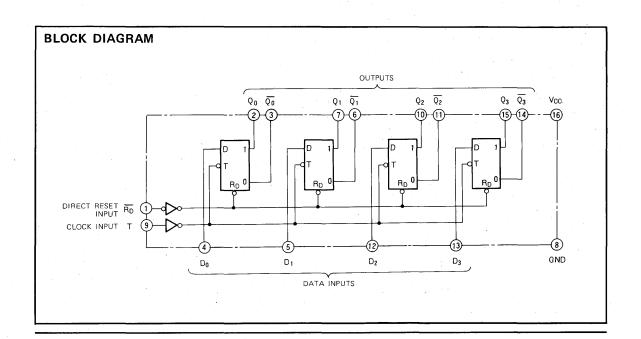


FUNCTION TABLE (Note 1)

RD	Т	D	Q ·	Q
L	Х	X	L	Н
Н	1	н	н	L
н	1	L	L	н
Н	L	X	Q0	Q0

Note 1 X : Irrelevant

- \uparrow : Transition from low to high level (positve edge trigger)
- Q0 : Level of Q before the indicated steady-state input conditions were established.



QUADRUPLE D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage	\$	-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	. V
Topr	Operating free-air ambient temperature range		-20~+75	. °C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits		
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
lo∟	Fow-level outbut confent	V ₀ L≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

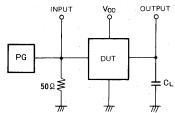
Symbol	Parameter	Test soud	itions		Limits		Unit	
Зуппрог	raianetei		Test conditions			Max	· Onit	
ViH	High-level input voltage						٧	
VIL	Low-level input voltage					0.8	V	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	-18mA			-1.5	V	
V _{OH}	High-level output voltage	1	V _{CC} =4.75V, V _I =0.8V V _I =2V, I _{OH} =-400μA		3.4		V	
ЙоГ	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I =2V	I _{OL} = 4mA		0.25	0.4	V	
l _{iH}	High-level input current	V _{CC} =5.25V, V _I =2.			0.00	20	μА	
'111	Tagn-level input current	$V_{CC} = 5.25V$, $V_{I} = 10$	V _{CC} =5.25V, V _I =10V			0.1	mA	
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	V _{CC} =5.25V, V _I =0.4V			-0.4	mA	
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	-20		— 100	mA	
loc	Supply current	V _{CC} =5.25V (Note 3)			11	18	mA .	

st : All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
- Cymber	, aramoto,	rest conditions	Min	Min Typ Max		
f _{max} .	Maximum clock frequency		30	50		ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C ₁ = 15 pF (Note 4)		10	25	ns
tpHL	time, from T to Q , \overline{Q}	OL-15pr (Note 4)		12	25	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	30	ns
tphL	time, from $\overline{R_D}$ to Q , \overline{Q}			19	30	ns

Note 4: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns,

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with 4.5V applied to D and $\overline{R_D}$ after T is set to 0V.

 $V_P = 3V_{P.P}, Z_0 = 50\Omega$

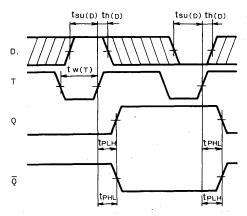
⁽²⁾ C_L includes probe and jig capacitance,

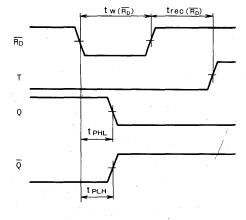
QUADRUPLE D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	raidilletei	rest conditions	Min	Тур	Max	Unit
t _{W(T)}	Clock input T pulse width		20	4		ns
tw(RD)	Direct reset input pulse width		. 20	7		ns
t _{SU(D)}	Setup time high to T		20	2		ns
t _h (D)	Hold time high to T		5	0		ns
trec(RD)	Recovery time for direct reset input		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

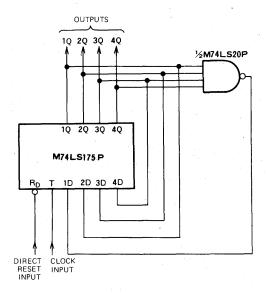


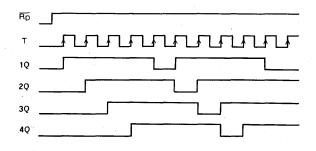


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Timing pulse generator





MT4LS190P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER
WITH MODE CONTROL

DESCRIPTION

The M74LS190P is a semiconductor integrated circuit containing a decade up/down counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control input
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (fmax = 38MHz typical)
- Wide operating temperature range (T_a≈ -20~+75°C)

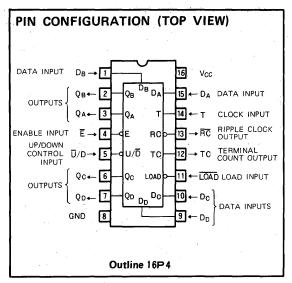
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

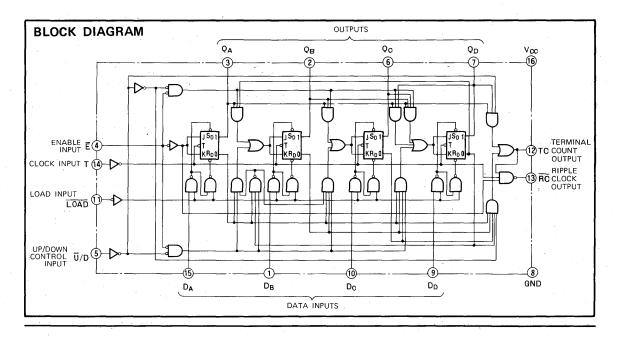
When enable input \overline{E} is low, load input \overline{LOAD} is high and the count pulses are applied to clock input T, the number of count pulses appear as a BCD code in the outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses. When the up/down control input \overline{U}/D is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high,

Presetting is performed regardless of the count pulses and by applying the data to data inputs DA, DB, DC and DD and by setting \overline{LOAD} low, the DA, DB, DC and DD signals appear in outputs QA, QB, QC and QD irrespective of the status of the other inputs and the count can be preset. Counting proceeds as per the status transition diagram with presetting to a numerical value of 10_2 or higher.



High appears in the terminal count output TC during count-up while 9_2 appears in Q_A , Q_B , Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output \overline{RC} only when \overline{E} and T are low and 9_2 appears in outputs Q_A , Q_B , Q_C and Q_D during count-up or Q_2 appears in the outputs during count-down. \overline{E} , TC and \overline{RC} are used when cascade-connecting the counter. (Refer to application examples.)

 \overline{E} can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for \overline{U}/D when T is high.



SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

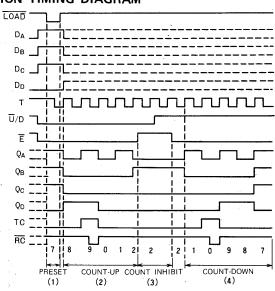
LOAD	Ē	Ū/D	Τ.	QA	QB	Qc	QD	
L.	×	X	Х	DA	DB	Dc	D _D	
Н	L.	L	1	Count-up				
н	L	٠Η	1	Count-down				
Н	Н	X	Х	Inhibit				

Note 1. ↑: Transition from low to high X : Irrelevant

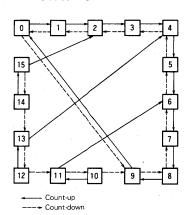
Ē	TC(1)	Т	RC
L	Н	L	L
L	Н	I	Н
н	· X	×	Ι
×	L.	Х	Н

TC is the output but the signal generated internally by the following logical expression.

OPERATION TIMING DIAGRAM



STATE DIAGRAM



Details of timing diagram

(1) Preset to 13

(2) Count-up 8, 9, 0, 1, 2

(3) Count inhibit

(4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	٧	
Vı	Input voltage		-0.5~+15	٧	
Vo	Output voltage	High-level state	-0.5~V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	.€	
Tstg	Storage temperature range		-65~+150	°C	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	D		Limits		Unit	
Symbol	Parameter	Min Typ		Max		
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА
	7 - 1 - 1 - 1 - 1 - 1	V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≦0.5V	0		. 8	mA

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

C	Dave		Tost conditi	ione	Limits			Unit
Symbol	Para	Parameter		Test conditions		Тур 🛊	Max	
V _{IH}	High-level input voltage	1			2			V
VIL	Low-level input voltage						0.8	. V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	8 mA			-1.5	V
Voн	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		. . V
VoL	Low-level output voltage		V _{CC} =4.75V V _I =0.8V, V _I =2V	I _{OL} =4mA		0.25	0.4	V V
Iн	High-level input current	T, LOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =2.7V	,		e,	20 60	μΑ
'IH		T, LOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =10V				0.1	mA
h_	Low-level input current	T, LOAD, U/D, DA~DD	V _{CC} =5.25V, V _I =0.4V	/			- 0.4 - 1.2	mA
los	Short-circuit output curre	ent (Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			20	35	mA

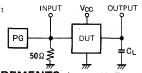
* : All typical values are at V_{CC} = 5V, Ta = 25°C. Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CC} is measured with all the inputs at OV.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

		Test conditions	-	Limits		Unit
Symbol	Parameter .	rest conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock freqency		20	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			19	33	ns
tphL	time, input LOAD to outputs QA, QB, QC, QD		1000	25	50	'ns
tpLH	Low-to-high-level, high-to-low-level output propagation			11	32	ns
tphL	time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD			25	40	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	CL=15pF (Note 4)		11	20	ns
t _{PHL}	time, from input T to output RC		-	11	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	24	ns
t _{PHL}	time, from input T to outputs QA, QB, QC, QD			14	36	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			20	42	ns
t _{PHL}	time, from input T to output TC			24	52	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			22	45	ns
tpHL	time, from input U/D to output RC			20	45	ns
tpLH	Low-to-high-level, high-to-low-level output propagation] .		15	33	ns
tpHL	time, from input U/D to output TC	·		15	33	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	1		10	33	ns
tpHL	time, from input E to output RC			11	33	ns

Note 4: Measurement circuit



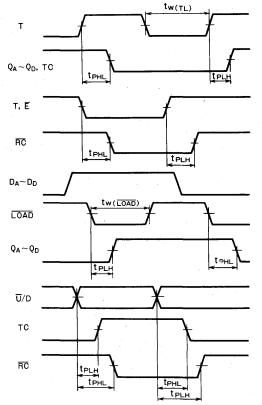
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_W = 500ns$, $V_P=3V_{P-P}, Z_O=50 \Omega$
- (2) C_L includes probe and jig capacitance

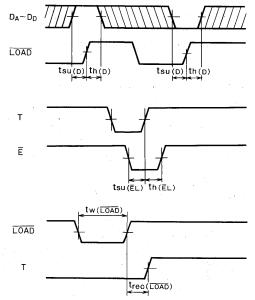
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	D	Test conditions		Limits		
	Parameter	rest conditions	Min	Тур	Max	Unit ns ns ns ns ns ns
tw(TL)	Clock input T low pulse width		25	9	2.30	ns
tw(LOAD)	Load LOAD pulse width		35	10		ns
tr	Clock pulse rise time	1		2000	100	ns
t _{SU(D)}	Setup time DA~DD to LOAD		20	9		ns
t _{SU(ĒL)}	Setup time E low to T		40	24		ns
t _h (D)	Hold time DA~DD to LOAD		5	0		ns
th(EL)	Hold time E low to T		- 5	2		ns
trec(LOAD)	Recovery time LOAD to T		20	16		ns

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

TIMING DIAGRAM (Reference level = 1.3V)

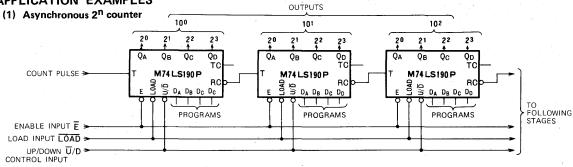


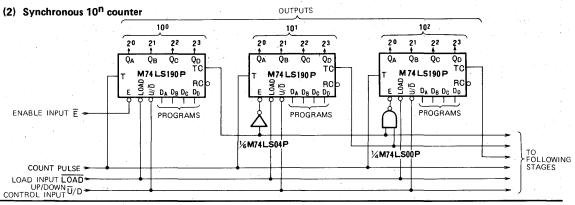


Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

Note 6. The shaded area with the arrows indicate the direction of when the input is permitted to change.

APPLICATION EXAMPLES





MITSUBISHI LSTTLS M74LS191P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

DESCRIPTION

The M74LS191P is a semiconductor integrated circuit containing a synchronous 4-bit binary (hexadecimal) counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control inputs
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (f_{max}= 40MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

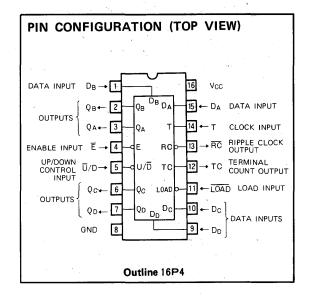
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

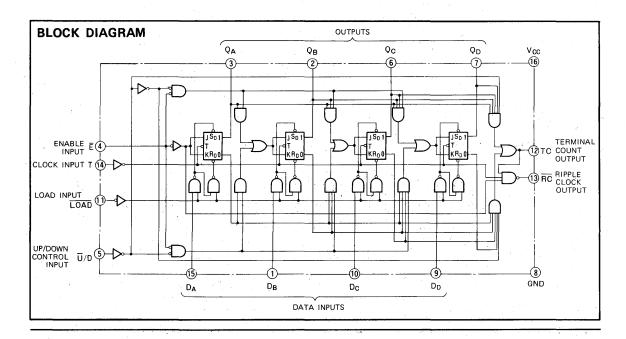
When enable input E is low, load input \overline{LOAD} is high and the count pulses are applied to clock input T, the number of count pulses appears as 4-bit pure binary code in the outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses. When the up/down control input \overline{U}/D is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs D_A , D_B , D_C and D_D and by setting \overline{LOAD} low, the D_A , D_B , D_C and D_D signals appear in outputs Q_A , Q_B , Q_C and Q_D irrespective of the status of the other inputs and the counter can be preset.



High appears in the terminal count output TC during count-up while 15_2 appears in $Q_A,\,Q_B,\,Q_C$ and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output \overline{RC} only when \overline{E} and T are low and 15_2 appears in outputs $Q_A,\,Q_B,\,Q_C$ and Q_D during count-up or 0_2 appears in the outputs during count-down. $\overline{E},\,TC$ and \overline{RC} are used when cascade-connecting the counter. (Refer to application example.)

 \overline{E} can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for \overline{U}/D when T is high.



SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

LOAD	Ē	Ū/D	T	QΑ	Qв	Qc	QD
L	Х	X	, X	DA	DB	Dc	D _D
H	L	L	1	Count-	up		
Н	L	Н	1	Count-	-down		
н	н	Х	X	Inhibit	t		

Note 1 \uparrow : Transition from low to high level

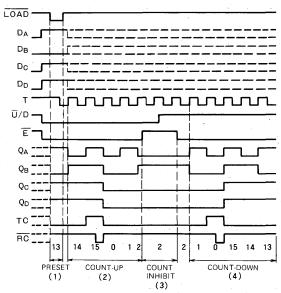
X: Irrelevant

Ē	TC ⁽¹⁾	Т	RC
L	н	L	L
L.	Н	н	H.
Н	×	. X	Τ
Х	· L	Х	Н

(1) TC is the output but the signal generated internally by the following logical expression.;

 $\begin{array}{l} TC = Q_{A} \cdot Q_{B} \cdot Q_{C} \cdot Q_{D} \cdot (\overline{U}/D) & \text{Count-up} \\ TC = \overline{Q}_{A} \cdot \overline{Q}_{B} \cdot \overline{Q}_{C} \cdot \overline{Q}_{D} \cdot (\overline{U}/D) & \text{Count-down} \end{array}$

OPERATION TIMING DIAGRAM



(1) Preset to 13

(2) Count-up 14, 15, 0, 1, 2

(3) Count inhibit

(4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5∼+7	V
Vı .	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5∼ V _{CC}	. V.
Topr	Operating free-air ambient temperature range		-20~+75·	°C
Tstg	Storage temperature range		−65∼ + 150	℃

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \approx +75^{\circ}C$, unless otherwise noted)

Symbol				Limits			
	Parameter	rarameter			Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ	
	Low-level output current	V _{OL} ≦0.4V	0		4	mA	
loL	Low-level output current	V _{OL} ≦0.5V	0 .	S	8	mA .	

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS (Ta = $-20 \sim +75 \, \text{°C}$, unless otherwise noted)

		- <u>-</u>	_			Limits		Umia	
Symbol		Parameter		Test conditions		Typ *	Max	Unit	
VIH	High-level input vol	tage			2			V	
VIL	Low-level input vol	tage					0.8	٧	
VIC	Input clamp voltage	3	V _{CC} =4.75V, I _{IC} =-18	3mA			- 1.5	٧	
Vон	High-level output v	oltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		V	
		-1	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V	
VOL	Low-level output v	ortage	$V_1 = 0.8V, V_1 = 2V$ $I_{OL} = 8 \text{ mA}$			0.35	0.5	V	
		T, LOAD, U/D, DA~DD	V 5 05V V 0 7V			20			
	High-level	Ē	$V_{CC}=5.25V, V_{I}=2.7V$				60	. μΑ.	
Ън	input current	T, LOAD, U/D, DA~DD					0.1		
	Ē	$V_{CC}=5.25V, V_{I}=10V$			0.3	mΑ			
	Low-level	T, LOAD, U/D, DA~DD					-0.4	^	
lie ;	input current	Ē	$V_{CC}=5.25V, V_{I}=0.4V$				-1.2	mA	
los	Short-circuit outpu	t current (Note 2)	V _{CC} =5.25V, V _O = 0 V		- 20		- 100	mA	
loc	Supply current		V _{CC} =5.25V (Note 3)			20	35	mA	

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Farallietei	rest conditions		Тур	Max	J Oille
fmax	Maximum clock frequency		20	40		MHz
t PL H	Low-to-high-level, high-to-low-level output propagation			19	33	ns
tPHL	time, from input LOAD to outputs QA, QB, QC, QD			25	· 50	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			11	32	ns
t PH L	time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD			25	40	ns
t _{PL} H	Low-to-high-level, high-to-low-level output propagation			11	20	ns
tphL	time, from input T to output RC			11	24	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	* .		12	24	ns
tphL	time, from input T to outputs QA, QB, QC, QD	C _L = 15pF (Note 4)		14	36	ns
t _{PL'H}	Low-to-high-output, high-to-low-level output propagation			20	42	ns
tphL	time, from input T to output TC	,		24	52	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			22	45	ns
tphL	time, from input U/D to output RC			20	45	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			15	33	ns
tphL	time, from input U/D to output TC			15	33	ns
t _{PL H}	Low-to-high-level, high-to-low-level output propagation			10	33	ns
tphL	time, from input E to output RC			11	33	ns

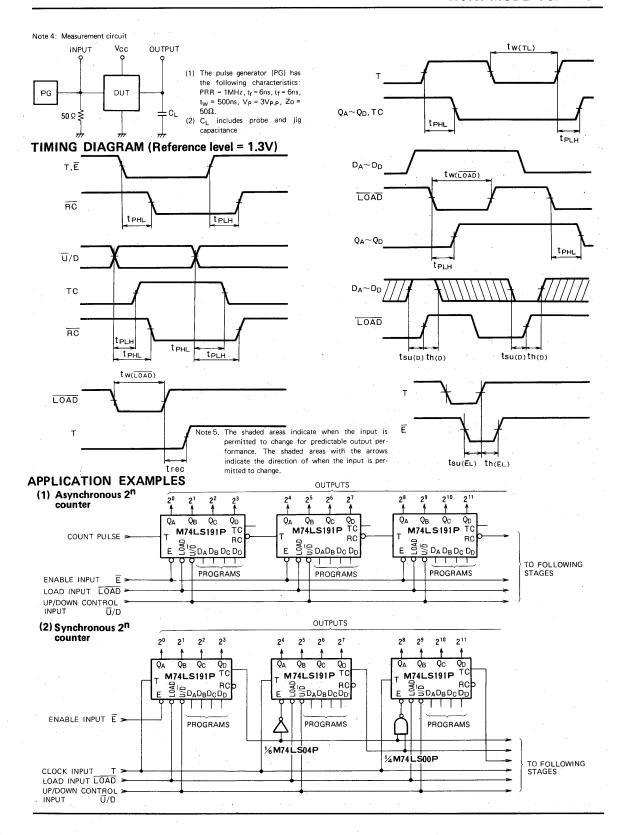
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions Limits			W . 1 122	11=14	
	Farameter	Test conditions	Min	Тур	Max	Unit	
tw(TL)	Clock input T low pulse width		25	9		ns	
tw(LOAD)	Load LOAD pulse width	· · · · · · · · · · · · · · · · · · ·	35	10		ns	
tr	Clock pulse rise time			2000	100	ns	
t _{SU(D)}	Setup time DA~DD to LOAD	•	20	9		ns	
t _{SU(ĒL)}	Setup time E low to T		40	24		ns	
th(D)	Hold time DA~DD to LOAD		5	0		ns	
th(ĒL)	Hold time E low to T		5	2		ns	
trec(LOAD)	Recovery time LOAD to T		20	16		ns	

Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3. I_{CC} is measured with all the inputs at OV.

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL



SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

DESCRIPTION

The M74LS192P is a semiconductor integrated circuit containing a synchronous decade up/down counter function with direct reset and preset inputs.

FEATURES

- Special up count, down count clock inputs
- Asynchronous preset input provided
- Direct reset input provided.
- Easy cascade connection possible
- High-speed counting (fmax = 38MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

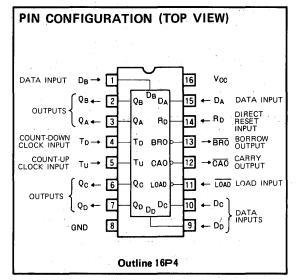
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the number of count pulses appears as a BCD code in outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses by setting load input \overline{LOAD} and T_D high, applying the count pulses to T_U while for count-down, \overline{LOAD} and T_U are set high and the count pulses are applied to T_D . Counting is performed when T_U or T_D changes from low to high.

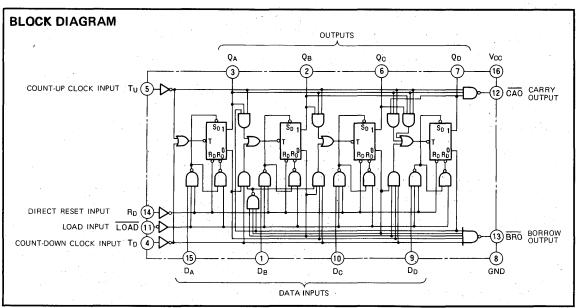
Presetting is performed independently of the count pulse. When data are applied to data inputs D_A , D_B , D_C and D_D and \overline{LOAD} is set low, the D_A , D_B , D_C and D_D signals appear in the Q_A , Q_B , Q_C and Q_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter. Counting proceeds as per the status



transition diagram with presetting to a numerical value of 10 or more.

Reset can be performed by setting the direct reset input R_D high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears in the carry output \overline{CAO} during count-up when 9 appears in Q_A , Q_B , Q_C and Q_D and when T_U is low while low appears in output \overline{BRO} when 0 appears in the outputs \overline{CAO} and \overline{BRO} should be connected to the next stage T_U and T_D for counter cascade connection. (Refer to the application examples.)



SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

FUNCTION TABLE (Note 1)

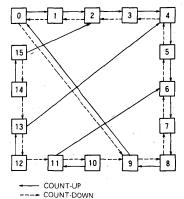
RD	LOAD	Τυ	T _D	Q_{A}	QB	Q _C	QD	CAO	BRO
I	X	Х	Х	L	L	L	L.	н	Н*
L	L	X	X	DA	DB	Dc	DD	н*	н*
L	Н	ıН	Н		Inf	nibit		H*	н*
L	H	1	Н	Count-up			H*	Н*	
L	н	Н	1	Count-down			н*	H*	

Note 1. ↑: Transition from low to high

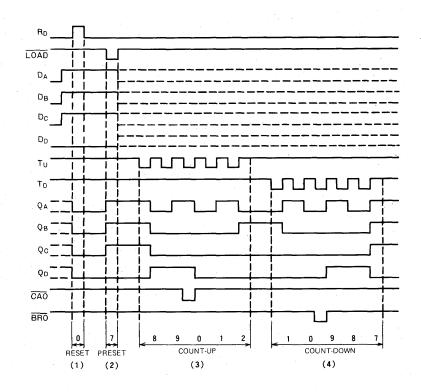
* : Normally high but low appears in accordance with the following logical expressions:

X : Irrelevant

STATE DIAGRAM



OPERATION TIMING DIAGRAM



Details of timing diagram

- (1) Reset
- (2) Preset to 7
- (3) Count-up 8, 9, 0, 1, 2 (4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	٧
Vi	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level state	-0.5 ~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg .	Storage temperature range		-65 ~ + 150	°C

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet					
	raramet	er	Min	Тур	Max	Unit
Voc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _O L≦0.4V	0		4	mA
lor	Low-level output current	V ₀ L≦0.5V	0		8	mΑ

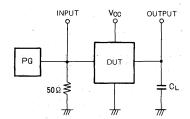
ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

		Test conditions		Limits			11-14
Symbol	Parameter	lest co	naitions	Min	Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					8.0	V
V _{IC}	Input clamp voltage	V _{CC} =4,75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V.
VoH	High-level output voltage	""	$V_{OC} = 4.75V \cdot V_{I} = 0.8V$ $V_{I} = 2V \cdot I_{OH} = -400 \mu A$		3.4		٧
.,	Low-level output voltage	V _{CC} = 4.75 V	I _{OL} =4mA		0.25	. 0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8mA		0.35	0.5	V
	High-level input current	V _{CC} =5.25V, V _I =2.	7 V			20	μА
lін	High-level input current	V _{CC} = 5.25V, V _I = 10	V _{CC} = 5.25V, V _I = 10V			0.1	mA
IIL	Low-level input current	V _{CC} = 5.25V, V _I = 0.	V _{CC} = 5.25V, V _I = 0.4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _C =0	V _{CC} =5.25V, V _O =0V			- 100	mA
lcc	Supply current	V _{CC} = 5.25V (Note 3	Vcc = 5.25V (Note 3)			34	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	T			Limits		Unit	
Зуппоот	rarameter	Test cond	ITIONS	Min	Тур	Max	Unit	
f _{max}	Maximum clock frequency			25	38		MHz	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				. 7	26	ns	
t _{PHL}	time, from input Tu to output CAO		- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1		14	24	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				7	24	ns	
tehL	time, from input To to output BRO	O 45 5 (Nam 4)			19	24	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)			20	38	ns	
tpHL	time, from input T _U , T _D to outputs QA, QB, QC, QD	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -			. 17	47	, ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation				24	40	ns	
t _{PHL}	time, from input LOAD to outputs QA, QB, QC, QD				20	40	ns	
t _{PHL}	High-to-low-level output propagation time, from input Rp to outputs QA, QB, QC, QD				12	35	ns	

Note 4. Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω .

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C. Note 2. All measurements should be done quickly and not more than one output should be shorted at a time. Note 3. I_{CC} is measured with R_D and $\overline{I_{COAD}}$ at 0V and T_U , T_D , $D_A \sim D_D$ at 4.5V

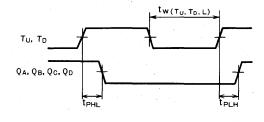
⁽²⁾ C_L includes probe and jig capacitance

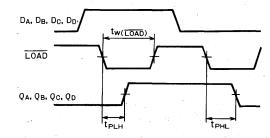
SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

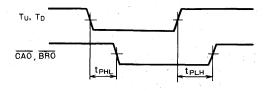
TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

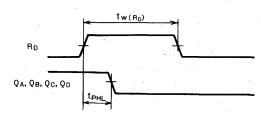
		T		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tw(TuL)	Clock input Tu low pulse width		20 .	14		ns
tw(TDL)	Clock input T _D low pulse width		20	18		ns
tw(LOAD)	Load LOAD pulse width		20	11		ns
tw(RD)	Direct reset R _D pulse width		20	4		ns
t _{SU (D)}	Setup time DA~DD to LOAD	· ·	20	4		ns
th(D)	Hold time D _A ∼D _D to LOAD		5	- 3		ns

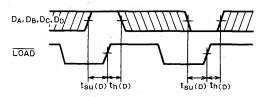
TIMING DIAGRAM (Reference level = 1.3V)











Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Asynchronous 10ⁿ counter OUTPUTS 100 101 102 QA COUNT-UP M74LS192P M74LS192P M74LS192P T_D DA DB DC DD D_A D_B D_C D_D COUNT-DOWN -DA De Do Rn I OAD TO FOLLOWING STAGES PROGRAM PROGRAM PROGRAM DIRECT RESET -LOAD

DESCRIPTION

The M74LS193P is a semiconductor integrated circuit containing a synchronous hexadecimal (4-bit binary) up/down counter with direct reset and preset.

FEATURES

- Special clock for up count, down count
- Asynchronous preset input provided
- Direct reset input provided
- · Cascade connection easily made
- High-speed counting (f_{max}=38MHz typical)
- Wide operating temperature range (T_a=-20~+75°C)

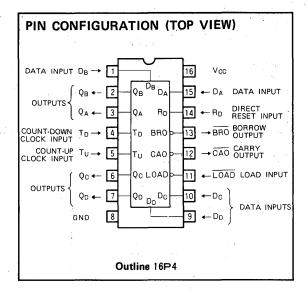
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the count pulse number appears as a 4-bit pure binary code in outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses by setting load input \overline{LOAD} and T_D to high, applying the count pulses to T_U while for count-down, \overline{LOAD} and T_U are set high and the count pulses are applied to T_D . Counting is performed when T_U or T_D changes from low to high.

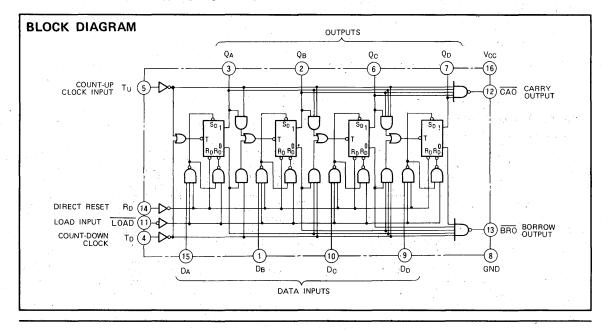
Presetting is performed regardlessly of the count pulse. When data are applied to data inputs D_A , D_B , D_C and D_D and \overline{LOAD} is set low, the D_A , D_B , D_C and D_D signals



appear in the Q_A , Q_B , Q_C , and Q_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter.

Reset can be performed by setting the direct reset input RD high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears is the carry output \overline{CAO} during count-up when 15 appears in O_A , O_B , O_C and O_D and when O_D is low, while low appears in output \overline{O} when 0 appears in the outputs and when O_D is low. \overline{O} and \overline{O} should be connected to O_D and O_D of the next stage for cascade connection. (Refer to the application example.)



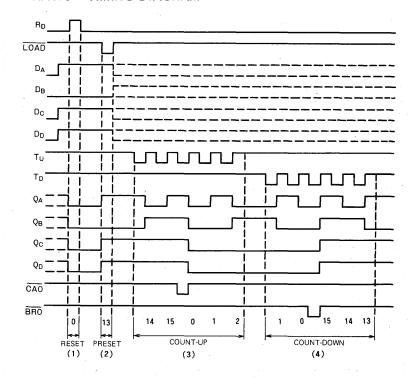
FUNCTION TABLE (Note 1)

RD	LOAD	Τυ	ΤD	QA	Qв	Q _C	QD	CAO	BRO
н	Х	X	Х		L	L	L	H.	H*
L	L	X	Х	DA	DB	Dc	DD	н*	н*
L	H	Н	H		Inh	ibit .		Н*	н*
L	Н	1	Н		Count-up			н*	н*
L	н	н	1		Count	-down		н*	H*

Note 1 ↑: Transition from low to high

X : Irrelevant

OPERATION TIMING DIAGRAM



Details of timing diagram

(1) Reset

(2) Preset to 13

(3) Count-up 14, 15, 0, 1, 2

(4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	rarame	er	Min	Тур	Max	Unit	
Voc	Supply voltage		4.75	5	5.25	. v	
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μА	
	Low-level output current	V _{OL} ≤0.4V	, 0.		4	mA	
loL	Low-level output current	VoL≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

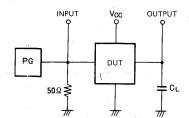
Constant	B	T	1		Limits		
Symbol	Parameter	Test cond	itions	Min	Typ *	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-			-1.5	٧	
Voн	High-level output voltage	$V_{CC} = 4.75V \cdot V_1 = 0.8V$ $V_1 = 2V \cdot 1_{OH} = -400 \mu A$		2,7	3.4		V
VoL	Low-level output voltage	V _{CC} = 4.75 V V _I = 0.8 V, V _I = 2 V	I _{OL} = 4mA I _{OL} = 8mA		0.25 0.35	0.4	V
I	High-level input current	V _{CC} =5.25V. V _I =2.	7V			20	μА
Ін	I ngir-lever input current	V _{CC} = 5.25V, V _I = 10	V			0,1	mΑ
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		- 20		- 100	mA
loc	Supply current	V _{CC} =5.25V (Note 3)	,		19	-34	mΑ

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
Oymbor	raidificter	est conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock frequency		25	38		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	26	ns
t _{PHL}	time, from input Tu to output CAO	*		14	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	24	ns
tpHL	time, from input TD to output BRO	0 45.5 (04)		19	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		20	38	ns
t _{PHL}	time, from inputs T_U , T_D to outputs Q_A , Q_B , Q_C , Q_D	'		17	47	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			24	40	ns
t _{PHL}	time, from input LOAD to outputs QA, QB, QC, QD			20	40	ns
t _{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A , Q_B , Q_C , Q_D			12	35	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P .p, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

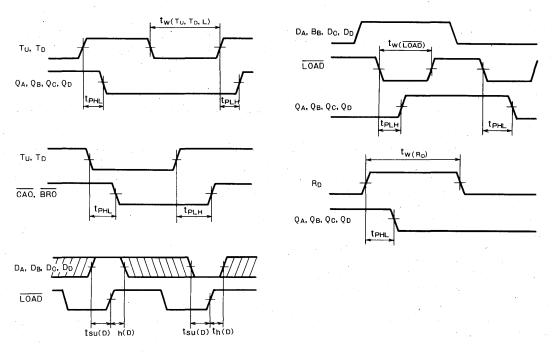
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with R_D and \overline{LOAD} at 0V and T_U , T_D , $D_A \sim D_D$ at 4.5V

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

0		Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
tw(TuL)	Clock input Tu low pulse width		20	14	1.	ns
tw(TDL)	Clock input T _D low pulse width		20	18		ns
tw(LOAD)	Load LOAD pulse width		20	11		ns
tw(RD)	Direct reset R _D pulse width		20	4		ns
t _{SU} (D)	Setup time DA~DD to LOAD		20	4		ns
th(D)	Hold time DA~DD to LOAD		- 5	- 3		ns

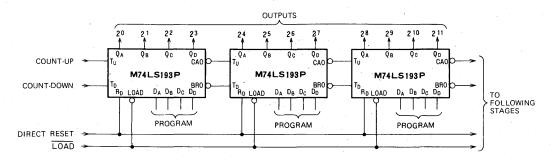
TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Asynchronous 2ⁿ counter



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS194AP is a semiconductor integrated circuit with a 4-bit bidirectional serial/parallel input-serial/parallel output shift register functions.

FEATURES

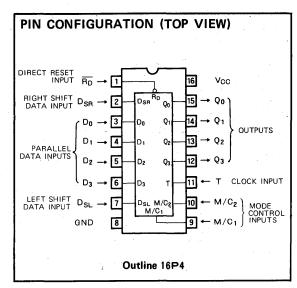
- Synchronous serial/parallel input-serial/parallel/output
- Right shift and left shift functions
- Mode control input provided
- Direct reset input provided
- Hold mode function
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

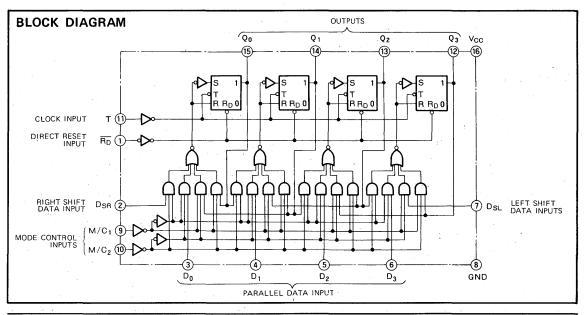
FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the modes control inputs M/C₁ and M/C₂. When M/C₁ is kept in high and M/C2 in low, the serial data are applied to right shift data input DSR and the clock pulse is applied to clock input T, the serial data are shifted sequentially to outputs $Q_0 \sim Q_3$ in synchronization with the clock pulse. When M/C₁ is kept in low and M/C₂ in high the serial data are applied to left shift data input D_{SL} and clock pulse is applied to clock input T, the serial data are shifted sequentially in synchronization with the clock pulse. The $D_0 \sim D_3$ signal appears in $Q_0 \sim Q_3$ by keeping M/C₁ and M/C_2 in high, applying the parallel data to parallel data inputs $D_0 \sim D_3$ and applying a 1-bit clock pulse to clock input T. When both M/C1 and M/C2 are kept in low, the status of the flip-flops does not change even if the clock



pulse is applied to the clock input T.

When T changes from low to high, the right shift, left shift or parallel data are read in, $Q_0 \sim Q_3$ are set low by setting direct reset input $\overline{R_D}$ low irrespective of the status of the other input signals.



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

	Operational mode	R _D	M/C ₁	M/C ₂	Τ.	D _{SR}	D _{SL}	$D_0 \sim D_3$	Q ₀	Q ₁	Q ₂	Q ₃
	Direct reset	L	Х	Х	Х	×	Х	Х	L	L	L	L
		Н	Н	L	1	L	Х	Х	L	Q ₀ 0	Q1 ⁰	Q2 ⁰
İ.	Right shift	Н	н	L	1	н	X	Х	н	Q ₀ 0	Q1 ⁰	Q2 ⁰
		н	L	Н.	1	X	L	Х	Q ₁ 0	Q2 ⁰	Q3 ⁰	L
	Left shift	Н	.L	н	1	Х	н	X	Q ₁ 0	Q ₂ 0	Q ₃ 0	н
	Parallel read	н	н	Н	1	Х	×	D ₀ ~D ₃	D ₀	D ₁	D ₂	D ₃
	Clock inhibit	• н	L	L	×	×	х	X.	Q ₀ 0	Q1 ⁰	Q ₂ 0	Q3 ⁰

Note 1. ↑: Transition from low to high (positive edge trigger)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
V _O	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	င

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Complead	Demania	Parameter		Limits			
Symbol	Parame			Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Тон	High-level output current	V _{OH} ≧2.7V	. 0		- 400	μΑ	
	Low-level output current	V _{OL} ≦0.4V	0		4	mΑ	
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter				Limits		11-1-
Symbol	rai aine ter	Test conditi	ons	Min	Тур. 🛊	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage	•	12			0.8	٧.
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
V	High-level output voltage	V _{CC} =4.75V, V _I =0.8	BV	2.7	3.4		V
Voh	riigh-level output voltage	$V_1 = 2V$, $I_{OH} = -400$	ıΑ.	2.7	3.4		V
	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mÅ		0.25	0.4	V
V _{OL}	Low-lever output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
1	High-level input current	$V_{CC}=5.25V, V_{I}=2.7$	7V.			20	μΑ
ин	righ-level input current	V _{CC} =5.25V, V _I =10V	i			0.1	mA
li_	Low-level input current	V _{CC} =5.25V, V _I =0.4	IV .	T .		-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0	V	- 20		— 100	mA.
loc	Supply current	V _{CC} =5.25V (Note 3)			15	23	mA

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C.

 $[\]mathbf{Q^0}$: Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

Note 2: All measurements must be done quickly and not more than one output should be shorted at a time.

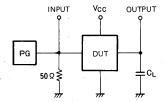
Note 3: I_{CC} is measured after $D_0 \sim D_3$ have been set to OV, D_{SR} , D_{SL} , M/C_1 , M/C_2 and $\overline{R_D}$ to 4.5V and T to 4.5V from OV.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS ($V_{\infty}=5V$, Ta=25%, unless otherwise noted)

		-		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Ollit
fmax	Maximum clock frequency		25	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation		Ī.	10	22	ns
tphL	time, from input T to outputs $Q_0 \sim Q_3$	C _L =15pF (Note 4)		12	26	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{R}_D to outputs $Q_0 \sim Q_3$			8	30	ns

Note 4: Measurement circuit

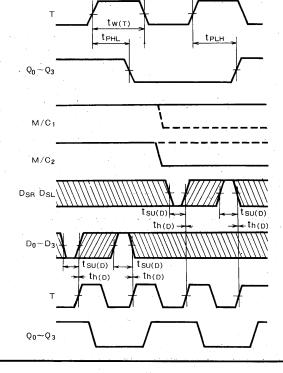


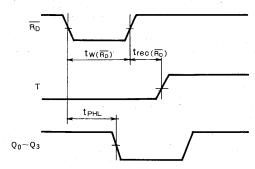
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

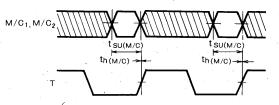
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

0 1 1				Limits		11.2
Symbol	Parameter	Test conditions	Min	Тур	. Max	Unit
tw(T)	Clock input T high pulse width		20	5		ns
tw(RD)	Direct reset input RD pulse width		20	6		ns
tsu(D)	Setup time D to T		20	7		ns
tsu(M/C)	Setup time M/C ₁ , M/C ₂ to T		30	. 12		ns
th(D)	Hold time D to T		0	– 3		ns
th(M/C)	Hold time M/C ₁ , M/C ₂ to T	,	0	- 6		ns
trec(RD)	Recovery time to direct reset		25	3		ns

TIMING DIAGRAM (Reference level = 1.3V)







Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance. The broken liners for M/C_1 and M/C_2 indicate three timings for left shifting. Setup time D_{SR} is for Q_0 only; setup time D_{SL} is for Q_3 only

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS195AP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function with a direct reset input.

FEATURES

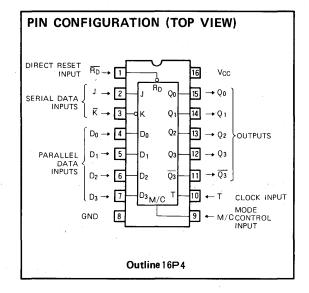
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Serial inputs J and K provided
- Direct reset input provided
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

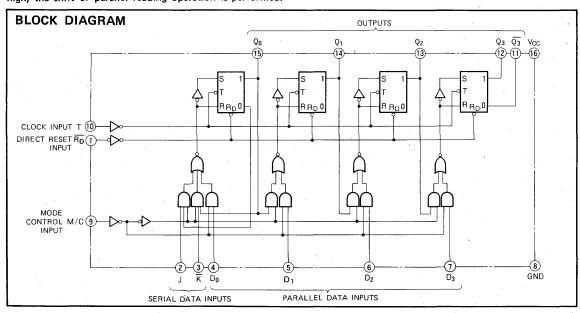
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in high, the serial data are applied to serial data inputs J and \overline{K} and the clock pulse is applied to clock input T, the serial data are shifted sequentially into outputs $O_0 \sim \overline{O}_3$ in synchronization with the clock pulse. The first stage flip-flop with J and \overline{K} functions as a J-K flip-flop. When serial data are applied from line 1, J and \overline{K} are mutually connected and used as serial input pins. When M/C is kept in low, the parallel data are applied to parallel data inputs $O_0 \sim O_3$ and a 1-bit clock pulse is applied to T, the $O_0 \sim O_3$ signals appears in $O_0 \sim \overline{O}_3$. When T changes from low to high, the shift or parallel reading operation is performed.



The last stage flip-flop output has mutually complementary outputs Q_3 and $\overline{Q_3}$, $Q_0 \sim Q_3$ are reset low and $\overline{Q_3}$ high by setting direct reset input $\overline{R_D}$ low irrespective of all the other input signals.



4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

Operational mode	T	RD	M/C	J	K	D ₀ ~D ₃	Q ₀ .	Q ₁	Q ₂	Q ₃	Q ₃
Direct reset	×	L	×	×	Х	X	L	L	L	L	н
	1	Н	Н	н	Н	X	Н	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q ₂ 0
Distantia	1	Н	Н	L	L	×	L	Q ₀ 0	Q10	Q ₂ 0	Q ₂ 0
Right shift	1	Н	Н	н	L	×	$\overline{Q_0}$	Q ₀ 0	Q10	Q ₂ 0	Q ₂ 0
	1	н	Н	L	• н	Х	Q ₀ 0	Q_0^0	Q ₁ 0	Q ₂ 0	$\overline{Q_2^0}$
Parallel read	1	Н	L	×	×	D ₀ ~D ₃	D ₀	D ₁	D ₂	D ₃	D ₃

Note 1. ↑: Transition from low to high (positive edge triggering)

Q0: Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	٧
Vo	Output voltage	High-level output	-0.5~ V _{CC}	Y
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		11.25			
Symbol	. rarameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
loH	High-level output current	V _{OH} ≥2.7V	0		-400	μА
1	Low-level output current	V ₀ L≦0.4V	0		4.	mΑ
loL	Low-level output current	V ₀ L≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T	lista			Unit	
Symbol	Parameter	l est cond	Test conditions			Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8.	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	٧
V _{OH}	High-level output voltage	V _{CC} =4.75V, V _I =0. V _I =2V, I _{OH} =-400		2.7	3.4		V
VoL	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I =2V	I _{OL} = 4mA		0.25	0.4	V
	High Invalidation	V _{CC} =5.25V, V _I =2.	7V			20	μА
ΙΗ	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4	4 V			-0.4	mA
lós	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _C =0V	/	- 20		<u> </u>	mA
Icc	Supply current	V _{CC} =5.25V (Note 3)			14	21	mA

^{* :} All typical values are at V_{CC} =5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

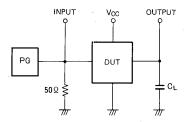
Note 3: I_{CC} is measured with M/C at OV, J, \overline{K} and $D_0 \sim D_3$ at 4.5V, with \overline{R}_D kept at 4.5V after changing from OV and after changing T from OV to 4.5V.

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock frequency		- 30	60	,	MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	22	ns
t _{PHL} .	time, from input T to outputs $Q_0 \sim Q_3$, $\overline{Q_3}$			12	26	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{R}_D to output $Q_0 \sim Q_3$	C _L =15pF (Note 4)		14	30	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output $\overline{Q_3}$			12	30	ns

Note 4: Measurement circuit

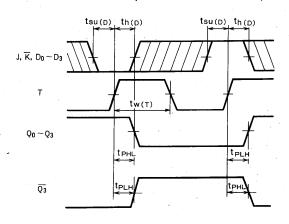


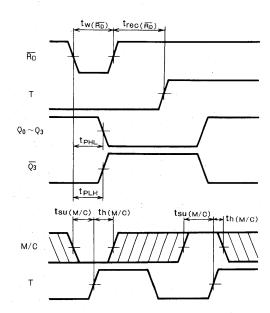
- (1) The pulse generator has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		, Limits			
Symbol	Farameter	Test conditions	Min	Тур	Max	Unit	
t _W (T)	Clock input T high pulse width		16	10		ns	
tw(RD)	Direct reset RD pulse width		12	6		ns	
t _{SU} (D)	Setup time input data to T]	15	3	1	ns	
t _{SU(M/C)}	Setup time M/C to T		25	10		ns	
t _{h(D)}	Hold time input data to T		3	-1		ns	
th (M/C)	M/C hold time to T		0	-7		ns	
trec(RD)	Direct reset recovery time to T		25	5		ns	

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

DESCRIPTION

The M74LS196P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset input and preset input.

FEATURES

- Direct reset input and asynchronous preset input provided
- Usable independently as binary and divide-by-five counter
- High-speed counting (f_{max} = 80MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

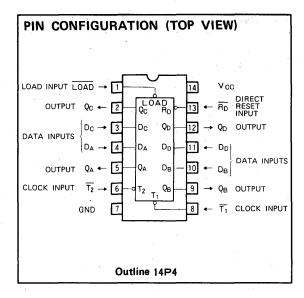
APPLICATION

General purpose, for use in industrial and consumer equipment.

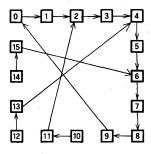
FUNCTIONAL DESCRIPTION

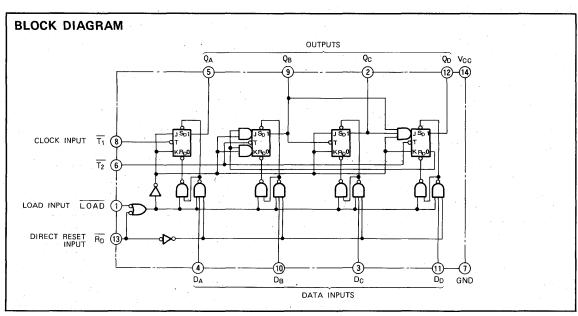
This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a BCD code appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The counter can be preset by applying data to data inputs D_A , D_B , D_C and D_D and by setting \overline{LOAD} input low, and the D_A , D_B , D_C and D_D signals appear in Q_A , Q_B , Q_C , Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs. When preset to a numerical value of 10 or above, the count proceeds in accordance with the status transition figure.



STATE DIAGRAM





For resetting, it is possible to set $Q_A = Q_B = Q_C = Q_D =$ low by setting direct reset input R_D low irrespective of the status of the other inputs.

FUNCTION TABLE (Note 1)

Ŧ	R _D	LOAD	QΔ	Qв	Qс	Qр
×	L	Х	L	L	L	L
×	н	L	DA	DΒ	Dc	D _D
1	н	I		Cou	unt	

Note 1 \(\preceq : Transition from high to low (negative edge trigger)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS

($T_a = -20 \sim +75 \, ^{\circ} \! \text{C}$, unless otherwise noted)

number	QA	Qв	Qc	QD
0	L	L	L	L
1	н	L	L	L
2	L	н	L	L
3	н	I	Г	L
4	L	٦	I	L
5	н	Ė.	Н	L
6	L	, H	· H	L
7	ı	Н	Ŧ	L
8	L	, F	L	Н
9	. н	L	L	Н

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
	V _I Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5	
VI		Inputs LOAD, RD, DA~DD	-0.5~+15	- v
Vo	Output voltage	High-level state	-0.5~ Vcc	V .
Topr	Operating free-air ambient temperature range		-20~+75	°C
T _{stg}	Storage temperature range		-65~+150	°

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter			Limits			
Зульы	rarame	eter	Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	٧		
Ion	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ	
		V _{OL} ≦ 0.4 V	0		4	mA	
FOL	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

Cb. a.l	Parameter		T			Limits		Unit
Symbol		Parameter	Test condi	tions	Min	Typ ∗	Max	Unit
ViH	High-level input vo	tage			2			٧
VIL	Low-level input vol	tage					0.8	٧
Vic	Input clamp voltag	е	V _{CC} =4.75V, I _{IC} =-1	8mA			- 1.5	V
V _{OH}	High-level output v	roltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		٧
		- 14	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VOL	Low-level output ve	ortage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V .
	LOAD, DA,	LOAD, DA, DB, DC, DD					20	μΑ
		T ₁ , R _D	V _{CC} =5.25V, V _I =2.7\	/			40	
	High-level	T ₂					80	
lін	input current	T ₁		<u> </u>			0.2	
		T ₂	$V_{CC}=5.25V, V_{I}=5.5V$	/			0.4	
		LOAD, DA, DB, DC, DD	V 5 05) / V 40)				0.1	mA
_		RD	$V_{CC} = 5.25V, V_I = 10V$				0.2	,
	14	LOAD, DA, DB, DC, DD					-0.4	
	Low-level	RD					-0.8	
HL	input current	input current T ₁	VCC=5.25V, VI=0.4V	$V_{CC} = 5.25V, V_I = 0.4V$			-2.4	mA _
		Tz					-2.8	
los	Short-circuit outpu	t current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		- 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			16	27	mA

All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

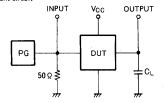
Note 3: I_{CC}is measured with all inputs at 0V.



SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, Ta = 25 C, unless otherwise noted)

0		Test conditions	Limits			Unit
Symbol	Parameter	l est conditions	Min ⁻	Тур	Max	Unit
f _{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A		30	80		MHz
f _{max}	Maximum clock frequency, from input \overline{T}_2 to output Q_B			25		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			9	15	ns
t _{PHL}	propagation time from input $\overline{T_1}$ to output Q_A			8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			10	24	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_B			10	33	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	·		20	57	ns
t _{PHL}	propagation time, from input T ₂ to output Q _C	C ₁ = 15pF (Note 4)		17	62	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L = 15pF (Note 4)		10	18	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D			9	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs DA, DB, DC, DD			9	30	ns
t _{PHL}	to outputs QA, QB, QC, QD			. 11	44	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input input LOAD to outputs			14	41	ns
t _{PHL}	QA, QB, QC, QD			10	45	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs Q_A , Q_B , Q_C , Q_D			14	51	ns

Note 4: Measurement circuit

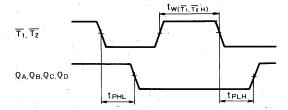


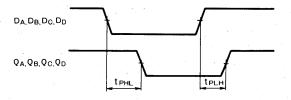
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

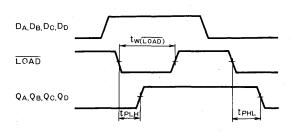
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

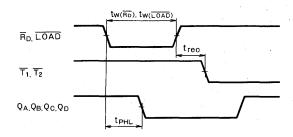
Symbol	Parameter	Total conditions	1.5	Limits		
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width		. 20	5		ns .
tw(T₂H)	Clock input T ₂ high pulse width		30	17		ns
tw (LOAD)	Load LOAD input pulse width		20	8		ns
tw(RD)	Direct reset RD pulse width		15	4		ns
tsu(DL)	Setup time DA~DD low to LOAD		15	3		. ns
t _{su(DH)}	Setup time DA~DD high to LOAD	C	10	0		ns
th(DL)	Hold time DA~DDlow to LOAD		6	0		ns
th(DH)	Hold time D _A ~D _D high to LOAD		3	-1		ns
trec(LOAD)	Recovery time LOAD to T		30	7		ns
trec(AD)	Recovery time RD to T		30	7		ns

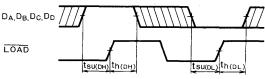
TIMING DIAGRAM (Reference level = 1.3V)







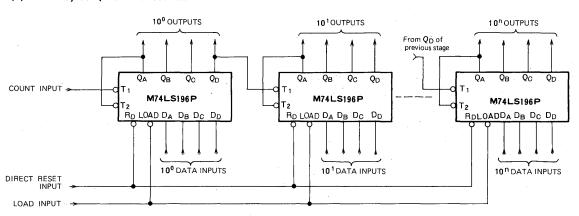




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLES

(1) Divide-by-10ⁿ presettable counter

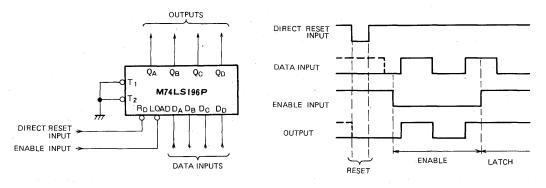


The above counter can be configured by connecting n + 1 M74LS196P devices. It operates at a high speed (60MHz typical) but since the system is synchronous, the time during which the output

changes with respect to the input is delayed in accordance with the following formula.

The delay time (typical) of each output at the Mth stage is:

(2) Use as a latch



DESCRIPTION

The M74LS197P is a semiconductor integrated circuit containing an asynchronous hexadecimal (4-bit binary) counter function with direct reset and preset inputs.

FEATURES

- Direct reset input and asychronous preset input provided
- Usable independently as binary and octal counter
- High-speed counting (fmax= 80MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

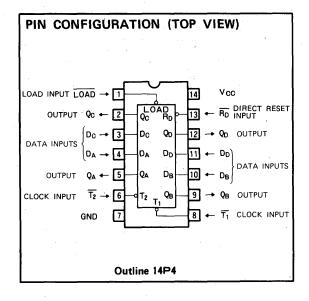
General purpose, for use in industrial and consumer equipment.

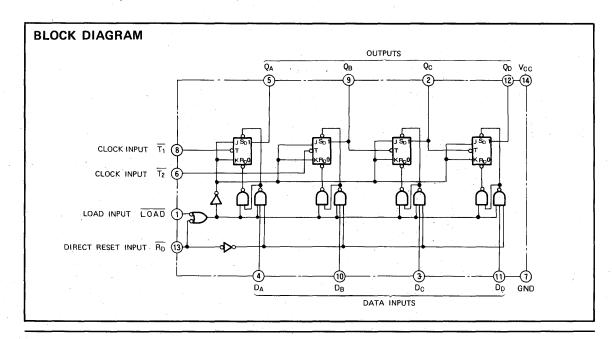
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a 4-bit pure binary code appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The counter can be preset by applying data to data inputs D_A , D_B , D_C and D_D and by setting \overline{LOAD} input low, and the D_A , D_B , D_C and D_D signals appear in Q_A , Q_B , Q_C , Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs.

For resetting, it is possible to set $Q_A = Q_B = Q_C = Q_D = 1$ low by setting direct reset input \overline{R}_D low irrespective of the status of the other inputs.





FUNCTION TABLE (Note 1)

Ť	R_{D}	LOAD	QA	Qв	Qc	Q _D
Χ.	L	X	L	٦	L	L
Х	н	L	DA	DB	Dc	D _D
1	Н	н		Cou	ınt	

Note 1 ↓ : Transition from high to low (negative trigger)

X : Irrelevant

Count number	Q _A	Qв	Qc	Q_{D}
0	L	L	L	L
1	Ι	L	L	L
2	L	Н	L	L
3	Ι	н	L	· L
4	L	L	Н	L
5	I	L	н	L
6	L	н	Н	L
7	Η	Н	Н	L
8	L	L	L	. н
9	Н	Ľ	L	Н
10	L	н	ĻL	Н
11	Н	Н		н
12	L	L	Η	Н
13	Ι	_	Ξ	н
14		Η	Н	Н
15	H	Н	H	Н
	. —			

⁽¹⁾ Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS (Ta = $-20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
	V _I Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	-0.5~+5.5		
VI		Inputs LOAD, RD, DA~DD	-0.5~+15	1. V	
Vo	Output voltage	High-level state	-0.5~V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~ + 150	r	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75 \,^{\circ}C$, unless otherwise noted)

01	Parameter			Limits			
Symbol	rarame	ter	Min	Тур	Max 5.25 - 400	Unit	
Vcc	Supply voltage		4.75	5	5.25	. V	
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μА	
		V _{OL} ≦0.4V	0		4	mA	
TOL	Low-level output current	V _{OL} ≦0.5V	0		.8	mΑ	

ELECTRICAL CHARACTERISTICS (Ta = −20~+75°C, unless otherwise noted)

0	the second				Limits		4	
Symbol		Parameter	Test condit	ions	Min	-Typ ≠	Max	Unit
VIH	High-level input vol1	age	T :		2			٧
VIL	Low-level input volt	age					0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	18mA			- 1.5	V
Vон	High-level output vo	ltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		٧
		lana.	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
V _{OL}	Low-level output vo	rtage	$V_1 = 0.8V, V_1 = 2V$ $I_{0L} = 8 \text{ mA}$			0.35	0.5	V
		LOAD, DA, DB, DC, DD	V . 5 05V V - 0 7				20	
		\overline{R}_D , \overline{T}_1 , \overline{T}_2	$V_{CC} = 5.25V, V_1 = 2.7V$				40	μΑ
I _{IH}	High-level input current	T ₁ , T ₂	V _{CC} =5.25V, V _I =5.5V	v			0.2	
	Input current	LOAD, DA, DB, DC, DD	V _{CC} =5.25V, V _I = 10V	,			0.1	mA .
		RD	VCC-5.25V, V - 10V				0.2	
		LOAD, DA, DB, DC, DD					-0.4	
1 V	Low-level	RD	$V_{CC}=5.25V, V_{I}=0.4V$	V			-0.8	. mA
li <u>L</u> .	input current	input current T ₁					-2.4	mA
		T ₂	7				-1.3	
los	Short-circuit output	current (note 2)	V _{CQ} =5.25V, V _O = 0 \	/	- 20		100	mΑ
Icc	Supply current		V _{CC} =5.25V (Note 3)			16	27	mΑ

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

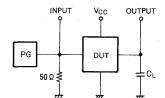
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit	
Symbol	, and the contract of	lest conditions	Min	Тур	Max	0,,,,
fmax	Maximum clock frequency(T ₁)		30	80	,	MHz
fmax	Maximum clock frequency $(\overline{T_2})$]		35		MHz
tpLH	Low-to-high-level, high-to-low-level output			6	15	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_A			7	21	ns
tp∟н	Low-to-high-level, high-to-low-level output			8	19	ns
t PHL	propagation time, from input T2 to output QB			8	35	ns
t PLH	Low-to-high-level, high-to-low-level output	C _L = 15pF (Note 4)		15	51	ns
t PHL	propagation time, from input T ₂ to output Q _C	OL-13bi (Mote 4)	· .	15	63	ns
tpLH	Low-to-high-level, high-to-low-level output			22	78	ns
t PHL	propagation time, from input $\overline{T_2}$ to output Q_D			24	95	ns
t _{PLH}	Low-to-high-level, high-to-low-level output		Ĺ	8	27	ns
tPHL	propagation time, from inputs DA, DB, DC, DD to outputs QA, QB, QC, QD	1.2		. 10	44	ns
tpLH	Low-to-high-level output propagation time, from			13	39	ns
t PHL	input LOAD to outputs QA, QB, QC, QD			10	45	ns
tpHL	High-to-low-level output propagation time, from input \overline{R}_D to outputs Q_A , Q_B , Q_C , Q_D			13	51	ns

Note 4: Measurement circuit

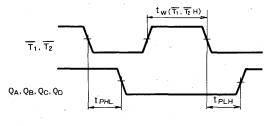


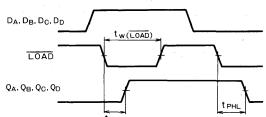
- (1) The pusle generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_{P-P} , Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

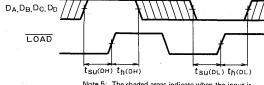
TIMING REQUIREMENTS (V_{CC}= 5 V, Ta = 25°C, unless otherwise noted)

C	Parameter	T		Limits		11-14
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width		20	5		ns
tw(TzH)	Clock input T ₂ high pulse width		30	14		ns
tw(LOAD)	Load LOAD input pulse width		20	8		ns
tw(RD)	Direct reset RD pulse width		15	4		ns
t _{su(DL)}	Setup time DA~DD low to LOAD	1	15	3		ns
t _{su(DH)}	Setup time DA~DD high to LOAD		10	. 0		ns
th(DL)	Hold time DA∼DD low to LOAD		6	0		ns
th(DH)	Hold time D _A ∼D _D high to LOAD	1	3	-1		ns
trec(LOAD)	Recovery time LOAD to T	1	30	. 7.		ns
trec(RD)	Recovery time R _{D.to} T	1	30	7		ns

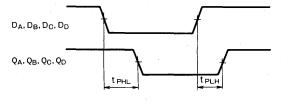
TIMING DIAGRAM (Reference level = 1.3V)

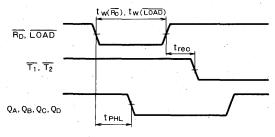






Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.





DESCRIPTION

The M74LS221P is a semiconductor integrated circuit containing two monostable multivibrator circuits with direct reset inputs.

FEATURES

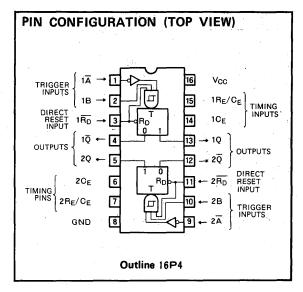
- Pulse width excellent temperature characteristics and supply voltage
- Schmidt trigger inputs (B inputs) provided
- Wide output pulse width range ($t_w = 47 \text{ns} \sim 1 \text{s}$)
- Operation possible with duty cycle up to 90% $(R_T=100k\Omega)$
- Direct reset inputs provided
- A, B complementary inputs provided
- Q and Q outputs
- High input breakdown voltage (V_I≥15V)
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

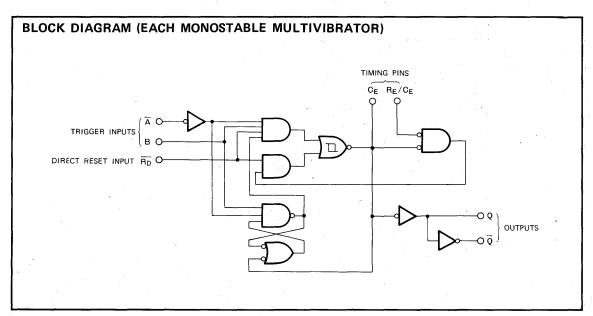
FUNCTIONAL DESCRIPTION

Positive pulses appear in output Q and negative pulses in output \overline{Q} by connecting external resistor R_T and electrostatic capacitor C_T to timing pins R_E/C_E and C_E , as shown in Fig. 1, and by applying a trigger from input \overline{A} or B. The width t_w of the pulses appearing in the outputs is set by R_T and C_T . When \overline{A} changes from high to low or when B changes from low to high, the trigger is applied. This IC is able to obtain an output pulse width with excellent supply

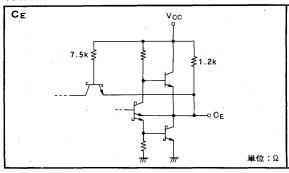


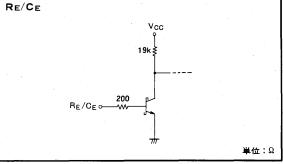
voltage and temperature characteristics since both its supply voltage and temperature are assured.

Q can be reset immediately low and \overline{Q} high by setting direct reset input \overline{R}_D low irrespective of the status of the outputs. If \overline{R}_D changes from low to high when \overline{A} is low and B is high, the trigger is applied and the pulse appears in the output.



TIMING PIN EQUIVALENT CIRCUIT





FUNCTION TABLE (Note 1)

R _D	Ā	В	Q	Q
. L	Х	X	L	Н
X	Н	×	L.	Н
X	х	L	L	Н
Н	L	1	Л	7.
н	ļ .	н	Ţ	T
1	L	′ н	ŗ	Ţ

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and electrostatic capacitor C_T are connected to timing pins R_E/C_E and C_E . Connect the negative to the R_E/C_E side and the positive to the C_E side when using C_T with polarity.

Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

Note 1. ↑: Transition from low to high.

 \downarrow : Transition from high to low.

Positive one-shot operation.

Negative one-shot operation.

X: Irrelevant

2. Output pulse width tw

The output pulse width t_{W} is set using R_{T} and C_{T} by the following formula:

$$t_W = C_T \cdot R_T \cdot \ln 2 \text{ (ns) } X \text{ (1 ± 0.1)}$$

 $\simeq .0.7C_T \cdot R_T \text{ (ns) } X \text{ (1 ± 0.1)}$

 $R_{\rm T}$ is measured in kiloohms and $C_{\rm T}$ in picofarads. Individual fluctuations of +10% may occur in products.

Depending on the product, fluctuations in the order of 3/-10% may occur.

3. Precautions with use

In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_{T} and C_{T} wiring as short as possible and avoid signal wires which may be conducive to noise.

Connect a capacitor of $0.01 \sim 0.1 \mu F$ with good high-frequency characteristics between pins V_{CC} and GND. Mount this capacitor as close as possible to the IC.

ABSOLUTE MAXIMUM RATINGS (Ta = -20 - +75 %, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V _I	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	٧.
Topr	Operating free-air ambient temperature range		-20~+75	ဗ
Tstg	Storage temperature range		- 65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \,^{\circ}$ C, unless otherwise noted)

6	Parameter			Limits				
Symbol	Para	meter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Тон	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ		
		V _{OL} ≦0.4V	0	:	4	mA		
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA		
R _{T.}	External timing resistance		1.4		100	kΩ		
Ст	External timing capacitance		0		1000	μF		

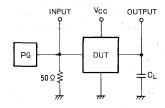
Complete	D		Task condition			Limits		Unit V V V V V
Symbol	Parameter		lest condition	Test conditions		Typ ★	Max	Onit
ViH	High-level input voltage				2			
.,		Ā, B					0.8	
VIL	Low-level input voltage	R _D					0.5	ν.
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	mA			— 1.5	V
.,	18-1-1-1-1-1-1		$V_{CC}=4.75V, V_{I}=0.5,$	0.8	0.7	3.4		
VoH	High-level output voltage		$V_1 = 2V$, $I_{OH} = -400 \mu A$		2.7	3.4		٧.
1/-	Low level output valtere		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage		$V_1 = 0.5 V, 0.8 V, V_1 = 2 V$	I _{OL} =8mA		0.35	0.5	٧
	Lieb level input ourrent		V _{CC} =5.25V, V _I =2.7V				20	μΑ
IIН .	High-level input current		V _{CC} =5.25V, V ₁ =10V				0.1	mΑ
		Ā	V _{CC} =5.25V				-0.4	
. fic	Low-level input current	B, RD	V ₁ = 0.4 V			*.	-0.8	mΑ
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O = 0 V	,	-20		— 100	mΑ
	Supply current (static state)		V _{CC} =5.25V	1 1 1		4.7	11	mΑ
lcc	Supply current (one-shot stat	e)	V _{CC} =5.25V			19	27	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits		Unit
Symbol	1 at at the ter		rest conditions	Min	Тур	Max	Oilit
t _{РLН}	Low-to-high-level output propagation time, from input \overline{A} to output Q	-			27	70	ns
tpLH	Low-to-high-level output propagation time, from input Bto output Q				24	55	ns
tenL	High-to-low-level output propagation time, from input \overline{A} to output $\overline{\overline{Q}}$	$C_T=80pF$ $R_T=2k\Omega$ $C_L=15pF$ (Note 3)		30	80	ns	
t₽HL	High-to-low-level output propagation time, from input B to output \overline{Q}		(Note 3)		26	65	ns
tрцн	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output \overline{Q}				23	65	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q				18	55	ns
two(min)	Minimum output pulse width, from inputs \overline{A} , B to outputs Q, \overline{Q}	$C_T = 0_D F$, R $C_L = 15_D F$ (20	30	70	ns
1		0 -15-5	$C_T = 80pF, R_T = 2k\Omega$	70	120	150	ns
two	Output pulse width, from inputs \overline{A} , B to outputs Q, \overline{Q}	C _L = 15pF (Note 3)	$C_T = 100 pF, R_T = 10 k \Omega$	600	670	750	ns
		(Note 3)	$C_T = 1 \mu F$, $R_T = 10 k \Omega$	- 6	6.9	7.5	ms

Note 3: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_r =6ns, t_w =40ns, V_P =3 $V_{P,P}$, Z_O =50 Ω

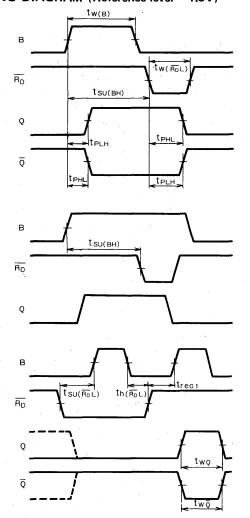
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

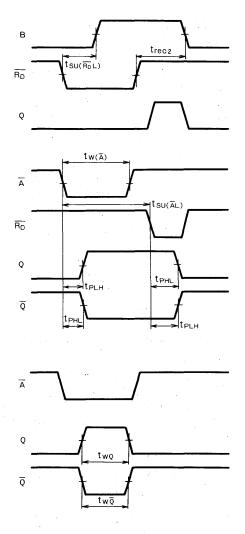
⁽²⁾ C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

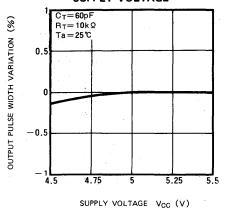
	•		7	Test conditions	* * *		Limits		Unit
Symbol	Parameter			rest conditions		Min	Тур	Max	. 01111
		Ā				1			V/μs
tr, tf	Maximum rise, fall voltage rate of inp	Ut pulse B	٠.			1			V/s
tw(Ā)	Trigger A pulse width		,			40	35		ns
tw(B)	Trigger B pulse width					40	35		ns
tw(RD)	Direct reset input pulse width		-			40	9		ns
O.D.C	O stand data and a	R _T =2kΩ						50	%
0.0.0	Output duty cycle	R _T = 100kΩ	(Note 3)					90	%
tsu(ĀL)	Setup time A low to RD					60	33		ns
tsu(BH)	Setup time B high to RD					60	25		ns
tsu(RDL)	Setup time RD low to B					50	15		ns
trec 1	Recovery time					15	– 5		ns
trec 2	Recovery time (when B is superimpos	ed onto $\overline{R_D}$)	-			50	30		ns
th(RDL)	Hold time RD low to B					0	— 15		ns

TIMING DIAGRAM (Reference level = 1.3V)

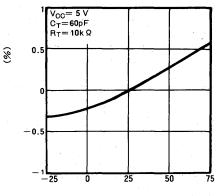




OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



AMBIENT TEMPERATURE Ta (℃)

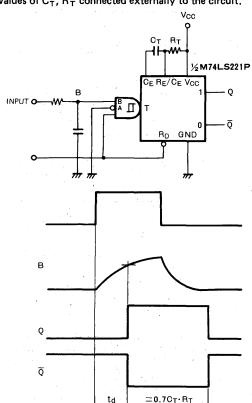
APPLICATION EXAMPLES

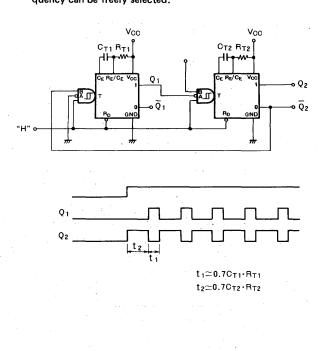
(1) Delay circuit

By connecting an integration circuit to the B input, a rectangular waveform applied to the input is changed to the waveform shown at B and delayed by time t_d . The width of the pulse output at Q and Q is determined as usual by the values of C_T , R_T connected externally to the circuit.

(2) Pulse generator

Using the fact that the output pulse width of the M74LS221P varies only slightly with changes in supply voltage and ambient temperature, a pulse generator with good supply voltage and temperature stability can be implemented. By choosing the values of externally connected components C_{T} and R_{T} , the duty cycle and frequency can be freely selected.

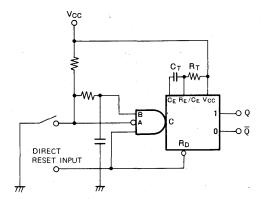


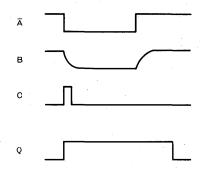


MT4LS221P

DUAL MONOSTABLE MULTIVIBRATOR

(3) ANTI-CHATTERING CIRCUIT





OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

DESCRIPTION

The M74LS240P is a semiconductor integrated circuit containing 2 blocks of buffers with 3-state inverted output and common output control input for all 4 discrete circuits.

FEATURES

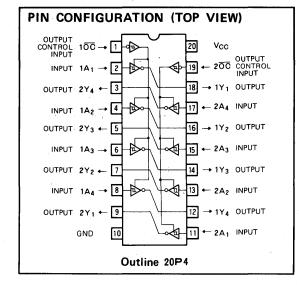
- Small input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage (V₁≥5V)
- Output control input having same phase for 2 circuits. (10C, 20C)
- High fan-out, 3-state output.
 (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. $(T_a = -20^{\circ} + 75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuits has enabled the achievement of small input load factor and high breakdown input voltage. With hysteresis characteristics, the buffer has a 3-state inverted output with high noise margin. When the output control input \overline{OC} is low, high appears in the output Y if input A is low, and low appears in the Y if A is high. If, on the other hand, \overline{OC} is high, all the outputs Y_1, Y_2, Y_3 , and Y_4 are in a high-impedance state, irrespective of the status of A.



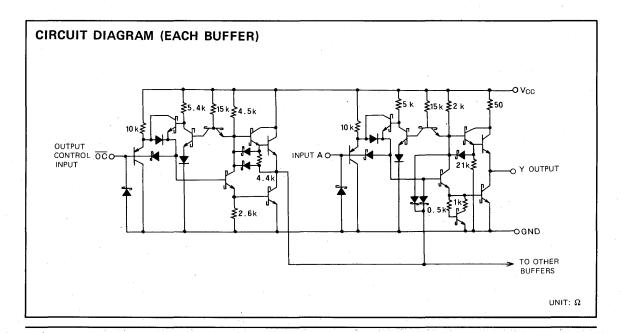
By connecting $1\overline{OC}$ with $2\overline{OC}$, it becomes possible to control the output of the 8 circuits. The output can be terminated with load resistor of 133Ω or over.

FUNCTION TABLE (Note 1)

Α	ÖC	Y
L	L	Н
Н	L	L
Х	н	Z

Note 1: Z: high-impedance

X: irrelevant



OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		−65 − + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

			Limits		Unit	
Symbol	Parame	ter .	Min	Onn		
Vcc	Supply voltage		4.75	5	Max 5.25 — 3 — 15 — 12 — 24	V
		V _{0H} ≧2.4V	0		-3	mA
ЮН	High-level output current	V _{OH} ≧ 2 V	0	-	- 15	mA
	Low-level output current	V _{OL} ≤0.4V	0		12	mA
IOL		V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

		—	Ì	Limits		Unit
Symbol	Parameter	Test conditions	Min	Typ*	Max	Unit .
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _T + -V _T	Hysteresis	V _{CC} =4.75V	0.2	0.4		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-I.5	V
.,	High-level output voltage	$V_{CC} = 4.75V \mid V_{I} = 0.8V, I_{OH} = -3$	mA 2.4	3.4		V
Voн	High-level output voltage	$V_{I}=2V$ $V_{I}=0.5V, I_{OH}=-1!$	5mA 2			V
· ·	Low-level output voltage	V _{CC} =4.75V I _{OL} =12m	Α	0.25	0.4	V
V _{OL}	Low-level output voltage	V _I =0.8V, V _I =2V I _{OL} =24m	Α	0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _O =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V, V _O =0.4V			-20	μА
	High-level input current	V _{CC} =5.25V, V _I =2.7V			20	V V V V V V V V V V V V V V V V V V V
l _{IH}	riigii-leveriiiput current	V _{CC} =5.25V, V _I =10V			0.1	mA
I _I L	Low-level input current	V _{CC} =5.25V, V ₁ =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	-40		-225	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V		17	27	mA
ICCL	Supply current, all outputs low	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		26	44	mA
locz	Supply current, all outputs off	V _{CC} =5.25V, V _I =4.5V		29	50	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

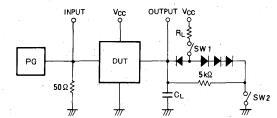
$\textbf{SWITCHING} \ \ \textbf{CHARACTERISTICS} \ \ (V_{CC} = 5V, \ Ta = 25^{\circ}C, \ \ \text{unless otherwise noted})$

Symbol		Test conditions	Limits			Unit
Symbol	Parameter	l est conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		. 7	-14	ns
t _{PHL}	time, from input A to output Y	(Note 3)		9	18	ns
t _{PZL}	Output enable time to low-level	$R_{L} = 667\Omega$, $C_{L} = 45pF$ (Note 3)		15	30	ns
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	. R _L =667Ω, C _L = 5 pF (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		12	18	ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

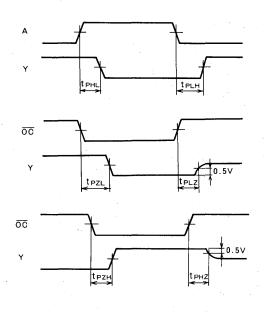
Note 3: Measurement circuit



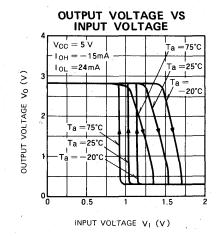
Parameter	SW 1	SW2
t pzh -	Open	Closed
t PZL	Closed	Open
tpLZ .	Closed	Closed
t pHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

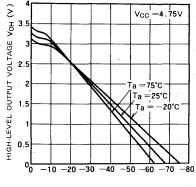
TIMING DIAGRAM (Reference level = 1.3V)



TYPICAL CHARACTERISITCS

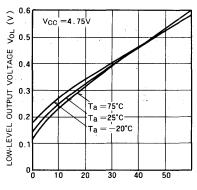


HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



HIGH-LEVEL OUTPUT CURRENT IOH (mA)

LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT CURRENT IOL (mA)

MITSUBISHI LSTTLS M74LS241P

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS241P is a semiconductor integrated circuit containing 2 buffer blocks with 3-state non-inverted outputs and is provided with output control inputs which are common to 4 circuits and which are independent.

FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (=400mV typical)
- High breakdown input voltage (V₁ ≥ 15V)
- Complementary output control inputs (100, 200)
- High fan-out 3-state outputs
 (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range (T_a=-20~+75°C)

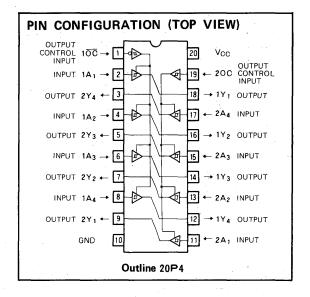
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

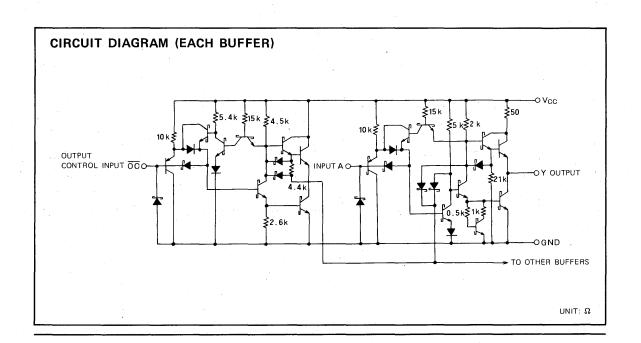
Since pnp transistors are used for the input circuits, the input load factor is small and a high breakdown input voltage is provided. The 3-state non-inverted output buffers have a high noise margin due to hysteresis.

When $1\overline{OC}$ is low, low appears in output Y if input 1A is low, and high appears in Y if 1A is high. When 2OC is high, low appears in output 2Y if input 2A is low and high



appears in 2Y if 2A is high. All the outputs are put in a high-impedance state when $1\overline{OC}$ and 2OC are high and low, respectively.

The device can be used as a 4-bit two-way bus driver by connecting $1\overline{OC}$ and 2OC, 1A and 2Y and also 2A and 1Y. The outputs can be terminated with load resistors of not less than 133 ohms.



OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

	1A	1 <u>00</u>	1Y
Г	L	L	L
	н	L	Н
Г	.X	H	Z

2A	20C	2Y
L	н	L
н	,H	н
Х	L	Z

Note 1 Z : High-impedance

X: irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V -
Vo	Output voltage	Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		-20-+75	°C
Tstg	Storage temperature range		-65~ + 150	℃ .

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter						
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	- 5	5.25	V	
	1 Cab land a second	V _{OH} ≥2.4V	0		-3	mA	
юн	IOH High-level output current	VoH≥ 2 V	V _{OH} ≧ 2 V	0		-15	mA
	I _{OL} Low-level output current	V _{OL} ≤0.4V	0		12	mA	
IOL		V ₀ L≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Complete	Parameter	Tara and Mala		Limits		
Symbol	Parameter	Test conditions	Min	Тур 🗱	Max	Unit
V _{IH}	High-level input voltage		2			V
,V _{IL}	Low-level input voltage				0.8	V
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V	0.2	0.4		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
V	High-level output voltage	$V_{OO} = 4.75V$ $V_{I} = 0.8V$, $I_{OH} = -3mA$	2.4	3.1	÷	V
V _{OH}	High-level output voltage	$V_1 = 2V$ $V_1 = 0.5V$, $I_{OH} = -15 \text{ m/s}$	2			·V
V	Low-level output voltage	V _{CC} =4.75V I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	V _I =0.8V, V _I =2V I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _C =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V, V _C =0.4V			-20	μА
1	High level input gurrent	V _{CC} =5.25V, V _I =2.7V			20	μА
liH	High-level input current	V _{CC} =5.25V, V _I =10V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{OO} =5.25V, V _O =0V	-40		-225	mA
Госн	Supply current, all outputs high	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		17	27	mA
I CCL	Supply current, all outputs low	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$		27	46	mA
locz	Supply current, all outputs disabled	V _{CC} =5.25V, V _I =0V, V _I =4.5V		32	54	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

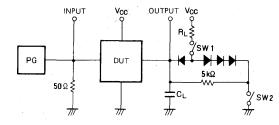
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

Symbol		T	Limits			Unit
	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		8	18	ns
t _{PHL}	time, from input A to output Y	(Note 3)		9	18	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	30	ns
t _{PZH}	Output enable time to high-level	$R_{\perp}=667\Omega$, $C_{\perp}=45pF$ (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_{\perp}=667\Omega$, $C_{\perp}=5$ pF (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)		12	18	ns

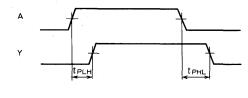
Note 3: Measurement circuit

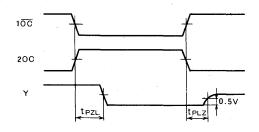


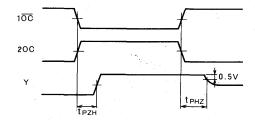
_			
	Symbol	SW 1	SW2
ſ	t PZH	Open	Closed
	t PZL	Closed	Open
ſ	t PLZ	Closed	Closed
ſ	t _{PHZ}	· Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P,P}, Z_0 = 50\Omega.$ (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



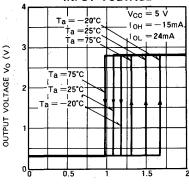




CONTROL OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

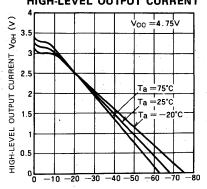
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS INPUT VOLTAGE



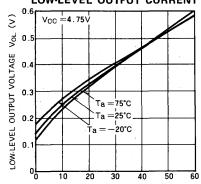
INPUT VOLTAGE VI (V)

HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



HIGH-LEVEL OUTPUT CURRENT IOH (MA)

LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT CURRENT IOL (MA)

MT4LS242P

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS242P is a semiconductor integrated circuit containing 4 bus transmitters/receivers circuit with 3-state inverted outputs.

FEATURES

- Two-way transmission for, or isolation from, two 4-bit data words
- Low input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

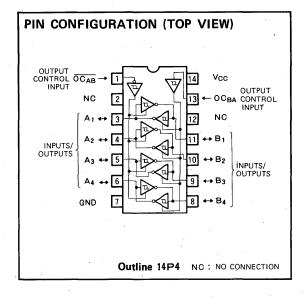
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with the 3-state inverted outputs are made two-way buffers.

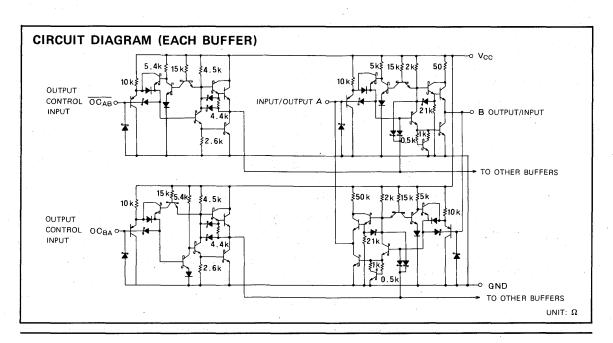
Since the input section is provided with hysteresis, the noise margin is increased and the use of pnp transistors in the inputs reduces the input load factor.

The input/output direction is controlled by $\overline{OC_{AB}}$ and OC_{BA} . When $\overline{OC_{AB}}$ and OC_{BA} are low, input/output pins A are made the input pins and the output/input pins B are made the output pins. When $\overline{OC_{AB}}$ and OC_{BA} are high, pins B are made the input pins and A the output pins. When $\overline{OC_{AB}}$ is high and OC_{BA} is low, both A



and B are put in the high-impedance state and A and B are isolated. When $\overline{OC_{AB}}$ is low and OC_{BA} is high, both A and B are put to the output state resulting in the possibility of oscillation and damage to the IC. Use in this state must therefore be avoided. This state resulting from the $\overline{OC_{AB}}$ and OC_{BA} signals should be kept as short as possible. Termination is possible with a load resistor of not less than 133 ohms.

Refer to M74LS240P for the typical characteristics.



QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

OCAB	OC _{BA}	. А	В
н	Н	ō	1
L	н	*	*
н	L	Z	Z
L	L	. 1	ō

Note 1: | Input pin

Output pin (inverted)

*: Inhibited (A and B are made output pins)

Z: High-impedance (A, B are isolated)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter Conditions		Parameter		Parameter Conditions		Limits	Unit
Voc	Supply voltage				-0.5~+7	V		
Vı	A, B				-0.5~+5.5	V		
۷į	Input voltage OC	OCAB, OCBA			-0.5∼+15	V		
Vo	Output voltage		Off-state		-0.5~+5.5	V		
Topr	Operating free-air ambient temperature range			,	-20~+75	°C		
Tstg	Storage temperature range				−65∼+150	°C		

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter					
Symbol			Min	Тур	Max	Unit .
Vcc	Supply voltage		4.75	5	5.25	V
1	V _{OH} ≥2.4V		0		-3	mA
Іон	High-level output current	V _{OH} ≧ 2 V	0		– 15	mA
	Low-level output current	V _{OL} ≦0.4V	0		12	mΑ
IOL	V _{OL} ≤0.5V		0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

	Parameter		Test conditions		Limits			Unit	
Symbol					Min	Typ *	Max	: Onit,	
V _{IH}	High-level input voltage				2			V	
V _I L	Low-level input voltage							0.8	٧
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V			0.2	0.4		٧
Vic	Input clamp voltage		V _{CC} =4.75V . I _{IC} =-18mA					-1.5	V
Voн	High-level output voltage		V _{CC} =4.75V	V _I = 0.8\	/, I _{OH} = -3mA	2.4	3.1		٧
			V ₁ =2 V	$V_1 = 0.5V$, $I_{OH} = -15mA$		2			٧
VoL	Low-level output voltage		V _{OC} =4.75V		I _{OL} =12mA		0.25	0.4	V
			V1=0.8V, V1	=2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =2.7V					40	μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =0.4V					-200	μА
Ін		A, B	V 5 25V V 2 7V				20	μA mA	
	High-level input current	OCAB, OCBA	V _{CC} =5.25V, V _I =2.7V						20
		A, B	V _{CC} =5.25V, V _I =5.5V						0.1
		OCAB, OCBA	V _{CC} =5.25V, V _I =10V				0.1		
lıL	Low-level input current	OCAB, OCBA	V F 25V					-0.2	
		Α	V _{CC} =5.25V V _I =0.4V	OCAL	B=0CBA=0V			-0.2	mA
		В		OCAL	B=OCBA=4.5V			-0.2	L
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		-40		225	mA	
Госн	Supply current, all outputs high		$V_{CC} = 5.25V, V_I = 0V, V_i = 4.5V$			22	38	mA	
ICCL	Supply current, all outputs low		$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$				29	50	mA
Iccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V, V _I =4.5V				29	50	mA

^{* :} All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

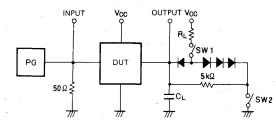


QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

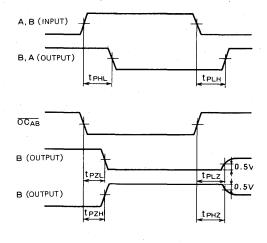
Cumbal	Symbol Parameter	Test conditions	Limits			Unit`
Symbol Parameter	Test conditions	Min	Тур	Max	Onit	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,	C _L =45pF		7	14	ns
t _{PHL}	from inputs A, B to outputs B, A	(Note 3)		9	18	ns
t _{PZL}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		15	40	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		12	40	ns
t _{PLZ}	Output enable time to low-level	R _L =667Ω, C _L = 5 pF (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$ $C_L=5$ pF (Note 3)		12	18	ns

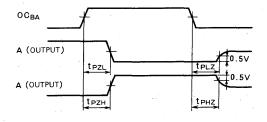
Note 3: Measurement circuit



Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50Ω
- (2) All diodes are switching diodes (trr ≤ 4ns)
- (3) C_L includes probe and jig capacitance.





QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS243P is a semiconductor integrated circuit containing 4 bus transmitters/receivers with 3-state non-inverted outputs.

FEATURES

- Two-way transmission for, or isolation from, two 4-bit data words
- Low input load factor (pnp input)
- Hysteresis provided (= 400 mV typical)
- High fan-out (I_{O1} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

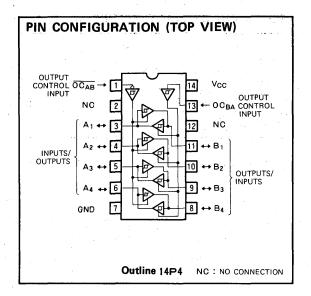
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with the 3-state non-inverted outputs are made two-way buffers.

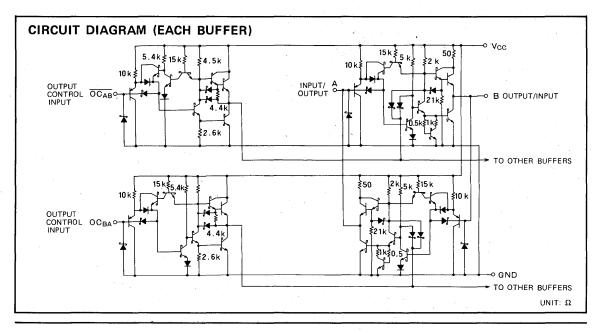
Since the input section is provided with hysteresis, the noise margin is increased and the use of pnp transistors in the inputs reduces the input load factor.

The input/output direction is controlled by $\overline{OC_{AB}}$ and OC_{BA} . When $\overline{OC_{AB}}$ and OC_{BA} are low, input/output pins A are made the input pins and the output/input pins B are made the output pins. When $\overline{OC_{AB}}$ and OC_{BA} are high, pins B are made the input pins and A the output pins. When $\overline{OC_{AB}}$ is high and OC_{BA} is low, both A and B are put in the high-impedance state and A and B are isolated. When



 $\overline{\text{OC}_{AB}}$ is low and $\overline{\text{OC}_{BA}}$ is high, both A and B are put to the output state resulting in the possibility of oscillation and damage to the IC. Use in this state <u>must</u> therefore be avoided. This state resulting from the $\overline{\text{OC}_{AB}}$ and $\overline{\text{OC}_{BA}}$ signals should be kept as short as possible. Termination is possible with a load resistor of not less than 133 ohms.

Refer to M74LS241P for the typical characteristics.



QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

OCAB	OCBA	Α	В
Н	• н	0	I
L_	Н	*	*
Н	L	Z	Z
L	L	ı	0

Note 1: | : Input pin

O: Output (non-inverted) pin

* : Inhibited (A and B are made output pins)

Z: High-impedance (A, B are isolated)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Pa	rameter	C	Conditions	Limits	Unit
Vcc	Supply voltage				-0.5~+7	V
Vı	Input voltage	A, B		,	-0.5~+5.5	V
٧I	OCAB, OCBA			-0.5~+15	V	
Vo	Output voltage		Off-state		-0.5~+5.5	V
Topr	Operating free-air ambier	nt temperature range			-20~+75	°C
Tstg	Storage temperature range	ge			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Unit		
			Min	Тур	Max	Onit
.V _{CC}	Supply voltage		4.75	5	5.25	V
-1	High-level output current VoH≥ 2.4V VoH≥ 2.V	V _{0H} ≥2.4V	0		-3	mA
Іон		0		-15	mA	
		V _{0L} ≤0.4V	0		12	mA
loL	Low-level output current VoL≤0.5V		. 0		24	mÀ

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted.)

Symbol	Parameter		-	est conditio		Limits			Unit		
Symbol	Paramete	er	'	est conditio	ns	Min	Typ *	Max	Unit		
V _{IH}	High-level input voltage					2			V		
VIL	Low-level input voltage							0.8	٧		
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V			0.2	0.4		V		
Vic	Input clamp voltage		V _{CC} =4.75V,	I _{IC} = - 18	mA			-1.5	V		
.,	High-level output voltage		V _{CC} =4.75V	V _I = 0.8V	', I _{OH} = - 3mA	2.4	3.1		v		
Voн	migri-lever output vortage		V _I =2V	V _I = 0.5V	, I _{OH} = — 15 mA	2		100	. V		
.,	Low-level output voltage		V _{CC} =4.75V		I _{OL} = 12mA		0.25	0.4	V		
VoL	Low-level output voltage		V _I =0.8V, V _I =2V		V ₁ =0.8V, V ₁ =2V		I _{OL} =24mA		0.35	0.5	V
lozh	Off-stage high-level output current		V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =2.7V				40	μА			
lozL	Off-state low-level output curre	ent	V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =0.4V				-200	μА			
	A, B		V 5 25V V 0 7V				20				
	High-level input current	OCAB, OCBA	V _{CC} =5.25V, V _I =2.7V				20	μΔ			
ЛН .	riigii-level liiput current	A, B	V _{CC} =5.25V,	V _I =5.5V				0.1	mA		
	OCAB, OCBA		V _{CC} =5.25V,	V _I = 10V				0.1	mA		
		OCAB, OCBA	V 5 25V					-0.2			
liu .	Low-level input current	Α	$V_{CC}=5.25V$ $V_{I}=0.4V$	OCA	B=0CBA=0V			-0.2	mΑ		
		В	VI=0.4V	OCA	B=OCBA=4.5V			-0.2			
los	Short-circuit output current (N	Note 2)	V _{CC} =5.25V, V _O =0V		-40		-225	mΑ			
Госн	Supply current, all output high	1	V _{CC} =5.25V,	$V_{l} = 0 V$,	V _I =4.5V		22	38	mA		
COL	Supply current, all outputs low	v	V _{CC} =5.25V,	$V_1 = 0 \ V$,	V _J =4.5V	•	29	50	mA		
locz	Supply current, all outputs off		V _{CC} =5.25V,	$V_1 = 0 V_1$	V ₁ =4.5V		32	54	mΑ		

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.



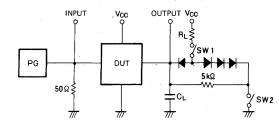
Note 2: All measurements should be done quickly and not more than one outputs should be shorted at a time.

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

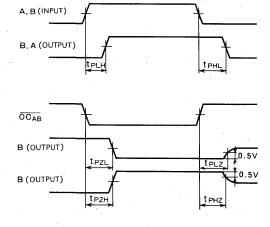
Symbol	Parameter	Test conditions	Limits			Unit
Syllibol	raianietei	rest conditions	Min	Тур	Max	Oiiit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time,	C _L =45pF		8	18	ns
t _{PHL}	from inputs A, B to outputs B, A	(Note 3)		9	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		15	40	ns
t _{PZL}	Output enable time to low-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		11	25	ns
t _{PHZ}	Output disable time from high-level	R _L =667Ω C _L = 5 pF (Note 3)		12	18	ns

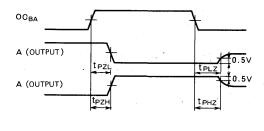
Note 3: Measurement circuit



Symbol	SW 1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
- (2) All diodes are switching diodes ($t_{rr} \le 4ns$).
- (3) CL includes probe and jig capacitance.





OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

DESCRIPTION

The M74LS244P is a semiconductor integrated circuit containing 2 blocks of buffers with 3-state non-inverted output and common output controlling input for all 4 discrete circuits.

FEATURES

- Low input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage (V₁ ≥ 15V)
- Output control input having same phase for 2 circuits
- High fan-out, 3-state output $(I_{OL} = 24mA, I_{OH} = -15mA)$
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

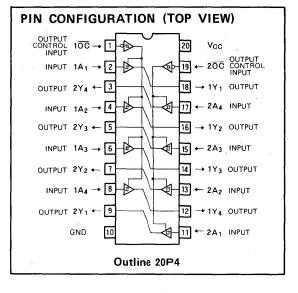
FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuit has enabled the achievement of small input load factor. With hysteresis characteristics, the buffer has a 3-state noninverted output with high noise margin.

When output control input OC is low, the output Y is low if input A is low and Y is high if A is high, When OC is high, all of Y₁, Y₂, Y₃, and Y₄ are in the highimpedance state, irrespective of the status of A.

By connecting 100 with 200, it becomes possible to control the output of all 8 circuits simultaneously. Output can be terminated by a load resistor of 133Ω or over.

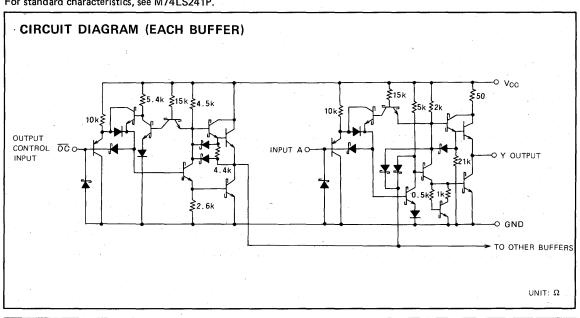
For standard characteristics, see M74LS241P.



FUNCTION TABLE (Note 1)

Α	ōc	Y
L	L	L
Н	L	Н
X	Н	Z

Note 1: Z: high-impedance X: irrelevant



OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

ABSOLUTE MAXIMUM RATINGS $(T_a = -20 \sim +75^{\circ}C, \text{ unless otherwise noted})$

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
Vı	Input voltage		−0.5~+15	V -
V ₀	Output voltage	Off-state	$-0.5 \sim +5.5$	V
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol				Unit			
Symbol	Paramete	Min	Тур	Max	Onit		
Vcc	Supply voltage		4.75	5	5.25	V	
	18-b	V _{OH} ≧2.4V			-3	mA	
Іон	High-level output current			- 15	mA		
			V _{OL} ,≤0.4V			12	mA
IOL	Low-level output current VoL≤0.5V				24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Compleal	D		Test conditions		Limits			Unit
Symbol	Parameter		Test conditions			Тур*	Max	Unit
V _{IH}	High-level input voltage				2			V
V _{IL}	Low-level input voltage					0.8	· V	
V _{T+} -V _{T-}	Hysteresis	V _{CC} =4.75V		0.2	0.4		V	
V _{IC}	Input clamp voltage	V _{CC} =4.75V	, I _{IC} =-18	mA			-1.5	V
	High level event veltere	V _{CC} =4.75V	V _I = 0.8V	/, I _{OH} =-3mA	2.4	3.4	-	V
V _{OH}	High-level output voltage	V ₁ =2V	V _I = 0.5V	$I_{OH} = -15 \text{mA}$	2			٧
.,	Law lavel output veltage	V _{CC} =4.75V	•	I _{OL} =12mA		0.25	0.4	V
· VOL	V _{OL} Low-level output voltage	V _I =0.8V, V	=2V	I _{OL} =24mA		0.35	0.5	V
lozн	Off-state high-level output current	V _{CC} =5.25V	, V _I =2V, V	7 ₀ =2.7V			20	μA
lozL	Off-state low-level output current	V _{CC} =5.25V	, V _I =2V , V	/ _O =0.4V			-20	μA
1	High-level input current	V _{CC} =5.25V	V _{CC} =5.25V, V _I =2.7V				20	μΑ
hH.	night-level input current	V _{CC} =5.25V	, V _I =10V				0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V	, V _I =0.4V				-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V	, V ₀ =0V		- 40	4 1	-225	mA
Гссн	Supply current, all outputs high	$V_{CC} = 5.25V, V_{I} = 0V, V_{I} = 4.5V$			17	27	mA	
ICCL	Supply current, all outputs low	V _{CC} =5.25V,	V _I = 0 V			27	46	mA
looz	Supply current, all outputs off	V _{CC} =5.25V	, V _I =4.5V			32	54	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

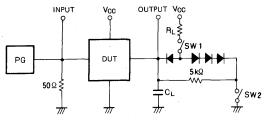
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Syllibol	rarameter	l est conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		8	18	ns
t _{PHL}	time, from input A to output Y	(Note 3)		9	18	ns
t _{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	30	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		12	40	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		11	25	ns
tpHZ	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		12	18	ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

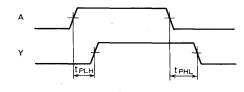
OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

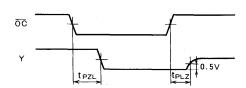
Note 3: Measurement circuit

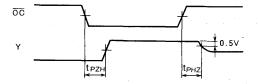


Symbol	SW 1	3W2
t pzh	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_f = 6ns$, $t_f = 6ns$, $t_W = 500ns$,
 - $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$
- (2) All diodes are switching diodes (t_{fr} ≤ 4ns)
 (3) C_L includes probe and jig capacitance.







OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

DESCRIPTION

The M74LS245P is a semiconductor integrated circuit containing of 8 bus transmitter/receiver circuits with non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Low input load factor (pnp input)
- Input/output A and output/input B have hysteresis characteristics (Hysteresis = 400mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

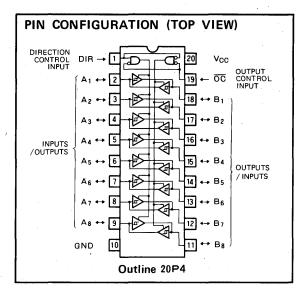
APPLICATION

General digital equipment for industrial and consumer use

FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected alternately to form a bi-directional buffer.

With hysterisis characteristics in the input section of input/output A and output/input B, noise margin is high. The use of a pnp transistor input has made the input load factor small. The data direction control input DIR controls the direction of input and output. When DIR is high, A is the input terminal and B is the output terminal. On the contrary, when DIR is low, B is the input terminal and A is the output terminal.



When the output control input \overline{OC} is high, both A and B, in a high-impedance state, are separated.

FUNCTION TABLE (Note 1)

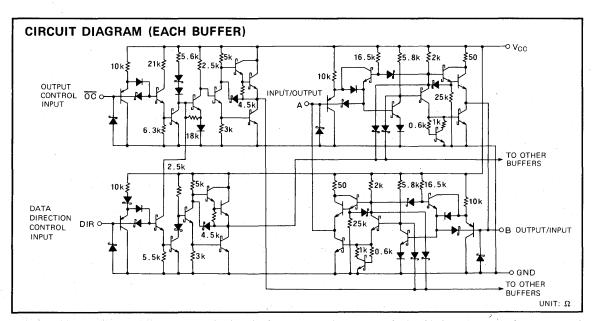
ŌĈ	DIR	Α .	В
L	L	0	ı
L	Н	1	0
. н	х	z	Z

Note 1: | : input

O: output (noninverted output)

Z: high-impedance

X: irrelevant



OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

Symbol	Par	ameter	Condi	tions	Limits	Unit
Vcc	Supply voltage				-0.5~+7	V
	land altere	A, B	,		-0.5~+5.5	V
Vi	V _I Input voltage	DIR, OC			-0.5~+15	V
Vo	Output voltage	, ,	Off-state		-0.5~+5.5	V
Topr	Operating free-air ambier	nt temperature range			-20~+75	°C
Tstg	Storage temperature range	ge			- 65~ + 150	€

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

		Parameter		Limits					
Symbol	rarami	eter	Min	Тур	Max	Unit			
Vcc	Supply voltage		4.75	5	5.25	V			
	High level and a second as	V _{OH} ≥ 2.4V	0		-3	mA			
Тон	High-level output current	V _{OH} ≧ 2V	0		— 15	mΑ			
. 1	Laurent - de de march	V _{OL} ≤ 0.4 V	0		12	mΑ			
IOL	Low-level output current	V _{OL} ≤ 0.5V	0		24	mA			

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

0	D		Test cond	dia in ma		Limits		Unit
Symbol	Para	emeter	rest cond	IILIOIIS	Min	Тур	Max	Offic
VIH	High-level input voltage				2	- 1		V
VIL	Low-level input voltage						0.8	V
$V_{T+}-V_{T-}$	Hystersis		V _{CC} =4.75V		0.2	0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	V
	High lavel autout valtage		V _{CC} =4.75V	I _{OH} = -3mA	2.4	3.4		V
Voн	High-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OH} = - 15mA	2			V
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 12mA			0.4	V
VoL	Low-level output voltage		$V_1 = 0.8V, \ V_1 = 2V$	I _{OL} =24mA			0.5	V
lozh	Off-state high-level outpu	t current.	V _{CC} =5.25V, V _I =0.8V	$V_1 = 2V, V_0 = 2.7V$			20	μΑ
lozL	Off-state low-level output	current	V _{CC} = 5.25V, V _I = 0.8V	$V_1 = 2V, V_0 = 0.4V$			-200	μΑ
		A, B	V 5 05V V 0	*\ /			20	μΑ
	High-level input current	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.7$				20	μА
lin .	migri-lever imput current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
	•	DIR, OC	V _{CC} =5.25V, V ₁ = 10	V			0.1	mA
lı∟	Low-level input current		V _{CC} =5.25V, V _I =0.4	IV			-0.2	mΑ
los	Short-circuit output curre	ent (Note 2)	V _{CC} =5.25V, V _O = 0	V	40		- 225	mA .
LCCH	Supply current, all outpu	ts high	$V_{CC} = 5.25V, V_I = 0$	V, V _I = 4.5V		48	70	mΑ
ICCL	Supply current, all output	ts low	$V_{CC} = 5.25V, V_I = 0$	V, V _I = 4.5V		62	90	mΑ
lccz	Supply current, all outpu	ts off	V _{CC} =5.25V, V _I = 0	V, V _I = 4.5V		64	95	mA

^{* :} All typical values are at V_{CC} = 5V, $Ta \approx 25$ °C.

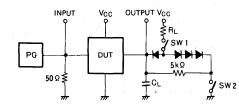
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, Ta=25% unless otherwise noted)

6		T P		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Offic
tpLH	Low-to-high-level, high-to-low-level output propagation	0 45-5 (1) 2)		10	15	ns
tpHL	time, from input A, B to output B, A	C _L = 45 pF (Note 3)		10	15	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		25	40	ns
t _{PZH}	Output enable time to high-level	$R_L = 667 \Omega$, $C_L = 45 pF$ (Note 3)		23	40	ns
t _{PLZ}	Output disable time from low-level	R _L =667Ω, C _L =5pF (Note 3)		15	25	ns
tenz	Output disable time from high-level	$R_L = 667 \Omega$, $C_L = 5 pF$ (Note 3)		14	25	ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

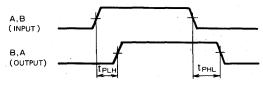
Note 3: Measurement circuit

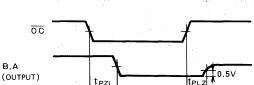


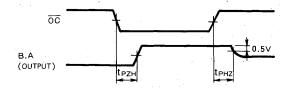
Symbol	SW1	SW2
tрzн	Open	Closed
tezu	Closed	Open
tpLz	Closed	Closed
touz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω
- (2) All diodes are switching diodes (t_{rr} ≤ 4ns)
- (3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

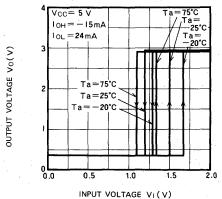




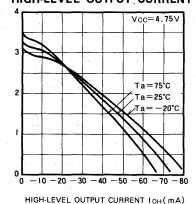


TYPICAL CHARACTERISTICS

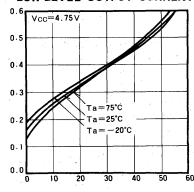
OUTPUT VOLTAGE VS INPUT VOLTAGE



HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VOL(V)

HIGH-LEVEL OUTPUT VOLTAGE VOH(V)

BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

DESCRIPTION

The M74LS247P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function and open collector outputs.

FEATURES

- Suitable for 7-segment display element lighting
- RBI input and BI/RBO outputs for zero suppression
- LT input for lamp testing
- BI/RBO input for extinguishing all segments
- Open collector outputs
- Wide operating temperature range (T_a=-20~+75°C)

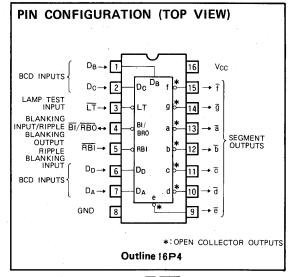
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a number is specified in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment ouputs $\overline{a} \sim \overline{g}$ are set low in accordance with that number. By connecting the 7-segment display element to each of the outputs, the character indicated on the display character can be displayed. $\overline{a} \sim \overline{g}$ are open collector outputs with a breakdown voltage of not less than 15V and a low-level output current of 24mA, therby making it possible to drive directly a 7-segment LED for the display of anode-common numbers.

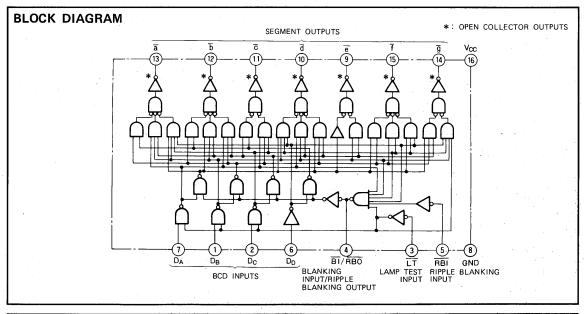
Suppression of the unnecessary high-order zeroes is possible by setting the highest order \overline{RBI} ripple blanking input low and connecting ripple blanking output $\overline{BI}/\overline{RBO}$ to the next-level \overline{RBI} for each of the digits. Refer to the M74LS47P for the application example.



By setting blanking input $\overline{BI/RBO}$ low, outputs $\overline{a} \sim \overline{g}$ are set high and the display element is extinguished irrespective of the status of the other inputs. Since $\overline{BI/RBO}$ serves as both an input and output pin, only ICs with open collector outputs can be connected to this pin.

By setting lamp test input \overline{LT} low, $\overline{a} \sim \overline{g}$ are set low irrespective of the status of $\overline{BI/RBO}$, D_A , D_B , D_C and D_D , all the segments in the display element are lighted and each segment can be tested. Refer to M74LS47P for the $\overline{BI/RBO}$ and $a \sim g$ circuits.

The only difference between the M74LS247P and M74LS47P is the configuration of the 6 and 9 numerals.



BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	LT	RBI	D _D	Dc	DB	DA	BI/i	RBO	ā	Б	č	: d	ē	Ť	g	Note
. 0	Н	н	L	L	L	L		Н	L	L	L	-L	· Ł	L	Н	
1	Ι	X	L	L	L	н		Н	Н	L.	L	Н	Н	Н	н]
2	Н	Х	L	L	н	L		н	L	L	н	L.	L	Н	L]
3	Н	Х	L	L	Н	н		. Н	L	L	L	L	Н	Н	L	
4	н	Х	L	Н	L	L		Н	H	L	TL.	Н	٠н	L	L	
5	Н	X.	L	Н	L	Н		Н	·L	Н	L	L	Н	L	. L	
6	Н	х	٦	Н	Н	L		Н	L	Н	L	L	L	L	, L	
7	Н	х	L	н	Н	н		Н	L	L	L	н	Н	Н	Н	(i)
8	Н	Х	Н	L	L	L		Н	L	L	L	L	L	L	L	(1)
9	Н	X	Η	L	L	н		Н	L	L	L	L	н	Ľ	L	1
10	Н	X	н	L	Н	L		H.	Н	н	н	L	L.	Н	L	
11	Н	Х	Н.	L	Н	Н		Н	Н	Н	L	· L	н	H	L.].
12	Н	х	Η	Н	L	L		: Н	Н	L	Н	Н	Н	L	L	
13	н	Х	Н	Н	L	н		Н	L	н	н	L	н	L	L	
14	Н	X	H	H	Н	L		Н	н	н	Н	L	L	L	L	
15	Н	· X	I	Н	Н	Н		Н	Н	Н	Н	Н	. н	Н	Н	
Blanking	X	×	×	. X	×	Χ.	L		Н	н	Н	Н	Н	Н	н	(2)
Ripple blanking	Н	L	L	L	L	L		L	Н	Н	н	H.	Н	Н	Н	(3)
Lamp test	L	Х	Х	X	Х	×		Н	L	L	L	L	L	· L	L	(4)

Note 1. (1) LT is normally kept in high.

DEFINITION OF SEGMENTS

- RBI is kept open or in high with a decimal 0 output.
- (2) When $\overline{BI}/\overline{BBO}$ is low, all the segment outputs are high irrespective of the status of the other inputs.

 (3) All the segment outputs are set high and $\overline{BI}/\overline{BBO}$ is set low when \overline{BBI} , D_A , D_B , D_C and D_D are set low with \overline{LT} high.
- (4) When LT is low, all the segment outputs are low.
- X: Irrelevant



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character			n	3	4	5	5	<u> </u>	8	9	n	Ü	U	ıП	۲	

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Para	meter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~.+7	. V
	Input voltage	Input BI/RBO		-0.5~V _{CC}	V
Vı	imput voitage	Other inputs		-0.5~+15	V
Vo	Output voltage	Output BI/RBO	High-level state	-0.5~V _{CC}	V
Vo.	Output voltage	Other outputs	I ngirievei state	-0.5~+15	· v
I _{O(peak)}	Output current		tw≤1ms, dutycycle≤10%	200	mA ·
10	Output current		High-level state	. 1	mA
Topr	Operating free-air ambier	t temperature range	¥1	-20~+75	°C
Tstg	Storage temperature rang	e		· −65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 - +75°C, unless otherwise noted)

C	Parameter	1		Limits		Unit
Symbol	rarameter		Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current, outputs a ~ g	V _{OH} =15 V	0		250	μА
Іон	High-level output current, output BI/RBO	V _{OH} ≥2.4V	0		-50	μΑ
	Low-level output current,	V _{OL} ≤0.4V	0		12	mA
loL	outputs a ~ g	V _{OL} ≦0.5V	0		24	mA
1	Low-level output current,	V _{OL} ≤0.4V	0		1.6	mA
loL	output BI/RBO	V _{OL} ≦0.5V	0		3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +70^{\circ}C$, unless otherwise noted)

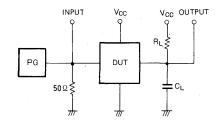
0	Paramete		Test condi	tions		Limits		11-14
Symbol	raramete	ır	Test condi	tions	Min	Typ *	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage ·		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	٧
VoH	High-level output voltage, out	out BI/RBO	V _{CC} =4.75V	I _{0H} ≈ −50μA	2.4	4.2		V
loH	High-level output current, out	outs ā — g	V _I =0.8V, V _I =2V	V ₀ =15V			250	μΑ
		Outputs a ~ g		I _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	Outputsa ~ g	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	٧
VOL	Low-level output voltage	Output BI/RBO	V _I =0.8V, V _I =2V	I _{OL} =1.6mA		0.25	0.4	٧
		Output Bij NBO		I _{OL} =3.2mA		0.35	0.5	V
1	High-level input voltage, excep	t input BI/BBO	V _{CC} =5.25V, V ₁ =2.7	7 V			20	μΑ
Ιн	riigii-level nipat voltage, excep	Cilipot Biv 1180	V _{CC} =5.25V, V _I =10V	/			0.1	mA
1	Low-level input current	Input BI/RBO	V = 5 25V V = 0	11/			-1.2	mA
հլ	Low-level hiput current	Other inputs	$V_{CC} = 5.25V, V_{I} = 0.4$	+ v			-0.4	mΑ
los	Short-circuit output current, o	utput BI/RBO	V _{CC} =5.25V, V _O =0\	1	-0.3		-2	mA
lcc	Supply current		V _{CC} = 5.25V (Note 2)			7	13	mA

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C. Note 2. I_{CC} is measured with all inputs at 4.5V.

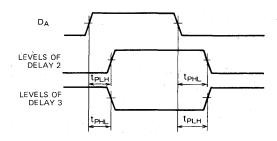
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

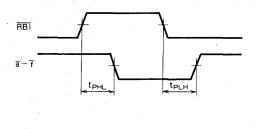
Symbol	Parameter	Test conditions		Limits		Unit
Зупрог	rai ai i e tei	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	D oor o		35	100	ns
t _{PHL}	time, from input $D_{\pmb{A}}$ to outputs $\overline{\pmb{a}} \sim \overline{\pmb{g}}$	$R_{L} = 665 \Omega$ $C_{1} = 15 pF$		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	(Note 3)		50	100	ns
t _{PHL}	time, from input \overline{RBI} to outputs $\overline{a} \sim \overline{f}$		***	45	100	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance





BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

DESCRIPTION

The M74LS248P is a semiconductor integrated circuit provided with a BCD-to-7-segment decoder/driver function and 2kohm (typ) pull-up resistor outputs.

FEATURES

- Suitable for lighting 7-segment display element
- RBI input and BI/RBO output for zero suppression
- LT input for lamp testing
- BI/RBO input for blanking all segments
- NPN transistor can be externally mounted for highcurrent drive.
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

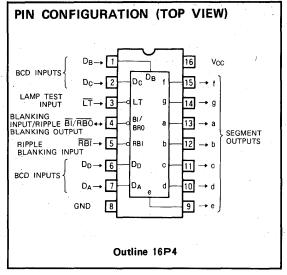
FUNCTIONAL DESCRIPTION

This IC is a version of the M74LS247P without the output transistors. When numbers are specified in BCD code for BCD inputs D_A , D_B , D_C and D_D , segment outputs a~g are set high in accordance with those numbers. These outputs have built-in $2k\Omega$ pull-up resistors suited to driving common-cathode LEDs. High-current display elements can be driven by connecting NPN transistors to the outputs.

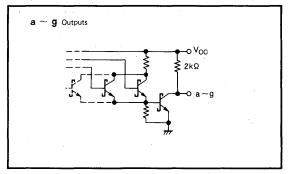
The ripple blanking, blanking and lamp test functions are the same as those for the M74LS247P.

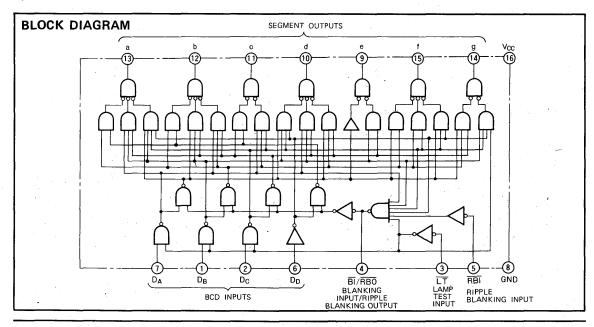
Refer to the M74LS47P for the application example.

The only difference from the M74LS48P is the configuration of the 6 and 9 numerals.



OUTPUT CIRCUIT SCHEMATIC





BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	ĹΤ	RBI	D _D	Dc	DB	DA	BI/F	RBO	а	b	С	d	е	f	g	Note
0	н	Н	L	, L	L	L		Н	Н	Н	Н	н	Н	н	L	
1	н	Х	∟	L	L	н		Н	L	Н	Н	L	Ľ	L	L	
2	Н	Х	L	L	Н	Ļ		Н	Н	Н	L	Н	н	L	н	
3	Н	· X	L	L	Н	Н		Н	Н	Н	Н	Н	L.	L	Ή.	
4.	н	Х	L	I	L	L		Н	L	н	Н	L	L	Н	.Н]
. 5	Н	Х	L	Н	L	Н		Н	Н	L	Н	Н	L.	н	н	
6	Н	Х	L	Н	Н	L		Н	Н	L	Н	Н	Н	Н	н	
7	Н	X	L	Н	Н	Н		Н	Н	Н	Н	L	L	L	L	(1)
8	Н	Х	Н	Ŀ	L	L		н	Н	^ H	Н	Н	Н	Н	н	1 (1)
9	н	Х	Н	L	L,	Н		Н	Н	Н	Н	Н	L	Н	Н	1
10	н	Х	Н	L	Н	L		Н	L	L	L	Н	Н	L	н	
11	н	Х	Н	L	Н	Н		Н	L	L	Н	Н	L	L	Н	Ī
12	Н	Х	Н	Н	L	L		Н	L	Н	L	L	L	Н	Н	1
13	Н	Х	Ĥ	Н	L.	Н		Н	Н	L	L	н	L	Н	Н	
14	н	Х	Н	Н	Н	L		Н	L	L	L	Н	н	Н	н	
15	Н	Х	Н	Н	Н	Н		Н	L	L	L	L	L	L	L	1
Blanking	Х	Х	Х	Х	Х	×	L		L	L	L	L	L	L	L	(2)
Ripple blanking	Н	L	L	L	L	L		L	L	L	L	L	L	L	L	(3)
Lamp test	L	Х	Х	X	Х	Χ.		H	н	Н	н	Н	Н	Н	н	(4)

Note 1. (1) LT is normally kept in high.

DEFINITION OF SEGMENTS

- RBI is kept open or in high in case of a decimal 0 output.
- (2) When $\overline{\text{BI/RBO}}$ is low, all the segment outputs are low irrespective of the status of the other inputs.
- (3) All the segment outputs are set low and $\overline{B1/RBO}$ is set low when $\overline{RB1}$, D_A , D_B , D_C and D_D are set low with \overline{LT} high.
- (4) When LT is low, all the segment outputs are high.
- X: Irrelevant

CHARACTERS DISPLAYED



ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Par	ameter	Conditions	Limits	Unit
Voc	Supply voltage			-0.5~+7	V
.,	1:	Input BI/RBO		-0.5 ~ V _{CC}	V
VI	Input voltage	Other inputs	1	-0.5~+15	V
	Output valtage	Output BI /RBO	Link to all the	-0.5 - V _{CC}	V
V ₀	Output voltage	Other outputs	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambier	t temperature range		−20 ~ +75	°C
Tstg	Storage temperature rang	e	`	-65~+150	°C ·

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

	•			Limits	-	
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5 .25	V
Іон	High-level output current, outputs a∼g	V _{OH} ≧2.4V	0		- 100	μА
Юн	High-level output current, output BI/RBO	V _{OH} ≧2.4V	0		50	μА
		V _{OL} ≤0.4V	0		2	mA
lor"	Low-level output current, outputs a~g	V _{OL} ≦0.5V	0		6	mA
	Low love out out of 1700	V _{OL} ≤0.4V	0		1.6	mA
IOL	Low-level output current, output BI/RBO	V _{OL} ≤0.5V	0		3.2	mΑ

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +70$ °C, unless otherwise noted)

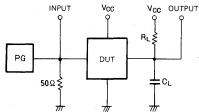
	D					Limits	ŀ	Unit
Symbol	Paramete	er .	Test cond	itions	Min	Тур 🛊	Max	Unit
VIH	High-level input voltage				2			V
ViL	Low-level input voltage						0.8	. V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA		,	-1.5	V
	High-level output voltage	Outputs a∼g	V _{CC} = 4.75V	$I_{OH} = -100 \mu A$	2.4	4.2	•	٧
Vo ^H	riigh-level output voltage	Output BI RBO	$V_1 = 0.8V, V_1 = 2V$	$I_{OH} = -50 \mu A$	2.4	4.2		V
Гон	High-level output current	Outputs a~g	V _{CC} =4.75V, V _I =0.8V	$V_1 = 2V_1 V_0 = 0.85V$	-1.3	-2		mA
		0.4		I _{OL} =2mA		0.25	0.4	V.
	Low-level output voltage	Outputs a∼g	V _{CC} =4.75V	I _{OL} =6mA		0.35	0.5	V
V _{OL}	Low-level output voltage	Output BI/RBO	$V_1 = 0.8\dot{V}, V_1 = 2V$	I _{OL} =1.6mA		0.25	0.4	V
		Output BI/NBO		I _{OL} =3.2mA		0.35	0.5	V
1	Liber Level Communication	Except input BI/RBO	V _{CC} =5.25V, V _I =2.	7 V			20	μА
Ιн	High-level input current	Except linbut BI\KBO	V _{CC} =5.25V, V _I =10V	/			0.1	mA
1	Low-level input current	Input BI/RBO	V _{CC} =5.25V, V _I =0.4	11/			-1.2	mA
l _{IL}	Low-level imput current	Other inputs	vcc-5.25v, V =U.	• • • • • • • • • • • • • • • • • • •			-0.4	mA
los	Short-circuit output current	Output BI/RBO	V _{CC} =5.25V, V _O =0\	/	-0.3		-2	mA
Icc .	Supply current		V _{CC} = 5.25V (Note 2)			25	38	mA

 $[\]bigstar$: All typical values are at $V_{CC} = 5 V$, $T_a = 25 ^{\circ} C$.

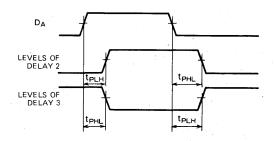
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

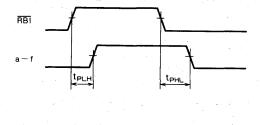
Symbol	Parameter	Test conditions		Limits		Ulate
Symbol .	rarameter	lest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation	R _L =4kΩ		30	100	ns
t _{PHL}	time, from input D_A to outputs a \sim g	C _L =15pF (Note 3)		30	100	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	R _L =6kΩ		40	100	ns
tpHL	time, from input RBI to outputs a∼f	C _L =15pF (Note 3)		45	100	ns

Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: $PRR=1MHz,\,t_r=6ns,\,t_f=6ns,\,t_w=500ns,\,V_P=3V_P.p,\,Z_O=50\Omega.$
- (2) C_L includes probe and jig capacitance







Note 2. I_{CC} is measured with all inputs at 4.5V.

MT4LS251P

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS251P is a semiconductor integrated circuit containing an 8-line to 1-line data selector/multiplexer function and 3-state outputs.

FEATURES

- 3-state outputs
- Complementary output provided
- Wide operating temperature range (T_a=-20~+75°C)

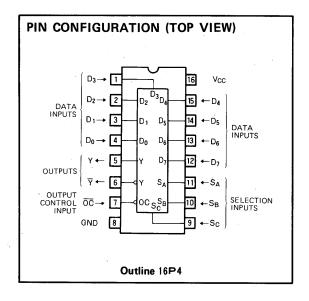
APPLICATION

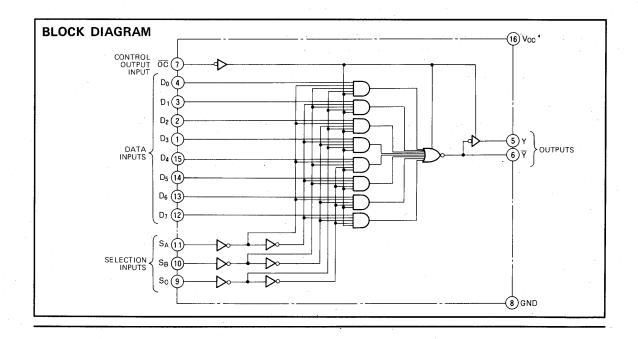
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has a data selector function which provides 1-line selection of 8 input signals and using a multiplexer function which converts the 8-bit parallel data into serial data by time-sharing. When 8-line signals are applied to the data inputs and 1 data is specified from among the 8 data from selection inputs S_A , S_B and S_C , the input signal is at output Y and the inverted signal from output \overline{Y} . When output control input \overline{OC} is set high, Y and \overline{Y} are put in the high-impedance state and the outputs are completely isolated.

M74LS251P has the same functions and pin connections as M74LS151P but the latter is provided with active pull-up resistor outputs.





8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

FUNCTION, TABLE (Note 1)

Sc	SB	SA	ōc ,	D ₀	D ₁	D ₂	D3	D4	D ₅	D ₆	D ₇	Υ Υ	7
Х	×	×	Н	×	×	Χ.	×	×	×	×	×	Z	Z
L	L	L	L	L	Х	. ×	×	Χ .	×	×	×	L	н
L	L	L	L.	н	×	Х	×	х	×	×	×	Н	L
L	L	Ή	L	×	L	·×	X	×	×	×	×	L	Η.
. L	L	н	L	×	H	×	×	X.	×	x	×	н	_
L	Н	· L	L	- X	×	L	X	×	×	X	×		Η
L	н	L	٦	×	×	Н	×	×	×	×	×	Н	۱.
L	Н	н	ال	×	×	×	L	, x	, x	Χ .	×	L	Н
L	н	н	L	×	×	×	н	×	×	×	×	н	١
н	L	· Ł	∟	×	. X	×	×	L	×	×	· X	L	Ι
н	L	L	L	×	×	×	×	Н	×	×	×	I	ا ـ
н	L	Н	١	×	×	x	Χ.	х	L	×	×	Ĺ	Ι
Н	L	н	, L	×	×	×	×	×	н	4, X	×	įН ,	L
: н	н	L	L	×	×	×	×	· x	X	L	×	L	I
Н	н	L	Ĺ	X	ΧŤ	×	- X	×	· X	н	×	Ŧ,	
н	н	н	. L	×	×	×	×	×	×	×	L	١	Ι
н	н	н	L	×	×	×	X	×	X.	×	H	Н	· .

Note 1 X: Irrelevant

Z: High-impedance state

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		-20~+75	℃
Tstg	Storage temperature range		-65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Limits		Unit
Symbol	Paramete	3r	Min	Тур	Max	Ullit
Vcc	Supply voltage		. 4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.4V	0		-2.6	mA
		V _O L≦0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

M74LS251P

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 \, ^{\circ}C$, unless otherwise noted)

C	Parameter	Test conditions		Limits		Unit
Symbol	rarameter	lest conditions	Min	Typ *	Max	Unit
ViH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
V _{OH}	High-level output voltage	$V_{CC} = 4.75V \cdot V_{I} = 0.8V$ $V_{I} = 2V \cdot I_{OH} = -2.6mA$	2.4	3.1		٧
VoL	Low-level output voltage	V _{CC} =4.75V		0.25	0.4	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V ₀ =2.7V			20	μА
lozL	Off-state low-level output current	V _{OC} =5.25V, V _I =2V, V ₀ =0.4V			-20	μА
1	High level in a town	V _{CC} =5.25V, V _I =2.7V			20	μА
hн.	High-level input current	V _{CC} =5.25V, V _I =10V			0.1	mA
TIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.4	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	-30		- 130	mA
loc	Supply current	V _{OC} =5.25V (Note 3)		6.1	10	mA
locz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)		7.1	12	mA

^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation			22	45	ns
t _{PHL}	time, from inputs SA, SB, SC to output Y			18	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	33	ns
t _{PHL}	time, from inputs S_A , S_B , S_C to output \overline{Y}	C _L = 15 pF (Note 5)		15	33	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL=15pr (Note 5)		15	28	ns
t _{PHL}	time, from inputs D 0~D 7 to output Y			14	28	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	15	ns
t _{PHL}	time, from inputs $D_0 \sim D_7$ to output \overline{Y}			7	15	ns
t _{PZH}	High-level output enable time, from input OC to output Y	2 20 2 45 5 11		11	45	ns
t _{PZL}	Low-level output enable time, from input OC to output Y	R _L =2kΩ, C _L =15 pF (Note 5)		16	40	ns
t _{PZH}	High-level output enable time, from input \overline{OC} to output \overline{Y}	B 210 0 -15-5 (11115)		11	27	ns
tpZL	Low-level output enable time, from input \overline{OC} to output \overline{Y}	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		13	40	ns
t _{PHZ}	High-level outpout disable time, from input OC to output Y		,	16	45	ns
t _{PLZ}	Low-level output disable time, from input OC to output Y	$R_L=2k\Omega$, $C_L=5$ pF (Note 5)		8	25	ns
t _{PHZ}	High-level output disable time, from input \overline{OC} to output \overline{Y}	D 010 0 - 5 - 5 (blace 5)		18	55	ns
t _{PLZ}	Low-level output disable time, from input \overline{OC} to output \overline{Y}	$R_L=2k\Omega$, $C_L=5$ pF (Note 5)	,	9	25	ns

Note 2: All measurements should be done quickly.

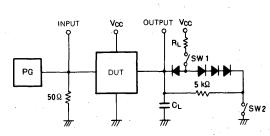
Note 3: I_{CC} is measured with \overline{OC} at 0V and all other inputs at 4.5V

Note 4: I_{CCZ} is measured with all inputs at 4.5V.

M74LS251P

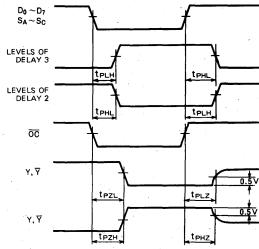
8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT





- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, $V_P=3V_{P.P}$, $Z_o=50\Omega$.
- (2) All diodes are switching diodes. (t_{rr} ≤ 4ns)
 (3) C_L includes probe and jig capacitance

Symbol	SW 1	SW2
t pzh	Open	Closed
tpzL	Closed	Open
tpLZ	Closed	Closed
t phz	Closed	Closed



MITSUBISHI LSTTLS M74LS253P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS253P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Selection inputs common to both circuits
- Output control inputs separate for each circuit
- 3-state outputs
- Wide operating temperature range (T_a=-20~+75°C)

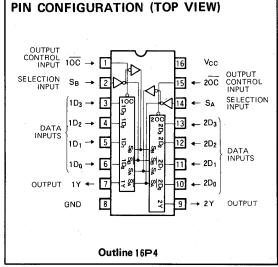
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signal using two multiplexer circuits which convert the 4-bit parallel data into serial data by time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 , and 1 data is specifed from among the data input by selection inputs S_A and S_B , the input signal is output at Y. By applying 4-bit parallel data to data inputs D_0 , D_1 , D_2 and D_3 and by connecting the output of a synchronous divide-by-four counter to S_A and S_B , data D_0 , D_1 , D_2 and D_3 appear in the order of D_0 , D_1 , D_2 and D_3 , synchronized with the clock pulse, S_A and S_B are common to both circuits while output control inputs $1\overline{OC}$ and $2\overline{OC}$ are separate. When $1\overline{OC}$ and $2\overline{OC}$ are set high, 1Y and 2Y are put in the high-impedance state ("Z") irrespective of the status of the inputs.

M74LS253P has the same functions and pin connections as M74LS153P but the latter is provided with active pull-up resistor outputs.

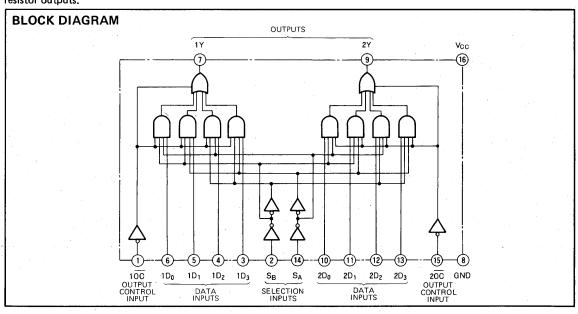


FUNCTION TABLE (Note 1)

S _B	SA	D ₀	1ם	D ₂	D ₃	ōc	Υ
×	х	Х	×	X	×	н	Z
L	L	L	×	×	X	L	L
١	L	Ξ	×	X	Х	L	н
Ĺ	н	X	L	X	×	L	L
<u>ا</u>	Ι	X	Н	X	X	L	н
Н	L	X	×	L	X	L	L
Н	L	×	X	Н	X	L	Н
Ι	н	Χ	×	×	L	L	L
Η	Н	Χ	Х	×	Ŧ	L	Н

Note 1 X : Irrelevant

Z: High-impedance state



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V ₁	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		−20~+75	, °C
Tstg	Storage temperature range		−65∼+150	°

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Sumb at	Parameter			Unit		
Symbol	rarameter		Min	Тур	Max	Omit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.4V	0,		-2.6	mA
		V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS (Ta = -20~+75℃, unless otherwise noted)

Combal	B	Took condit	Test conditions		Limits		
Symbol	Parameter	rest conditi	ions	Min	Typ ∗	Max	Unit
VIH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
Vall	High-level output voltage	V _{CC} =4.75V, V _I =0.8V	/ _	2.4	3.1		.,,
Vон	High-level output voltage	V _I = 2 V, I _{OH} = -2.6r	nA .	2.4	3.1		V
	Law level output voltage	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
V _{OL}	VoL Low-level output voltage	$V_{I}=0.8V, V_{I}=2V$	I _{OL} = 8 mA	1.	0.35	0.5	٧
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I = 2 V	, V ₀ =2.7V			20	μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I = 2 V	, V _O =0.4V			-20	μΑ
	High level in the summer	V _{CC} =5.25V, V _I =2.7V	/			20	μА
Ιн	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA
I _I L ·	Low-level input current	V _{CC} =5.25V, V _I =0.4V	/			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V		-30		— 130°	mA
Iccl	Supply current, all outputs low	V _{CC} =5.25V (Note 3)			7	12	mA
lccz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)		1.	8.5	-14	mA .

SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, Ta = 25 C, unless otherwise noted)

	Parameter	Test conditions		11-11		
Symbol	Parameter	l est conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation		٠.	8	25	ns
t _{PHL}	time, from inputs D ₀ ~D ₃ to output Y	0 45.5 (1)5)		12	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 5)		12	45	ns
t _{PHL}	time, from inputs SA, SB to output Y			12	32	ns
t _{PZH}	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		11	28	ns
t _{PZL}	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		12	23	ns
t _{PHZ}	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		15	41	ns
t _{PLZ}	Output disable time from low-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		9	27	ns

f * : All typical values are at V_{CC}=5V, T_a=25°C. Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

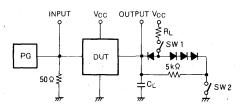
Note 3: I_{CCL} is measured with all inputs at 0V.

Note 4: I_{CCZ} is measured with $1\overline{OC}$ and $2\overline{OC}$ at 4.5V and all other inputs at 0V.

M74LS253P

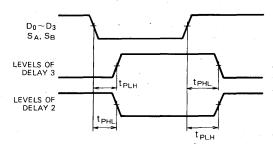
DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

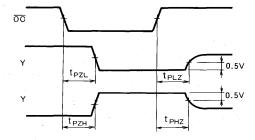
Note 5: Measurement circuit



Symbol	SW1	SW2
tрzн	Open	Closed
t PZL	Closed	Open
tplz	Closed	Closed
tpHZ	Closed	Closed

- The pulse generator (PG) has the following characteristics: PRR-1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P = $3V_{P-P}$, Z_O = 50Ω . All diodes are switching diodes. ($t_{rr} \le 4$ ns)
- C_L includes probe and jig capacitance.





MITSUBISHI LSTTLS M74LS256P

DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS256P is a semiconductor integrated circuit containing a dual demultiplexer circuit configured into a 4-bit latch addressable in 2-bit binary code.

FEATURES

- Easily expandable
- May be used as a 2-bit binary-to-quaternary decoder/ demultiplexer
- Active low common reset
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

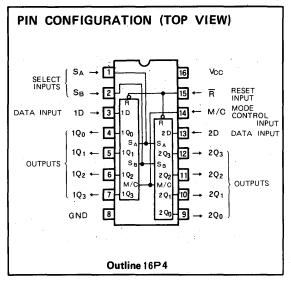
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device is configured from two circuits providing the capability to function as a 2- bit binary-to-quaternary demultiplexer or as a 4-bit latch. The operational modes listed below are selectable using mode control input M/C (common to both circuits) and reset input \overline{R} in combination.

- (1) 2-bit binary-to-quaternary decoder/demultiplexer
- (2) Addressable latch
- (3) Data input inhibit
- (4) Reset

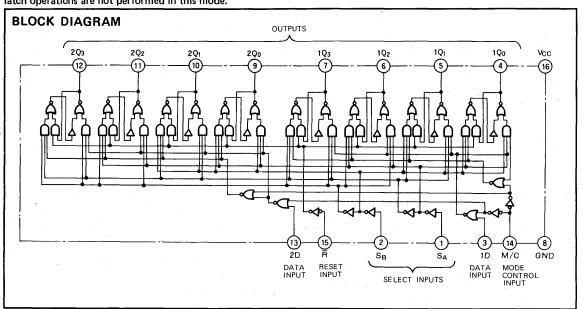
When used as a 2-bit binary-to-quaternary decoder/demultiplexer and a 2-bit binary number is applied to select inputs S_A and S_B , one of the $Q_0 \sim Q_3$ outputs will correspond to that number, and the signal appearing at its output will be the same as the one present at data input D. All other outputs will remain low-level at this time; and latch operations are not performed in this mode.



When used as an addressable latch, S_A and S_B will be recified as in the above operation, with the corresponding tch being selected. The signal present at data input D will then appear at output. When M/C transits from low to high (data inhibit mode), the information present at D immediately prior to that event will be latched. When M/C is low-level, changing the signal at D will also change the signal present at Q.

During the data input inhibit mode, changes applied to D will not affect $Q_0 \sim Q_3$, and the status prior to M/C transiting high will be held.

Direct reset is activated by all outputs at low-level, regardless of the status of D, S_A , and S_B .



FUNCTION TABLE (Note 1)

Operational mode	Ŕ	M/C	D	SA	SB	Q ₀	Q1	Q2	Q ₃
Reset	L	. Н	X	X	×	L	L	L	L
	L	L	Ļ	L	L	L	L.	Ĺ	L
	L	L	Н,	L	L.	Н	L	L	L
	L	L	١	Н	L ·	L	L	L	L
Active high 4-channel	L	با	Ŧ	н	L	L	н	L	L
demultiplexers	L	L	L	L	Н	L	L	١	L
	Ŀ	L	Ι	L	Н	L	L	т	الله
	L	٦	۲	н	Н	L	L	L	L
	L	L	Ι	Н	Н	L	L	L	Н.
Memory	н	н	Х	х	×	Q ₀ 0	Q 1 ⁰	Q2 ⁰	Q3 ⁰
	н	L	٦	L	L	L	Q1 ⁰	Q2 ⁰	Q3 ⁰
	н	L	Ι	L	L	Н	Q10	Q2 ⁰	Q3 ⁰
	Н	L	L	Н	L	Q ₀ ⁰	L	Q2 ⁰	Q ₃ ⁰
Addressable latch	н	L	Н	Н	Ľ	Q ₀ ⁰	Н	Q2 ⁰	Q3 ⁰
Addiesodbie laten	н	L	Ĺ	L	н	Q ₀ ⁰	Q ₁ ⁰	L	Q3 ⁰
	Н	L	Н	L	Н	Q ₀ º	Q 1 ⁰	Н	Q3 ⁰
	Н	∟	L	Н	Н	Qo ⁰	Q 1 ⁰	Q2 ⁰	L
,	Н	L	Н	Ĥ	Н	Q ₀ ⁰	Q 1 ⁰	Q2 ⁰ .	Н

Note 1. X : Irrelevant

Q 0 : Indicates output status prior to input conditions being set.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5 ~ V _{CC}	٧
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted.)

Symbol	Parameter			Limits				
Symbol	Farameter		Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Іон	High-level output current	V _{OH} ≥2.7V	0		- 400	μA		
		V _{OL} ≤0.4V	0		4	mA		
lor	Low-level output current	0		8	m-A			

DUAL 4-BIT ADDRESSABLE LATCH

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

C 11	Parameter		T	- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1		Limits		
Symbol	Farameter	Test conditi	ions	Min	Typ ∗	Max	Unit	
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
VIC	Input clamp voltage		V _{CC} =4.75V, r _{IC} =-1	8mA			-1.5	. V
Voн	High-level output voltage		$V_{CC}=4.75V \cdot V_{I}=0.8$ $V_{I}=2V \cdot I_{OH}=-400/4$		2.7	3.4		V
V I ambantantantantantantantantantantantantanta		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V	
VoL	Low-level output voltage	w-level output voltage		IoL=8mA		0.35	0.5	
		M/C		V F 25V N 2 7V			40	μA
ин	High-level input current	Exclusive of M/C	V _{CC} =5.25V, V _I =2.7V				20	,,,,
чн	High-level input current	M/C	V _{CC} =5.25V. V _I =10V				0.2	mA
		Exclusive of M/C					0.1	
	Law level is not a correct	M/C	V 5 05V V 0 4V	.,			-0.8	
lı_	Low-level input current	Low-level input current Exclusive of M/C		V _{CC} =5.25V. V _I =0.4V			-0.4	mA
los	Short-circuit output current (Note	e 2)	V _{CC} =5.25V, V _O =0V		-20		— 100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			20	36	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

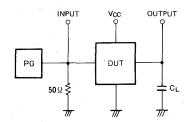
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
	r diditioto,	rest conditions	Min	Тур	Max	Unit
tpHL	High-to-low-level output propagation time, from input \overline{R} to output $Q_0{\sim}Q_3$		i.	9	27	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			15	32	ns
tpHL	time, from input D to output Q ₀ ~Q ₃			11	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		15	38	ns
tpHL	time, from input S_A , S_B to output $Q_0 \sim Q_3$	e e e		- 11	29	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			14	35	ns.
tpHL	time, from input M/C to output $Q_0 \sim Q_3$			13	24	"ns

TIMING REQUIREMENTS (Vcc=5V, Ta=25°C, unless otherwise noted)

Symbol	Symbol Parameter		Total pandial and	Limits			Unit
Symbol,			Test conditions		Min Typ Max		Unit
t _{su (DH)}	D high-level setup time to M/C			15	10		ns
th (DH)	D high-level hold time to M/C	3.00	The second secon	5	- 5		ns
t _{su (DL)}	D low-level setup time to M/C		•	15	8		ns
th(DL)	D low-level hold time to M/C			5	- 7		ns
t _{su(S)}	S _A , S _B setup time to M/C			15	7		ns
th(s)	S _A , S _B hold time to M/C		and the second second	5	- 5		ns
tw(M/C)	M/C pulse width			15	8		ns
tw(R)	R pulse width			15	7		ns

Note 4. Measurement Circuit

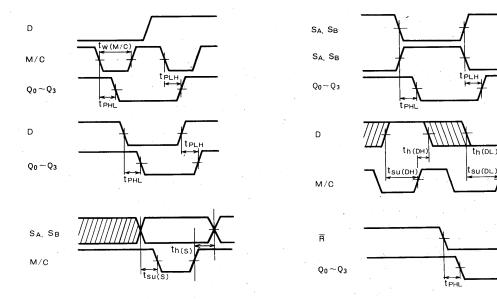


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6$ ns, $t_f = 6$ ns, $t_W = 50$ 0ns, $V_P = 3V_{P,P}$, $Z_O = 50\Omega$. (2) C_L includes probe and jig capacitance.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3.} I_{CC} is measured with all inputs at 0V.

DUAL 4-BIT ADDRESSABLE LATCH



Note 5. Shaded area denotes the time period in which switching is possible.

M74LS257AP

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS257AP is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Output control input common to all four circuits
- 3-state outputs
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

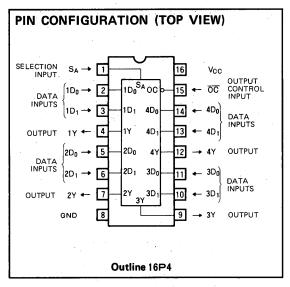
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 1-line selection of 2 input signals using four multiplexer circuits which convert the 2-bit parallel data into serial data by time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1 , and 1 data is specified from among the data input from selection input S_A , the input signal is output at Y.

 S_A and output control \overline{OC} are common to all four circuits. When \overline{OC} is set high, 1Y, 2Y, 3Y and 4Y are put in the high-impedance state irrespective of the status of the other inputs.

M74LS257AP has the same functions and pin connections as M74LS157P but the latter is provided with active pull-up resistor outputs.

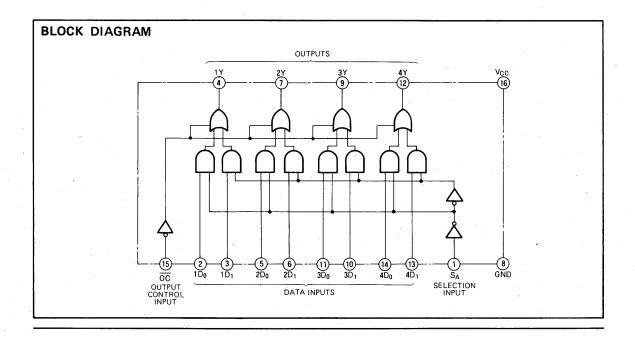


FUNCTION TABLE (Note 1)

ōc	SA	D ₀	D ₁	Y
н	×	X	×	Z
L	L	L	Х	L
L	L	н	Х	Н
L	Н	Х	L	L
L	н	×	Н	н

Note 1 X : Irrelevant

Z: High-impedance state



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Cumbal	Symbol Parameter			Limits				
Symbol			Min	Тур	Max .	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
1 он	High-level output current	V _{OH} ≧2.4V	0		-2.6	mΑ		
		V _{OL} ≤0.4V	0		12	mA		
IOL	Low-level output current	V _{OL} ≤0.5V	0		24	mA		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \,^{\circ}C$, unless otherwise noted)

0	Parameter				Limits		Unit	
Symbol	rarameter		lest conditi	Test conditions		Typ *	Max	Onit
ViH	High-level input voltage				2			V
ViL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{1C} =-11	8mA			-1.5	V
Voн	High-level output voltage		$V_{CC}=4.75V$, $V_{I}=0.8V$ $V_{I}=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
1/-	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 12mA		0.25	0.4	V
V _{OL}	Low-level carpat voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	V
. lozh	Off-state high-level output curre	nt	V _{CC} =5.25V, V _I =2V, V _O =2.4V				20	μА
lozL	Off-state low-level output curren	nt	V _{CC} =5.25V, V _I =2V,	V ₀ =0.4V			-20	μА
		D ₀ , D ₁ , OC	V _{CC} =5.25V				20	
	High-level input current	SA	V _I =2.7V				40	μΑ
ин	riigir-ievei iliput current	D ₀ , D ₁ , OC	V _{CC} =5.25V				0.1	
-		S _A	V _I =10V				0.2	mA
1	Low level in must assess	D ₀ , D ₁ , OC	V _{CC} =5.25V				-0.4	
h <u>∟</u> .	Low-level input current	SA	V _I =0.4V				-0.8	mA
los	Short-circuit output current (No	ote 2)	V _{CC} =5.25V, V _O =0V		-30		- 130	mA
Госн	Supply current, all outputs high		V _{CC} =5.25V (Note 3)		4	6.2	10	mΑ
ICCL	Supply current, all outputs low		V _{CC} =5.25V (Note 4)			10	16	mA
locz	Supply current, all outputs off		V _{CC} = 5.25V (Note 5)		1	12	19	mA

 \bigstar : All typical values are at $V_{CC} = 5V$, $T_a = 25 ^{\circ} C$.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with \overline{OC} , S_A , D_1 at 0V and D_0 at 4.5V

Note 4: I CCL is measured with all inputs at OV.

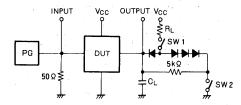
Note 5: 1_{CCZ} is measured with \overline{OC} at 4.5V and all other inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

0	Parameter	Tourist	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	18	ns
tpHL	time, from inputs Do, Do to output Y			8	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL=45pF (Note 6)		11	28	ns
t _{PHL}	time, from input SA to output Y			11	35	ns
t _{PZH}	Output enable time to high-level	$R_L = 667 \Omega$ $C_L = 45 pF$ (Note 6)		7	22	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 6)		9	35	ns
t _{PLZ}	Output disable time from low-level	R _L =667Ω, C _L =5 pF (Note 6)		11	26	ns
t _{PHZ}	Output disable time from high-level	R _L =667Ω, C _L =5 pF (Note 6)		8	35	ns

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

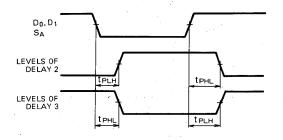
Note 6: Measurement circuit

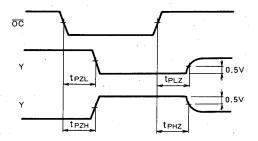


Symbol	SW1	SW2
tрzн	Open	Closed
tezu	Closed	Open
tplz	Closed	Closed
tphz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$.
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

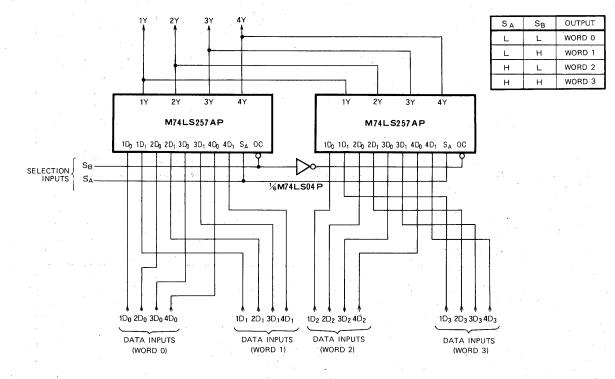
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

4-line to 1-line data selector (multiplexer)



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS258AP is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits with 3-stage outputs.

FEATURES

- Inverted outputs
- Output control input common to all four circuits
- Select input common to all four circuits
- 3-state outputs
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

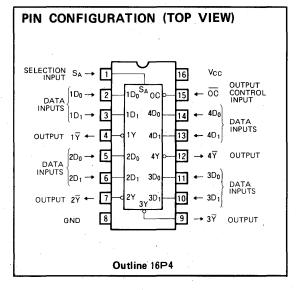
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC contains four sets of circuits which are used 1-line selection 2 input signals and as both data selectors, selecting 1-line out of 2 input signals, and multiplexers which convert the 2-bit parallel data into serial data by time-sharing. When one out of 2-line signals, which are applied to the data inputs D_0 and D_1 , is specified by select from input S_{Δ} , inverted signal of that appears at output \overline{Y} .

 S_A and output control \overline{OC} are common to all four circuits. When \overline{OC} is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are put in the high-impedance state irrespective of the status of the other inputs.

M74LS258AP has the same functions and pin connections as M74LS158P but the latter is provided with active pull-up resistor outputs.

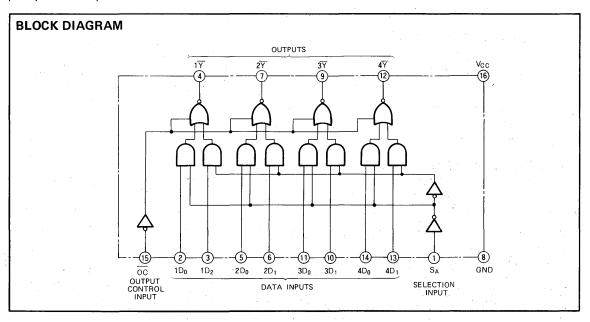


FUNCTION TABLE (Note 1)

OC '	SA	D ₀	D ₁	Ÿ
Н	Х	X	Х	Z
L	L		Х	Н
L	L	`Н	Х	L
, L	Н	×	L	Н
L	н	Х	н	L

Note 1 X : Irrelevant

Z: High-impedance state



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = -20 - +75 %, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambient temperature range		−20∼+75	C
Tstg	Storage temperature range		- 65∼ + 150	r

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted.)

	Parameter			Unit		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
I он	High-level output current	V _{OH} ≥2.4V	0		-2.6,	mA
	Low-level output current	V ₀ L≦0.4V	0		12	mA
1 OL	1 OL Low-level output current	V _{0L} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter				Limits		
Symbol	Paramete		Test conditions	Min	Typ *	Max	Unit
ViH	High-level input voltage	<u> </u>		2			V
VIL	Low-level input voltage					0.8	. V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA			- 1.5	٧
Vон	High-level output voltage		$V_{OC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-2.6 \text{ mA}$	2.4	3. 1		٧
	I am la al ante de calego		V _{CC} =4.75V I _{OL} = 12mA		0.25	0.4	V
VoL	Low-level output voltage		V _I =0.8V, V _I =2V I _{OL} =24mA		0.35	0.5	٧ .
lozh	Off-state high-level output curr	ent	$V_{CC}=5.25V, V_{I}=2V, V_{O}=2.7V$			20	. μΑ
lozL	Off-state low-level output curre	nt .	V _{CC} =5.25V, V _I =2V, V _O =0.4V			-20	μΑ
		D ₀ , D ₁ , OC	V _{CC} =5.25V			20	
1 _{1H}	High-level input current	SA	V _I =2.7V			40	μΑ
чн	Trigit level input carrent	D ₀ , D ₁ , OC	V _{CC} =5.25V			0.1	4
		SA	V _I =10V			0.2	mA
l _{IL}	Low-level input current	D ₀ , D ₁ , OC	V _{CC} =5.25V			-0.4	mΑ
'IL	Low-level input current	SA	V _I =0.4V			-0.8	, IIIA
los	Short-circuit output current (N	ote 2)	V _{CC} =5.25V, V _O =0V	- 30		- 130	mA
Іссн	Supply current, all outputs high	1	V _{CC} =5.25V (Note 3)		4.5	7	mA
ICCL	Supply current, all outputs low		V _{CC} =5.25V (Note 4)		8.8	14	mA,
locz	Supply current, all outputs off		V _{CC} =5.25V (Note 5)		12	19	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with all inputs at 0V.

Note 4: I_{CCL} is measured with \overline{OC} , S_A and D_1 at 0V and D_0 at 4.5V.

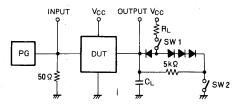
Note 5: I CCZ is measured with \overline{OC} at 4.5V and all other inputs at OV.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta = 25 ℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Links
Symbol	Farameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			5	18	ns
tpHL	time, from inputs D_0 , D_1 to output \overline{Y} .	O = 45 = 5 (Note 6)	2	8	18	. ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	CL == 45pF (Note 6)		9	28	ns
t _{PHL}	time, from input SA to output Y			16	35	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 6)		7	22	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 6)		12	35	ns
t _{PLZ}	Output disable time from low-level	R _L =667Ω, C _L = 5 pF (Note 6)		11	26	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667 \Omega$, $C_L = 5 pF$ (Note 6)		8	35	ns

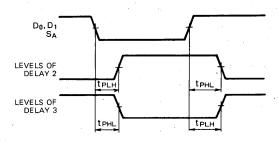
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

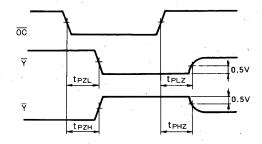
Note 6: Measurement circuit



Symbol	SW1	SW2
teze	Open	Closed
tpzL	Closed	Open
tpLz	Closed	Closed
tpHz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_O =50 Ω .
- (2) All diodes are switching diodes.
- (3) C_L includes probe and jig capacitance





M74LS259P

8-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS259P is a semiconductor integrated circuit containing 8 latch circuits and a demultiplexer which designates the latches with a 3-bit binary code.

FEATURES

- Easy bit expansion
- Usable as 3-bit binary/octal decoder/demultiplexer
- Direct reset input provided
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of a 3-bit binary/octal demultiplexer and 8 latch circuits. The following operational modes can be selected by combining the mode control input M/C with the reset input $\overline{\mathbb{R}}$

(1)	3-bit binary/octal	M/C: Low;
	decoder/demultiplexer	R: Low
(2)	Addressable latch	M/C: Low;
		ឨ: High
(3)	Data input inhibit	M/C: High
		ឨ: High
(4)	Reset	M/C: High;

 $$\overline{R}$$: Low When this device is used as a 3-bit binary/octal decoder/demultiplexer and the select inputs $S_A \simeq S_C$ are designated

PIN CONFIGURATION (TOP VIEW)

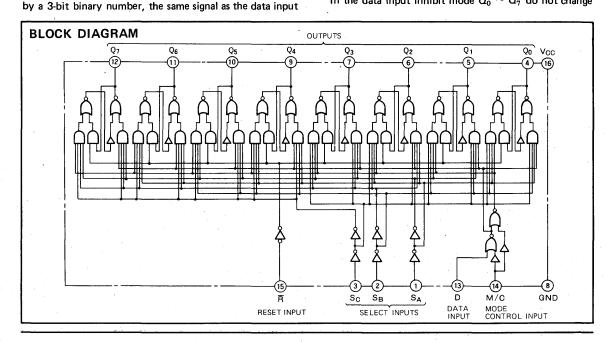
SELECT SB \rightarrow 2 SB SA R \rightarrow 15 \leftarrow RESET INPUT MODE CONTROL INPUT OUTPUTS Q0 \leftarrow 4 Q0 D 13 \leftarrow D DATA INPUT Q2 \leftarrow 6 Q2 Q6 11 \rightarrow Q6 Q3 \leftarrow 7 Q3 Q4 Q5 10 \rightarrow Q5 GND 8 \rightarrow 9 \rightarrow Q4

Outline 16P4

D appears in one of the outputs $\mathbf{Q}_0 \sim \mathbf{Q}_7$ corresponding to that number and all the other outputs are set low. There is no latch operation in this mode.

When used as an addressable latch and inptus $S_A \sim S_C$ are designated as above, the corresponding latch is selected and the same signal as D appears in the output. When M/C changes from low to high (data inhibit mode), the information from the data input D immediately before the change is latched. When M/C is low, the signal appearing in Q is also changed if the signal D is changed.

In the data input inhibit mode $Q_0 \sim Q_7$ do not change



8-BIT ADDRESSABLE LATCH

even if D is changed and the status before M/C is set high is held.

With direct resetting, all the outputs are reset low irrespective of the status of D and $\rm S_A \sim S_C$.

FUNCTION TABLE (Note 1)

Operational mode	Ŗ	M/C	D	SA	SB	Sc	Q ₀	Q1	Q ₂	Q3	Q4	Q5	Q ₆	Q7
Reset	L	Н	Х	Х	χ.	Х	L	L	L	L	L	Ļ	L	L
	L	L	L	L	L	L	L.	L	L	L	L	L	L	L
	L.	L	• н	L	L	L	Н	L	L	L	L	L	L	L
3-bit binary/octal	L	L	L	Н	L	L	L	L	L	L	L	L	L	L
decoder/demultiplexer	L	L	Н	Н	L	L	L	Н	L	L	L ·	L	L	L
	:	:	:	:	:	:	÷	:	÷	:	:	:	:	:
	L	L	L	Н	Н	Н	L	L	L	L	L	L	L	L.
	L	L	н.	Н	Н	Н	L	L	L	L	L	L	L	н
Data input inhibit	н	н	Х	Х	Х	Х	Q ₀ 0	Q1 ⁰	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q6 ⁰	Q7 ⁰
	Н	L	L	L	L	L	L	Q ₁ n	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
	Н	L	Ι	L	L	L	Н	Q1 ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q6 ⁰	Q7 ⁰
	Н	L	·L	Н	L	L	Q ₀ 0	L	Q 2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰
Addressable latch	Н	L	Н	н	L	L	Q ₀ 0	н	Q 2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Qe ⁰	Q7 ⁰
·	:	:	:	:	:	:	:	:	:	:	:	:	÷	:
	Н	L	L	н	Н	Н	Q ₀ 0	Q1 ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	L
	Н	L	Н	Н	. Н	Н	Q ₀ 0	Q1 ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q6 ⁰	н

Note 1 X : Irrelevant

Q0: Level of Q before the indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0:5∼ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter			11.5		
Symbol		er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
	łoL Low-level output current	V _{OL} ≦0.4V	0		4	mA
OL		. V _{OL} ≦0.5V	0		8	mA

8-BIT ADDRESSABLE LATCH

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted).

Combal		Parameter Test conditions			Limits		Unit
Symbol	Parameter	Test conditions		. Min	Typ *	Max	Onit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Vou High-level output voltage	V _{CC} =4.75V, V ₁ =0	8V	0.7	3.4		v	
VoH	VOH High-level output voltage	$V_1 = 2V \cdot I_{OH} = -400 \mu A$		2.7	3.4		V
	Low-level output voltage	V _{CC} =4.75V	$I_{OL} = 4 \text{ mA}$		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8 V. V_1 = 2 V$	I _{OL} =8mA		0.35	0.5	V
1	High-level input current	V _{OC} =5.25V, V _I =2.	7 V			20	μА
ίн	High-level input current	V _{CC} =5.25V, V _I =10	V _{CC} =5.25V, V _I =10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	- 20		- 100	mA
. loc	Supply current	V _{CC} =5.25V (Note 3)		22	36	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at OV.

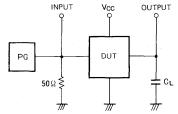
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			
Symbol	Parameter	l'est conditions	Min	Тур	Max	Unit	
tpHL	High-to-low-level output propagation time, from input \overline{R} to outputs $Q_0 \sim Q_7$			9	27	ns	
tplH	Low-to-high-level, high-to-low-level output propagation			15	32	ns	
tpHL	time, from input D to outputs Q0~Q7			12	21	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF		15	38	ns	
t _{PHL}	time, from inputs SA, SB, SC to outputs Q0~Q7			12	29	ns	
tpLH	Low-to-high-level, high-to-low-level output propagation			14	35	ns	
tpHL	time from input M/C to outputs Q0~Q7			13	24	ns	

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

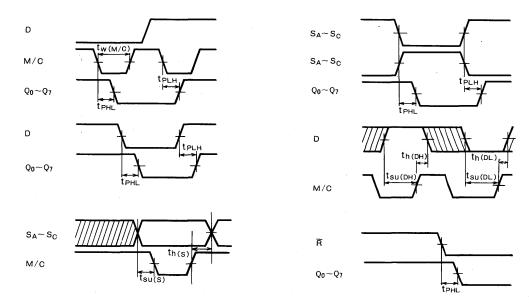
Symbol	Davasana	Test conditions		Unit		
Зуппон	Parameter .	est conditions	Min	Тур	Max	I Onit
t _{su (DH)}	Setup time D high to M/C		15	10		ns
t _{h (DH)}	Hold time D high to M/C		5	-5		ns
t _{su (DL)}	Setup time D low to M/C		15	8		ns
th(DL)	Hold time D low to M/C		5	- 7		ns
t _{su(s)}	Setup time SA, SB to M/C		15	7		. ns
th(s)	Hold time SA, SB, to M/C		5	5		ns
tw(M/C)	M/C input pulse width		15	8	1.	ns
tw(R)	R input pulse width		15	. 7		ns

Note 4: Measurement circuit



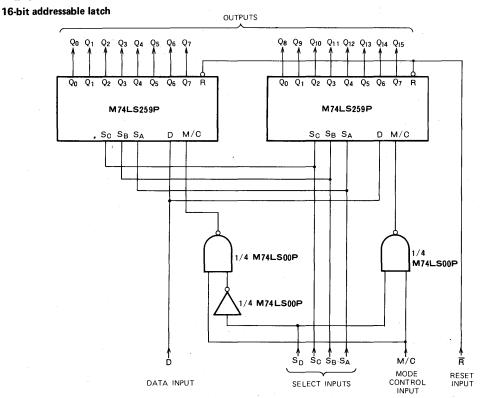
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE



M74LS266P

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS266P is a semiconductor integrated circuit containing four integral open-collector output circuits configured into dual input exclusive NOR gates.

FEATURES

- "wire-AND" capability
- Capable of gating high output voltages (V_O ≥ 7V)
- Low power dissipation (Pd = 40mW typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

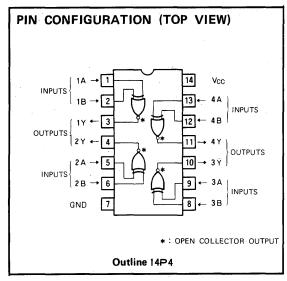
FUNCTIONAL DESCRIPTION

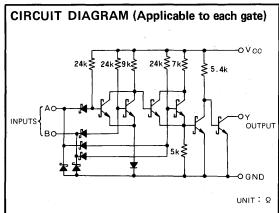
The use of open-collector output circuits in this device gives the user the option of varying high-level output impedance via an external resistance. It is thus possible to implement an AND tie which is not possible in conventional gates.

When both inputs A and B are either high or low-level, output Y goes high-level. Conversely, when A and B are high — low, or low — high with respect to each other, Y will be low-level.

FUNCTION TABLE

Α	В	Υ
L	L	н
Н	_	L
L	Ι	L
Н	. н	н





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		20 + 75	°C
Tstg	Storage temperature range		- 65~ + 150	°C



QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	ol Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
юн	High-level output current	V ₀ = 5.5V	0		100	μА	
	I _{OL} Low-level output current	V _{OL} ≤ 0.4V	0		4	mA	
OL		V _{OL} ≦ 0.5 V	0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

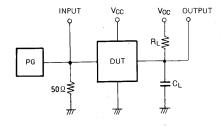
Symbol	Parameter	Ŧ .	Test conditions		Limits		
Symbol	Parameter	lest cond	itions	Min	Typ *	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
	High-level output current	V _{CC} =4.75V, V ₁ =0.8	BV			100 -	μА
Іон	nigh-level output corrent	V ₁ =2V, V ₀ =5.5V	$V_1 = 2V$, $V_0 = 5.5V$			100	μА
.,	Landard and an artist to a	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	٧
	History and the second	V _{CC} =5.25V, V _I =2.7	V			40	μА
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =10V	/			0.2	mA
l _I L	Low-level input current	V _{CC} =5.25V, V _I =0.4	V _{CC} =5.25V, V _I =0.4V			-08	· mA
Icc	Supply current	V _{CC} =5.25V (Note 1)			8	13	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = $25^{\circ}C$.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

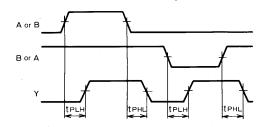
Complete	Parameter	Test conditions		Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Onic
tpLH	1	$R_L = 2 k\Omega$		16	30	ns
tenL	Low-to-high-level, high-to-low-level output	C _L = 15 pF Other input low-level (Note 2)		16	30	ns
tpLH	propagation time	$R_L = 2 k\Omega$		14	30	ns
tpHL	* *	C _L = 15 pF Other input high-level (Note 2)		14	30	ns

Note 2. Measurement Circuit



- (1) The pulse generator has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
 (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



Note 1. I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS273P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common direct reset and clock inputs.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Direct reset and clock inputs common to all 8 circuits
- Wide operating temperature range (T_a = −20~+75°C)

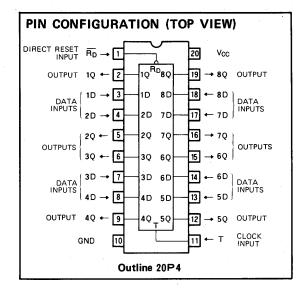
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with direct reset $\overline{R_D}$ input and clock input T common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

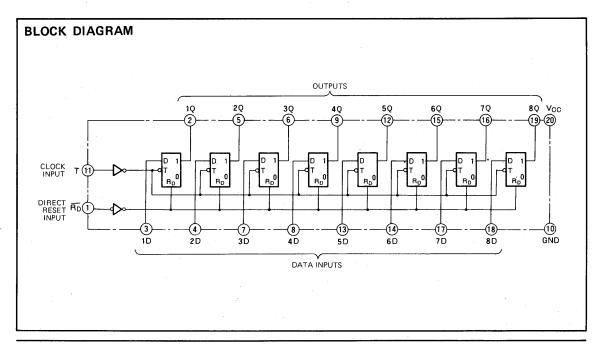
When $\overline{R_D}$ is set low, 1Q through 8Q are all set low irrespective of the status of the ID through 8D and T signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.



FUNCTION TABLE (Note 1)

R _D	T	D	Q
L	X	X	L
Н	1	н	н
Н	1	L	L
н	L	х	Q0

- Note 1 \uparrow : Transition from low to high (positive edge
 - trigger)
 - Q0: Level of Q before the indicated steady-state input conditions were established.
 - X : Irrelevant



OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
V ₀	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~ + 75	℃
Tstg	Storage temperature range		-65~+150	°

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted.)

	Symbol Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА	
	Low-level output current	V _{OL} ≤0.4V	0		4	mA	
lo _L		V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted.)

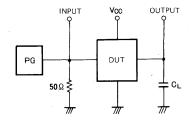
Cumbal	Parameter	T	Test conditions		Limits		
Symbol		Test cond	itions	Min	Тур 🛊	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	-18mA			-1.5	V
	High-level output voltage	V _{CC} =4.75V, V _I =0.	.8V	2.7	2.4		
V _{OH}	High-level output voltage	V _I =2V, I _{OH} =-400	uΑ	2.7	3.4		V
.,	Low food output value	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	$V_{1}=0.8V, V_{1}=2V$	I _{OL} =8mA		0.35	0.5	V
1 .	High level in the second	V _{CC} =5.25V, V _I =2.	7V			20	μА
ин	High-level input current	V _{CC} =5.25V, V _I =10	V	_		0.1	mA
liL	Low-level input current	V _{CC} =5.25V, V _I =0.	4V		-	-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	-20		- 100	mA
loc	Supply current	V _{CC} =5.25V (Note 3)		17	27	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0	Parameter	Test conditions	Limits			Unit
Symbol	Fallameter	rest conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock frequency		30	40		MHz
tply	Low-to-high-level, high-to-low-level output propagation			12	27	ns
tPHL	time, from T to 1Q~8Q	G _L =15pF (Note 4)		13	27	ns
t _{PHL}	High-to-low-level output propagation time, from $\overline{R_D}$ to $1Q \sim 8Q$			15	27	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P = 3V_{PP}$, $Z_O = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

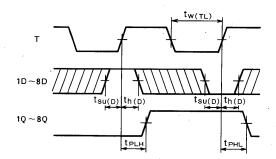
Note 3: I_{CC} is measured after 1D ~ 8D and $\overline{R_D}$ are made 4.5V and T has been changed from 0V to 4.5V.

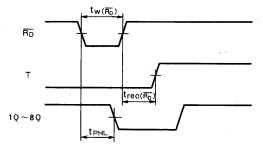
OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Combat	Parameter	Test conditions	Limits			Unit
Symbol	raiametei		Min	Тур	Max	Onit
t _{W(TL)}	Clock input T low pulse width		20	7		ns
tw (RD)	Direct reset pulse width		20	6		ns
t _{SU (D)}	Setup time 1D~8D to T		20	7		ns
t _{h(D)}	Hold time 1 D ~ 8D to T		5	-3		ns
trec(RD)	Recovery time RD to T		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance,

QUADRUPLE R-S LATCH

DESCRIPTION

The M74LS279P is a semiconductor integrated circuit containing 4 R-S flip-flop circuits.

FEATURES

- High breakdown input voltage (V_I ≥ 15V)
- High breakdown output voltage (V_O ≥ 7V)
- Low power dissipation (P_d = 19mW typical)
- Low output impedance
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

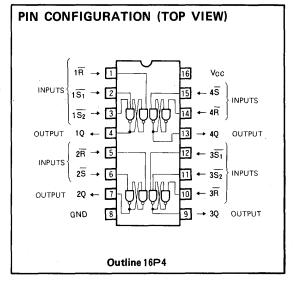
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Two of the 4 circuits have set inputs \overline{S}_1 and \overline{S}_2 and reset input \overline{R} and the other 2 circuits have \overline{S} and \overline{R} inputs.

When $\overline{S_1}$ or $\overline{S_2}$ or both are low or \overline{S} is low, high appears in output Ω , and when R is low, low appears in output Ω . When $\overline{S_1}$ or $\overline{S_2}$ or both are low and \overline{R} is low, high appears in the output but when each of the inputs is set high at the same time, the status of Ω cannot be anticipated.

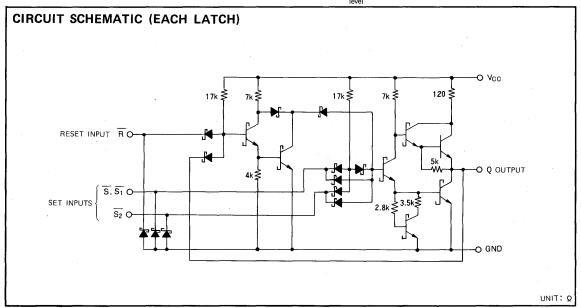


FUNCTION TABLE (Note 1)

S ₁	S ₂	R	n
			H*
<u> </u>	X		
Х	L	L	н*
L	X	Н	I
Х	L	Н	н
Н	н	L	L
Н	н	н	Ó۲

Note 1 Q⁰: Level of Q before the indicated steadystate input conditions were established

- X: Irrelevant
- *: Nonstable, it will not persist when \overline{R} , $\overline{S_1}$ and $\overline{S_2}$ return to their inactive (high)



QUADRUPLE R-S LATCH

ABSOLUTE MAXIMUM. **RATINGS** ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted,)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	ΰ
Tstg	Storage temperature range		65~ + 150	ຽ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

	D			Limits		: Unit
Symbol	Paramete		Min	Тур	Max	Onit
Vcc	Supply voltage		4.75	5	5.25	V
1он	High-level output current	V _{OH} ≥2.7V	0		-400	μΑ
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

County - 1	Parameter	Tour		Limits			
Symbol	Parameter	l est condi	Test conditions		Typ *	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Vон	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8$ $V_{I}=2V, I_{OH}=-400\mu$		2.7	3.4		٧
.,		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL	Low-level output voltage	V _i =0.8V, V _i =2V	I _{OL} =8mA		0.35	0.5	V
,		V _{CC} =5.25V V _I =2.7V				20	μΑ
Тін	High-level input current	V _{CC} =5.25V V ₁ =10V				0.1	mA
lıL	Low-level input current	V _{CC} =5.25V V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _C =0V		-20		100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)			3.8	7	mA

^{* :} All typical values are at $V_{CC} = 5V$, Ta = 25°C

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

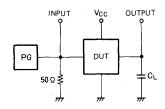
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit	
Symbol	raiametei	l est conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			6	22	ns
t _{PHL}	time, from input S to output Q	C _L =15pF (Note 4)		12	21	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{\mathbf{R}}$ to output \mathbf{Q}	0L 13p1 (Note 4)		12	27	ns

Note 3: I_{CC} is measured with all \overline{R} inputs at 0V and all \overline{S} inputs at 4.5V.

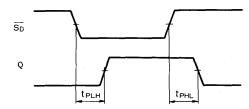
QUADRUPLE R-S LATCH

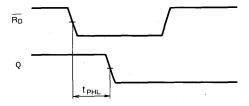
Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_P , Z_O = 50 Ω .
- (2). C_L includes probe and jig capacitance

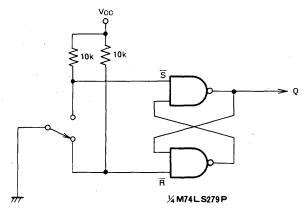
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Chattering prevention circuit



9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

DESCRIPTION

The M74LS280P is a semiconductor integrated circuit containing a 9-bit parity generator/checker function.

FEATURES

- Easy expansion of bits with cascade connection
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

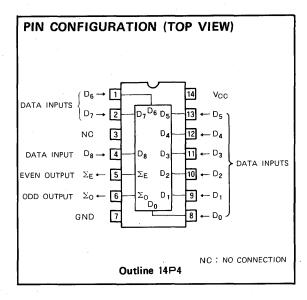
FUNCTIONAL DESCRIPTION

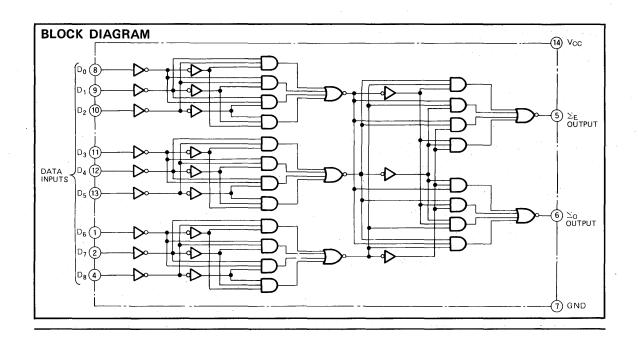
This device is provided with both a 9-bit parity generator and checker functions. For use as a parity generator, parity outputs in even output $\Sigma_{\rm E}$ and odd output $\Sigma_{\rm O}$ are obtained in accordance with the function table, depending on whether the number of high-level data in the inputs is even or odd when 9-bit data are applied to data inputs $D_0 \sim D_8$.

For use as a parity checker, one of the 9-bit data inputs is used for the even or odd parity designation and the remaining 8 bits are used as the data.

FUNCTION TABLE

Number of high-level data in input data.	ΣΕ	Σο
Even number	H	L
Odd number	L	Н





9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5∼ + 15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		- 20~ + 75	℃
Tstg	Storage temperature range		− 65 ∼ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Combat	Parameter		Limits		Unit		
Symbol	Parame	ter	Min Typ Max		Max		
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{OH} ≥2.7∨	. 0		-400	μА	
	L level eviteut ourrent	V _{OL} ≤0.4V	0		4	mA	
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA	

ELECTRICAL CHARACTERISTICS (Ta = $-20 \sim +75 \, ^{\circ} \! \text{C}$, unless otherwise noted)

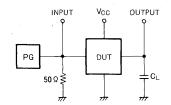
0	Parameter					Limits		
Symbol	raianeter		lest conditio	Test conditions		Тур 🛊	Max	Unit
VIH	High-level input voltage			,	2			V
VIL	Low-level input voltage						0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18	mA			- 1.5	V
VoH	High-level output voltage		V _{CC} =4.75V, V _I =0.8V		2.7	3.4		
VOH	riigiriever output voitage	Sotpat voltage	$V_1 = 2V$, $I_{OH} = -400\mu$ A	·		3.4		V V V V μΑ
Vol	Low-level output		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VOL	Low-level output	·	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
Lee	High-level input current		$V_{CC} = 5.25V, V_1 = 2.7V$				20	μΑ
hн ·	Thigh level alput content		$V_{CC} = 5.25V, V_I = 10V$				0.1	mA
IIL	Low-level input current		$V_{CC} = 5.25V, V_I = 0.4V$				-0.4	mA
los	Short-circuit output current (Note 1)		$V_{CC} = 5.25V, V_{O} = 0 V$		-20		100	mΑ
loc	Supply current		V _{CC} = 5.25V (Note 2)			16	27	mΑ

^{* :} All typical values are at V_{CC}= 5V, T_a= 25°C.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

Symbo!	Parameter	Test conditions		Limits		Unit
Symb	raiametei	lest conditions	Min	Тур	Max	Onit
tpLH	Low-to-high-level, high-to-low-level output propagation			22	50	ns
tpHL	time, from inputs $D_0 \sim D_8$ to output Σ_E	0 15-5 (N - 0)		17	45	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 3)		16	35	ns
t _{PHL}	time, from inputs $D_0 \sim D_8$ to output \geq_0	·		17	50	ns

Note 3: Measurement circuit



⁽¹⁾ The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 V_P -P, Z_Q =50 Ω .

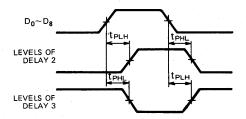
Note 1: All measurements should be done quickly.

Note 2: I_{CC} is measured with all inputs at 0V.

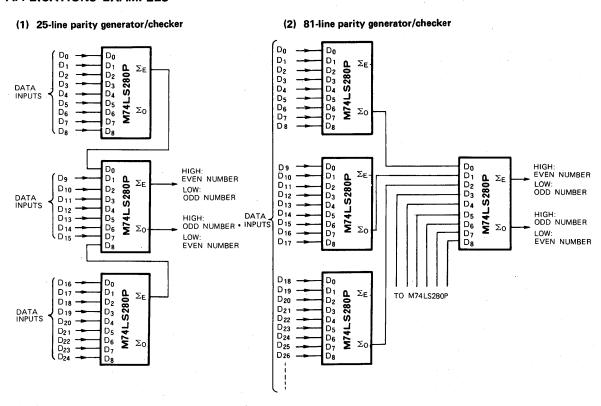
⁽²⁾ C_L includes probe and jig capacitance

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATIONS EXAMPLES



4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74LS283P is a semiconductor integrated circuit containing a 4-bit full adder function using the look-ahead carry method of operation.

FEATURES

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide operating temperature range (Ta = −20 ~ +75°C)

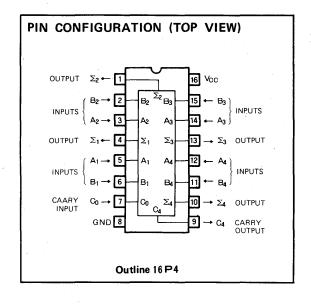
APPLICATION

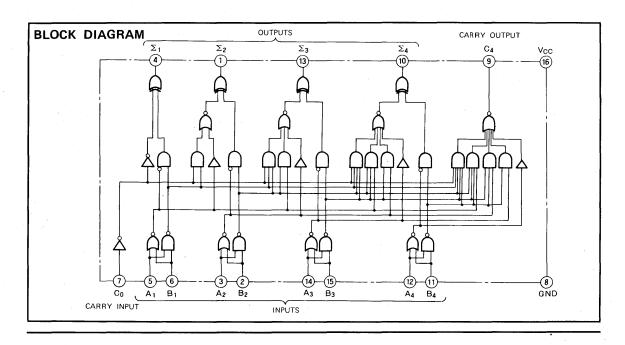
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions as a 2-group, 4-bit binary adder with full adder capability. When a 4-bit binary number is applied to input A_1 thru A_4 or B_1 thru B_4 and a carry signal from the previous column is applied to input C_0 , the sum output for the respective bits will appear at output $\Sigma_1 \sim \Sigma_4$; and carry output to the following column will appear at C_4 .

The full adder capability of this device is also complete with full look-ahead carry operations, and its high speed means that a 4-bit carry output is produced at an average rate of 8ns (typical). Thus, when N-stages are configured for parallel addition of an N-number of 4-bit inputs, a carry output can be obtained with a 8Nns delay time. (See the application example provided in the back of this specification sheet.) Also provided is the M74LS83AP with the same functions and electrical characteristics. This device differs only in its pin configuration.





4-BIT BINARY FULL ADDER WITH FAST CARRY

FUNCTION TABLE (Note 1)

	C _{k-1}	A _k	Bk	Σ_{k}	Ck
ĺ	L	L	L	L	L
	L	н	٦	н	L
	L.	L	н	н	L_
	٦	н	н	L	Н
	Н	L	L	Н	L
	Н	Н	L.	L	Н
	н	L	н	L	н
	Н	Н	Н	Н	Н

Note 1. $\Sigma_{\mbox{\scriptsize K}}$ and $\mbox{\scriptsize C}_{\mbox{\scriptsize K}}$ are the sum and carry output calculated in response to input at A_K , B_K , and $\mathsf{C}_{K\text{-}1}$ (carry input), derived from the following logical equation.

 $\Sigma_{K} = A_{K} \oplus B_{K} \oplus C_{K,1}$ $C_{K} = A_{K} + B_{K} + (A_{K} + B_{K}) \cdot C_{K,1}$ (Where K = 1~4; \oplus = Exclusive OR; + = OR; • = AND)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
Vı	Input voltage		0.5 ~ + 15	V
Vo	Output voltage	High-level state	-0.5 ~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65 - + 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Paramet			Unit		
Зупівої	ratatiet	er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	. 0		4	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20.- +75^{\circ}C$, unless otherwise noted)

Symbol	Paramete		Test cond	itions	Limits			Unit '
Зуппоот	ratamete	31	lest cond	Ittoris	Min	Тур *	Max	Onit
ViH	High-level input voltage	High-level input voltage			2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage	Input clamp voltage		18 mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.0$ $V_{I} = 2V, I_{OH} = -400\mu$		2.7	3.4		٧
V	Low lovel output values		V _{CC} = 4.75V	I _{OL} =4mA		0.25	0.4	V
V _{OL}	Low-level output voltage			I _{OL} = 8mA		0.35	0.5	
	High-level input current	V - 5 05V V 0 3				20		
		A1~A4. B1~B4	$V_{CC} = 5.25V, V_{I} = 2.7$	V			40	μ A
l _{IH}		Co	V _{CC} =5.25V, V _I =10V			0.1	mA	
		A1~A4, B1~B4				0.2		
	Low level in a town and	Co			-		-0.4	
liL.	Low-level input current	A1~A4. B1~B4	V _{CC} =5.25V, V _I =0.4V			-0.8	mΑ	
los	Short-circuit output current (Note 2) V _{CC} =5.25V, V _O =0V		,	-20		100	mA	
				V		22	39	
Icc ·	Supply current	*	V _{CC} =5.25V, V _I = 0	V, V _I = 4.5V(Note 3)		-19	34	mA ·
				5V		19	34	

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

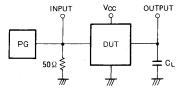
Note 3. I_{CC} is measured with $B_1 \sim B_4$ at 0V and with all other inputs 4.5V.

4-BIT BINARY FULL ADDER WITH FAST CARRY

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0	Parameter	Test conditions Limits			11.2	
Symbol	rarameter	lest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	24	ns
t _{PHL}	time, from input C_0 to outputs $\Sigma_1{\sim}\Sigma_4$,		13	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	24	ns
t _{PHL}	time, from inputs $A_1 \sim A_4$ or $B_1 \sim B_4$ to outputs $\Sigma_1 \sim \Sigma_4$	C ₁ = 15 pF (Note 4)		,11	24	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O[=13pr (Note 4)		8	17	ns
tehl	time, from inputs C ₀ to output C ₄			8	22	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	17	ns
tenL	time, from inputs A ₁ ~A ₄ or B ₁ ~B ₄ to output C ₄			8	17	ns

Note 4. Measurement Circuit



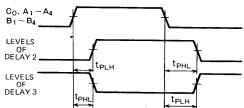
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_{P-P} , Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.

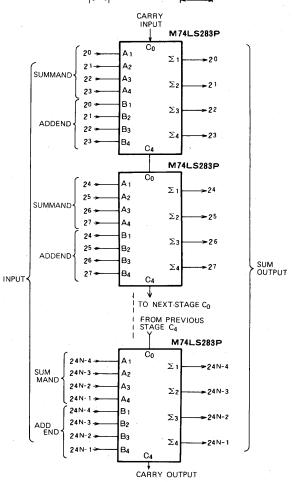
APPLICATION EXAMPLE

The accompanying diagram shows an N-number of M74LS283P devices connected in parallel for addition of an N-number of 4-bit inputs. Typical delay times for carry output in this circuit configuration are listed below. This figures indicates the suitability of this device for use in a high-speed adder employing the ripple-carry method.

N=1 (4 bits) 10.5 ns N=2 (8 bits) 21 ns N=3 (12 bits) 31.5 ns N=4 (16 bits) 42 ns N=8 (32 bits) 84 ns

TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI LSTTL: M74I \$290P

DECADE COUNTER

DESCRIPTION

The M74LS290P is a semiconductor integrated cirucit containing an asynchronous decade counter function with direct reset and direct 9-set inputs.

FEATURES

- Direct reset inputs provided
- Direct 9-set inputs provided
- Usable independently as binary and divide-by-5 counter
- High-speed counting (f_{max} = 75MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

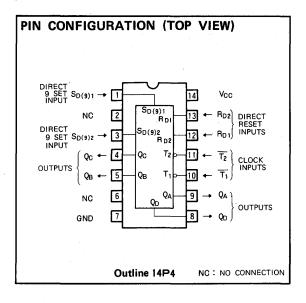
General purpose, for use in industrial and consumer equipment.

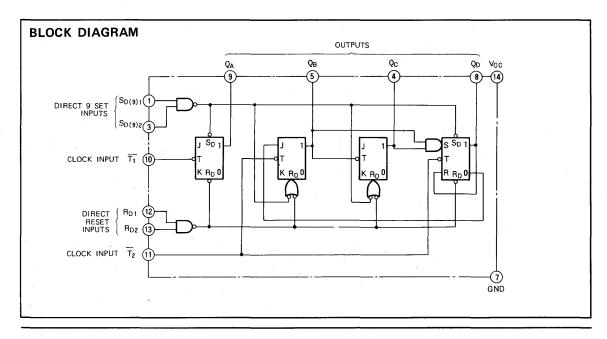
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A , Q_B , Q_C and Q_D . Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-5 counters can be reset or set to 9 simultaneously by setting direct reset inputs $R_{D\,1}$ and $R_{D\,2}$ and direct 9 set inputs $S_{D\,(9)\,1}$ and $S_{D\,(9)\,2}$ high. For use as a counter, either $R_{D\,1}$ or $R_{D\,2}$, or both, and $S_{D\,(9)\,1}$ or $S_{D\,(9)\,2}$, or both, are set low.

Also provided is the M74LS90P with the same functions and electrical characteristics. This device differs only in its pin configuration.





FUNCTION TABLE (Note 1)

Ŧ	R _{D1}	R _{D2}	S _{D(9)1}	S _{D(9)2}	QA	Qв	Qc	Q_{D}
Χ.	Н	Н	L	X	L	L	L	L
×	Н	Н	×	L	L	L	L	L
Х	×	X	H	Н	Н	L	L.	н
	L.	Х	L	Х		Coi	unt	
1	×	L	Х	L		Coi	unt	
1	L	, X	X	L	Count			
1	х	· L	L	×	Count			

Note 1: \$\dagger\$: Transition from high to low

X : Irrelevant

Count number	QA	Qв	Qc	QD
0	L	L	, L	L
1 .	н	L	L	L
2	L	Н	L	L
3	н	н	L.	L
4	٦	L	н	L
5	Ι	L	н	L
6	L	Н	н	٦
7	н	н	н	L
. 8	· L	L	L	н
9	Н	L	L	Н

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 \,^{\circ}$ C, unless other wise noted)

Symbol	Parameter	Parameter Conditions		Unit	
Vcc	Supply voltage		-0.5~+7	V	
Vı	Input voltae	Inputs $\overline{T_1}, \overline{T_2}$		$-0.5 \sim +5.5$	
VI .	input voitae	Inputs R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	-0.5 ~ +15	7 V	
V ₀	Output voltage	High-level state	-0.5∼ V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		−65∼+150	τ	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \, \text{C}$, unless otherwise noted)

St				Limits		
Symbol	Parame	ter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.7V	0		- 400	μΑ
		V _{OL} ≤0.4V	0		4	mA
OL	Low-level output current	V _{0L} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

Cumbal		Parameter	Test condi	41		Limits		Unit
Symbol		Parameter	l est condi	tions	Min	Typ *	Max	
ViH	High-level input vo	Itage			- 2			V
VIL	Low-level input vol	tage					0.8	٧
Vic	Input clamp voltage	e . •	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
Voн	OH High-level output voltage		$V_{CC}=4.75V$, $V_{I}=0.8$ $V_{I}=2V$, $I_{OH}=-400$		2.7	3.4		V
Va	V _{OL} Low-level output v	oltata	V _{CC} =4.75V	IOL=4 mA (Note 2)		0.25	0.4	٧
VOL	2017 lovel output voltate		$V_i = 0.8V, V_i = 2V$	I _{OL} =8 mA (Note 2)		0.35	0.5	٧
		R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}					20	
		T ₁	V _{CC} =5.25V, V _I =2.7	v			40	μA
1	High-level	T 2 .					. 80	
ін	input current	T ₁					0.2	
		T ₂	$V_{CC} = 5.25V, V_I = 5.5$	v ·			0.4	mA
	-	R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}	V _{CC} =5.25V, V _I =10V	′			0.1	mA
	Low-level	R _{D1} , R _{D2} , S _{D(9)1} , S _{D(9)2}					-0.4	
h∟	input current	Tı	V _{CC} =5.25V, V _I =0.4V				-2.4	m A
<u> </u>		T ₂					-3.2	
los	Short-circuit outpu	t current (Note 3)	V _{CC} =5.25V, V _O = 0 \	/	-20		— 100	mA
loc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mΑ

* : All typical values are at $V_{CC} = 5 \text{ V}$, $T_a = 25 ^{\circ}\text{C}$.

Note 2: Output Q_A should be tested with input $\overline{T_2}$ connected to output Q_A .

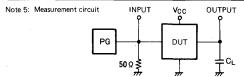
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T_1}$, $\overline{T_2}$, $S_{D\{9\}1}$ and $S_{D\{9\}2}$ at 0V after R_{D1} and R_{D2} have been set to 0V after 4.5V.

DECADE COUNTER

SWITCHING CHARACTERISTICS ($V_{CO}=5$ V, $T_a=25$ °C, unless otherwise noted)

		T		Limits		11-14
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	$\begin{array}{c} \text{Maximum clock frequency,} \\ \text{from input T_1 to output Q_{Δ}} \end{array}$		32	75		MHz
fmax	Maximum clock frequency, from input \overline{T}_2 to output Q_B		16	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	16	ns
t _{PHL}	time, from input T1 to output QA			8	18	ns
tpLH	Low-to-high-level, high-to-low-level output propagation			15	48	ns
t _{PHL}	time, from input T2 to output QB			16	50	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	*		7	16	ns
t _{PHL}	time, from input T2 to output QC			8	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0 45 5 (N5)		15	32	ns
tphL	time, from input T2 to output QD	C _L =15pF (Note 5)	,	15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	32	ns
t _{PHL}	time, from input $\overline{T_1}$ to output Q_D			8	35	ns
t _{PHL}	Low-to-high-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QA, QD			17	40	ns
t _{PLH}	High-to-low-level output propagation time, from inputs SD(9)1, SD(9)2 to outputs QB, QC			10	30	ns
t _{PHL}	High-to-low-level output propagation time, from inputs RD1, RD2 to outputs QA, QB, QC, QD			14	40	ns

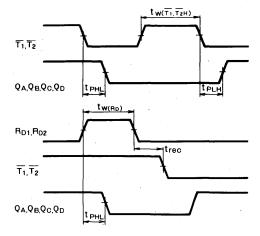


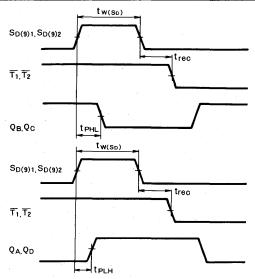
- (1) The pusle generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Tara and dialan		Unit		
Symbol	r arameter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width		15	6		ns
tw(T₂H)	Clock input T ₂ high pulse width	· · · · · · · · · · · · · · · · · · ·	30	17		ns
tw(RD)	Direct reset RD1, RD2 pulse width		15	5		ns
tw(SD)	Direct 9 set Sp(9)1, Sp(9)2 pulse width		15	5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(RD)	Recovery time R _{D1} , R _{D2} to $\overline{T_1}$, $\overline{T_2}$.		25	8		ns
trec(SD)	Recovery time $S_D(9)_1$, $S_D(9)_2$ to $\overline{T_1}$, $\overline{T_2}$	<u> </u>	25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





MT4LS293P

4-BIT BINARY COUNTER

DESCRIPTION

The M74LS293P is a semiconductor integrated circuit containing an asynchronous 4-bit binary (hexademical) counter function with direct reset inputs.

FEATURES

- Direct reset inputs provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max} = 60MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

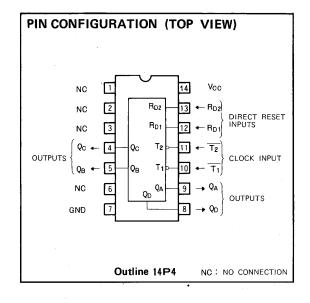
APPLICATION

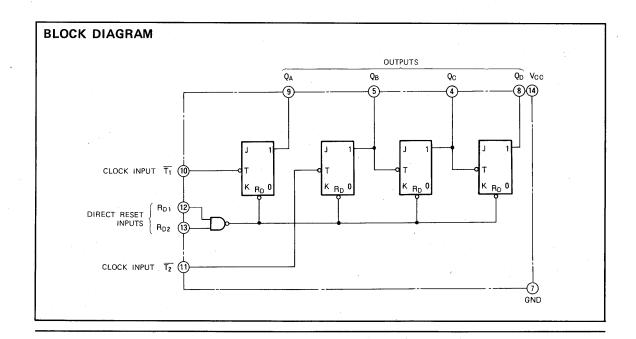
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B , Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A , Q_B , Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and octal counters can be reset simultaneously by setting direct reset inputs R_{D1} and R_{D2} high. For use as a counter, either R_{D1} or R_{D2} , or both, is set low. This pin has the same functions and electrical characteristics as the M74LS93P; only its pin configuration is different.





4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

Ţ	R _{D1}	R _{D2}	QΔ	Qв	Qc	Q D	
X	Н	. Н ⋅	L	L	L	L	
1	L	н	Count				
↓	Н	L	Count				
1	L	L	Count				

Note 1 | : Transition from high to low

X : Irrelevant

Count number	QA	Qв	Qc	Q _D
0	L	L	L	Γ
. 1	Н	L	L '	٦
2	L	н	L	L
3	н	н	L	L
4	L	L	н	L
5	Н	L	н	٦
6	L	н	н	L
7	н	н	н	L
8	L	L	L	н
9	н	L	L	н
10	L	н	L	н
11	н	н	L	Н
12	L	L	Н	Н
13	н	L	н	н
14	L	Н	Н	н
15	Н	Н	Н	Н

ABSOLUTE MAXIMUM RATINGS

 $(T_a = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

Valid when $Q_{\underline{A}}$ and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
.,	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$ $-0.5 \sim +5.5$.,	
VI	Input voltage	Inputs R _{D1} , R _{D2}	-0.5~+15	7 Y	
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V	
Topr	Operating free-air ambient temperature range	·	-20~+75	ဗ	
Tstg	Storage temperature range	·	-65~+150	. ℃	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75 \, \text{C}$, unless otherwise noted)

			Unit			
Symbol	Symbol Parameter	er	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Юн	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mΑ
loL	Low-level output current	V _{OL} ≦0.5V	0		8	mA

FI FCTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

				l'ata-		Limits		11.
Symbol	Paramet	er	Test cond	itions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage	High-level input voltage			2			V .
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} = 4.75V, I _{IC} = -1	18mA			- 1.5	V
V _{OH}	High-level output voltage	High-level output voltage		V <i>μ</i> Α	2.7	3.4		٧
	Laure Laure Laure Laure		V _{CC} =4.75V	I _{OL} = 4mA(Note 2)		0.25	0.4	٧
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	IOL= 8'mA(Note 2)		0.35	0.5	V
	1.1	R _{D1} , R _{D2}	5 051/ 1/ 0 7/				20	
	I I I I I I I I I I I I I I I I I I I	$\overline{T_1}$, $\overline{T_2}$	$V_{CC}=5.25V, V_{I}=2.7$	v			40	μA
I _{IН}	High-level input current	$\overline{T_1}$, $\overline{T_2}$	V _{CC} =5.25V, V _I =5.5	V			0.2	^
		R _{D1} , R _{D2}	V _{CC} =5.25V, V _I =10V	,			0.1	mA
		R _{D1} , R _{D2}					-0.4	mA
l ₁ L	Low-level input current	T ₁	V _{CC} =5.25V, V _I =0.4	v · [-2.4	
		T ₂					-1.6	
los	Short-circuit output current (N	lote 3)	V _{CC} =5.25V, V _O = 0	V	— 20		— 100	mΑ
loc	Supply current		V _{CC} =5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: Output QA should be tested with input T2 connected to output QA.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time. Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V after 4.5V.



4-BIT BINARY COUNTER

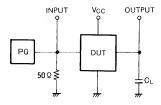
SWITCHING CHARACTERISTICS ($V_{CC}=5$ V, $T_a=25$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	Farameter	lest conditions	Min	Тур	Max	Unit
fmax	$\begin{array}{c} \text{Maximum clock frequency,} \\ \text{from input } \overline{T_1} \text{ to output } Q_A \end{array}$		32	60		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	35		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			7	16	ns
t _{PHL}	propagation time, from input $\overline{T_1}$ to output Q_A			8	18	ns
tp∟H	Low-to-high-level, high-to-low-level output			28	70	ns
t _{PHL}	propagation time, from input $\overline{\Gamma_1}$ to output Q_D			28	70	ns
t pLH	Low-to-high-level, high-to-low-level output	C _L =15pF (Note 5)		7	16	ns
t _{PHL}	propagation time, from input T ₂ to output Q _B			8	21	ns
tpLH	Low-to-high-level, high-to-low-level output			15	32	ns
tpHL	propagation time, from input $\overline{T_2}$ to output Q_C			15	35	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			22	51	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_D	·		22	51	ns
t _{PHL}	High-to-low-level output propagation time, from inputs R _{D1} , R _{D2} to outputs Q _A , Q _B , Q _C , Q _D			17	40	ns

TIMING REQUIREMENTS ($V_{CC} = 5 \text{ V}$, $T_a = 25 ^{\circ}\text{C}$, unless otherwise noted)

Cumbal	Parameter	Test conditions		Limits		Unit
Symbol	r al at leter	Test conditions	Min	Тур	Max	Unit
tw(TiH)	Clock input T ₁ high pulse width	·	15	6		ns
t _{w(T₂H)}	Clock input T ₂ high pulse width		30	15		ns
tw(AD)	Direct reset RD1, RD2 pulse width		15	5		ns
tr	Clock pulse rise time			500	100	ns
tf	Clock pulse fall time			200	100	ns
trec(RD)	Recovery time R _{D 1} , R _{D 2} to \overline{T}_1 , \overline{T}_2		25	8		ns

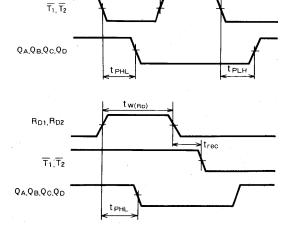
Note 5: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)

tw(=, =2H)



4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS295BP is a semiconductor integrated circuit containing a 3-state output 4-bit serial/parallel input serial/parallel output shift register function.

FEATURES

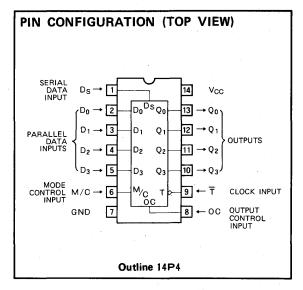
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Output control input provided
- Usable in AND-Tie connection (3-state output provided)
- Wide operating temperature range (T_a= −20~+75°C)
- High fan-out (I_{OL} = 24mA, I_{OH} = -2.6mA)

APPLICATION

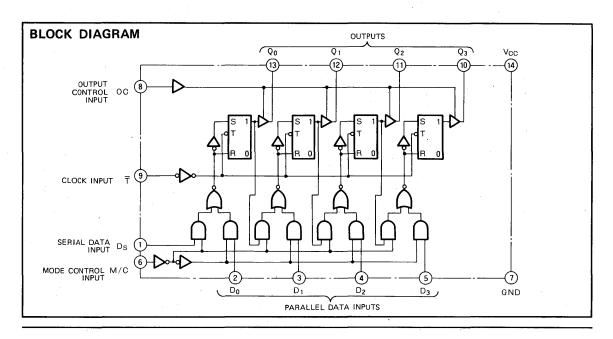
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in low, the serial data are applied to serial data input D_S and the clock pulse is applied to clock input \overline{T} , the serial data are shifted into outputs $Q_0{\sim}Q_3$ sequentially in synchronization with the clock pulse. When M/C is kept in high, the parallel data are applied to parallel data inputs $D_0{\sim}D_3$ and the 1-bit clock pulse is applied to clock input \overline{T} , the signals $D_0{\sim}D_3$ appear in $Q_0{\sim}Q_3$ respectively. When \overline{T} changes from high to low, the right shift or parallel data reading operation is performed. When M/C is kept in high,



 Q_3 is connected with D_2 , Q_2 with D_1 and Q_1 with D_0 , the serial data are applied to D_3 and the clock pulse applied to \overline{T} , the left shift operation is performed. When low is applied to output control input OC, $Q_0 \sim Q_3$ are put in the high-impedance state and AND-tie connection is enabled. Even when OC is changed, there are no effects on the shift and parallel data reading operations. When a low-level signal is applied to OC with an expansion in the bit number due to the high-impedance state and so shifting is disabled. In cases like this, the M74LS395AP with cascade output Q_3 is recommended.



4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

				Input					Out	put	
Function mode	M/C	〒			Parallel Data						
	IVI/C		Ds	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q3
Output hold	Н	Н	. X	х	×	х	×	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q3 ⁰
Parallel read	Н	1	Х	D ₀	D ₁	D ₂	D ₃	D ₀	D ₁	D ₂	D ₃
Left-shift	н	1	X	Q ₁ +	Q ₂ +	Q ₃ +	D ₃	Q1 ⁰	Q2 ⁰	Q3 ⁰	D3
Output hold	L	Н	X	Х	Х	Х	×	Q ₀ 0	Q1 ⁰	Q2 ⁰	Q ₃ 0
Right shift	L	Į.	Н	х	×	Х	×	Н	Q ₀ 0	Q ₁ 0	Q2 ⁰
rigit siiit	L	↓	L	Х	Х	X	×	L	Q ₀ 0	Q ₁ 0	Q2 ⁰

Note 1: † : transition from low to high level (negative edge trigger)

 $\mathbf{Q}^{\mathbf{Q}}$: level of \mathbf{Q} before the indicated steady-state input conditions were established

X : irrelevant

 ${\tt Q}^{\star}~:~{\tt D}_{\tt 0}$ and ${\tt Q}_{\tt 1}$, ${\tt D}_{\tt 1}$ and ${\tt Q}_{\tt 2}$, and ${\tt D}_{\tt 2}$ and ${\tt Q}_{\tt 3}$ are connected externally and serial data are applied to D3

High-impedance state when OC is low.

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	ဗ
Tstg	Storage temperature range		-65~+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75 ^{\circ}C$, unless otherwise noted)

Symbol	Paramete		Limits				
Symbol	i alamete				Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Гон	High-level output current	V _{OH} ≧2.4V	. 0		-2.6	mA	
	Low-level output current	V _{OL} ≤0.4V	0		12	mA	
loL	Low-lever output current	V _{OL} ≤0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	T	Test condotions		Limits		
Symbol	Parameter	l est con	idotions	Min	Тур *	Max	Unit
V _{IH}	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	V _{CC} =4.75V, I _{IC} =-18mA			- 1.5	V
	High-level output voltage	V _{CC} =4.75V, V _I =0.	.8V	2.4	2.1		V
V _{OH}	rigir-level output vortage	$V_1 = 2V$, $I_{OH} = -2.6$	$V_1 = 2V$, $I_{OH} = -2.6 mA$		3.1		
	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 12mA		0.25	0.4	V
VoL	Low-level output vortage	$V_{I} = 0.8V, V_{I} = 2V$	I _{OL} = 24mA		0.35	0.5	V
lozh	Off-state high-level output current	$V_{CC}=5.25V, V_1=0.$	8V, V _O =2.7V			20	μΑ
lozL	Off-state low-level output current	$V_{CC} = 5.25V, V_{I} = 0.$	8V, V _O =0.4V			-20	μА
	High-level input current	$V_{CC} = 5.25V, V_1 = 2.$	7V			20	μΑ
Iн	riigiriever input current	$V_{CC} = 5.25V, V_I = 10$	$V_{CC} = 5.25V, V_I = 10V$			0.1	mA
1 _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	V _{CC} =5.25V, V _I =0.4V		4.0	-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V		- 30		— 130	mA
Icc	Supply current	V _{CC} =5.25V (Note 3	V _{CC} =5.25V (Note 3)		20	29	mA
lccz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)			22	33	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with $D_0 \sim D_3$ at 0V, D_5 , M/C and 0C at 4.5V after \overline{T} has been set from 3V to 0V.

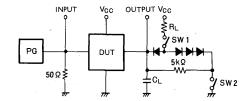
Note 4: I_{OCZ} is measured with $D_0 \sim D_3$, 0C and \overline{T} at 0V and D_S and M/C at 4.5V.

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

	Parameter	Total conditations		Unit		
Symbol		Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	O - 15-5 (Non-5)		15	20	ns
t _{PHL}	time, from input \overline{T} to outputs $Q_0 \sim Q_3$	C _L =15pF (Note 5)		18	30	ns
t _{PZH}	Output enable time to high-level	R _L =2kΩ, C _L =15pF (Note 5)		14	26	ns
tezu	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		16	30	ns
t _{PHZ}	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 5)		14	20	ns
tpLZ	Output disable time from low-level	R _L =2kΩ, C _L =5pF (Note 5)		14	20	ns

Note 5: Measurement circuit



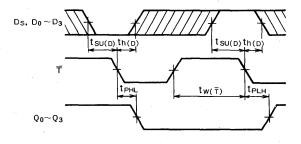
Symbol	SW1	SW2
tрzн	Open	Closed
tpzL	Closed	Open
tplz	Closed	Closed
tpHZ	Closed	Closed

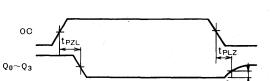
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_o = 50Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance

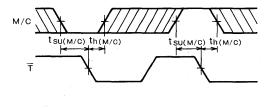
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

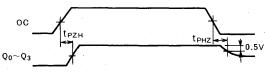
Symbol	Parameter	Test conditions		Unit		
	rarameter	Test conditions	Min	Тур	Max	Unit
tw(T)	Clock input T high pulse width		25	10		ns
tsu(D)	Setup time D to T		20	3		ns
tsu(M/C)	Setup time M/C to T		40	20		ns
th(D)	Hold time D to T		20	- 1		ns
th(M/C)	M/C hold time to T		. 0	-10		ns

TIMING DIAGRAM (Reference level = 1.3V)









Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.



QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

DESCRIPTION

The M74LS298P is a semiconductor integrated circuit which containing four 2-line to 1-line multiplexers provided with a temporary storage circuit with common selection input and clock input.

FEATURES

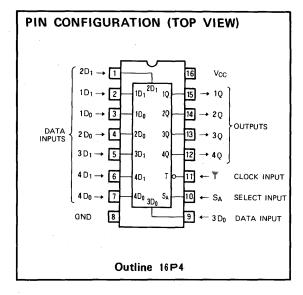
- One line data can be selected from 2-line data.
- · Equipped with D-type negative edge-triggered flip-flop.
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When the select input S_A is low, data input D_0 is selected, and when it is high, data input D_1 is selected. When the clock input \overline{T} changes from high to low, the selected data appears in the output Q. Since a D-type negative edge-triggered flip-flop is used as a temporary storage circuit, the status of Q does not change even if D is changed, whether \overline{T} is high or low.

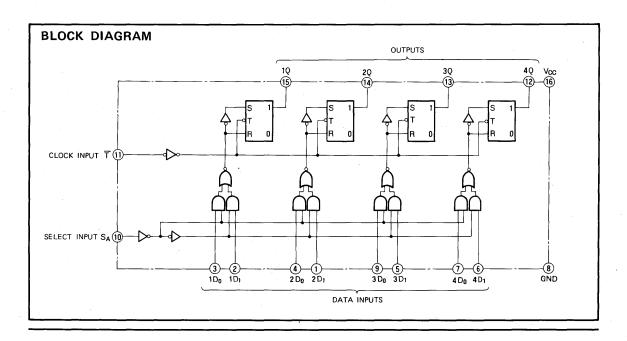


FUNCTION TABLE (Note 1)

Ŧ	SA	D ₀	D ₁	Q
Ţ	L	L	X	L
1	L	Н	X	н
1	Н	×	L	L
1	н	X	н	н

Note 1: ↓ : transition from high to low-level

X: irrelevant



QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

			Unit			
Symbol	Paramete	Parameter		Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≧2.7V	0		-400	μА
		V _{OL} ≤0.4V	0		4	mA
lo∟	Low-level output current	V ₀ L≦0.5V	. 0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

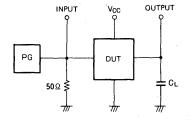
Construct	Parameter	Total	4141		Limits		Unit	
Symbol	rarameter	Test conditions		Min	Typ*	Max	Unit	
ViH	High-level input voltage			2			V	
VIL	Low-level input voltage					0.8	V	
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V	
1/.	High-level output voltage	V _{CC} =4.75V, V ₁ =0.8V		V _{CC} =4.75V, V ₁ =0.8V	2.7	3.4		
V _{OH}	High-level output voltage	V _I =2V, I _{OH} = -400,	ιA	2.7	3.4		V	
V-	Low-level output voltage	V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V	
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V	
1	Lieb level in	V _{CC} =5.25V, V _I =2.	7V			20	μА	
lін	High-level input current	V _{CC} =5.25V, V _I =10	V			0,1	mA	
IIL.	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0:4	· mA	
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	/	- 20		- 100	mA	
Icc	Supply current	V _{CC} =5.25V (Note 3)			13	21	mA	

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, runless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	i di di lietei	Test conditions	Min	Тур	Max	Unit
tpLH	Low-to-high-level, high-to-low-level output propagation	O _L =15pF		12	27	ns
tenL	time, from input \overline{T} to outputs $1Q \sim 4Q$	(Note 4)		11	32	ns

Note 4: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

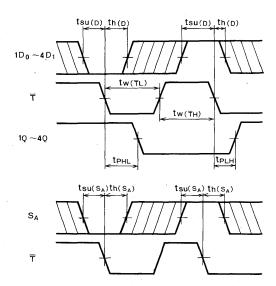
^{3:} ICC is measured with S_A , $1D_0 \sim 4D_1$ inputs grounded and a momentary 4.5V, then grounded, applied \overline{T} input.

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

· C b 1	Parameter	Test conditions		Limits			
Symbol	rarametei	Test conditions	Min	Тур	Max	Unit	
tw(₹H)	Clock input T high pulse width		20	7		ns	
tw(₹L)	Clock input Tow pulse width		20	4		ns	
tf	Clock pulse fall time		15	0		ns	
t _{SU(D)}	Setup time data input to \overline{T}		15	0		ns	
tsu(s _A)	Setup time SA to T	1	25	5		ns	
t _{h(D)}	Hold time data input to T		5	0		ns	
th(SA)	Hold time SA to T	1	0	-2		ns	

TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

174LS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

DESCRIPTION

The M74LS299P is a semiconductor integrated circuit containing an 8-bit serial/parallel input-parallel output shift register function equipped with 3-state outputs and direct reset input.

FEATURES

- Synchronous serial/parallel input-serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Direct reset input
- Wide operating temperature range ($T_a = -20 \sim +75 ^{\circ}$ C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs M/C₁ and M/C₂.

(1) Parallel read

M/C₁: High; High;

Low;

M/C₂: High

 M/C_1 : (2) Right shift M/C_1 :

 M/C_2 : Low

(3) Left shift

 M/C_2 : High

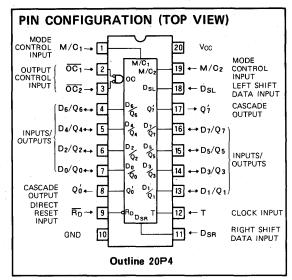
(4) Clock inhibit

 M/C_1 : M/C_2 : Low;

With parallel read, the 8-bit parallel data are applied to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$ and when the clock input T changes from low to high, the data are stored in each of the respective flip-flops.

With right shift, when the parallel data are applied to the right shift data input DSR, a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.

With left shift, when the parallel data are applied to the



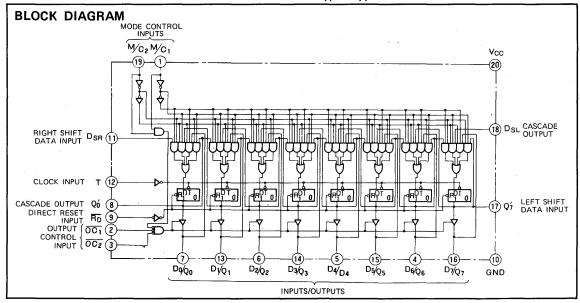
left shift data input DSL, a shift is made one bit at a time from D_7/Q_7 to D_0/Q_0 every time the clock input T changes from low to high.

With clock inhibit, the flip-flop status does not change since the clock pulses are inhibited from being applied to the flip-flop.

When one or both $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are put in the high-impedance mode "Z." The contents of the flip-flop do not change even if $\overline{OC_1}$ and $\overline{OC_2}$ are changed.

When $\overline{R_D}$ is set low, all the flip-flops are set low irrespective of the status of the other inputs.

Cascade outputs Q'0 and Q'7 are used for expansion of the respective bit numbers. Reference should be made to the typical application.



FUNCTION TABLE (Note 1)

Operational mode	RD	Т	M/C ₁	M/C ₂	DsR	D _{SL}	OC ₁	OC ₂	D ₀ /Q ₀	D1/Q1	D ₂ /Q ₂	D ₃ /Q ₃	D4/Q4	D ₅ /Q ₅	D ₆ /Q ₆	D ₇ /Q ₇	Qó	Qí
<u> </u>	L	Х	· L	х	Х	Х	L	L	L	L	Ĺ	L	L	L	L	L	L	L
Direct reset	L	×	х	L	х	х	L	L	L	L	L	L	L	L	L	L	L	L
District 1	Н	1	Н	L	L	X	L	L	L	Q ₀ ⁰	Q 1 ⁰	Q ₂ ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	L	Q ₆ 0
Right shift	Н	1	н	L	Н	х	L	L	н	Q ₀ ⁰	Q 1 ⁰	Q ₂ 0	Q ₃ ⁰	Q ₄ ⁰	Q5 ⁰	Q ₆ ⁰	Н	Q ₆ 0
1.6.15	Н	1	L	Н	×	L	L	L	Q 1 ⁰	Q ₂ 0	Q3 ⁰	Q ₄ ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰	L	Q 1 ⁰	L
Left shift	Н	1	L	Н	х	н	L	L	Q 1 ⁰	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q ₄ ⁰	Q ₆ 0	Q7 ⁰	I	Q 1 ⁰	н
Parallel read	Н	Ť	Н	н	X	×	L	L	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₇
	Н	×	L	L	х	×	L	L	Q ₀ 0	Q ₁ 0	Q ₂ 0	Q3 ⁰	Q ₄ ⁰	Q ₅ ⁰	Q ₆ 0	Q ₇ 0	Q_0^0	Q7 ⁰
Clock inhibit	Н	L	х	х	x	х	L	L	Q ₀ 0	Q 1 ⁰	Q ₂ 0	Q3 ⁰	Q ₄ ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰	Q ₀ 0	Q7 ⁰
Output inhibit	х	X.	х	X	×	×	н	L	z	z	Z	z	z	z	z	Z	Q_0^0	Q7 ⁰
(D ₀ /Q ₀ ~D ₇ /Q ₇ are put) in the high-impedance	×	×	×	х	х	×	L	н	z	z	z	z	z	z	z	z	Q ₀ 0	Q7 ⁰
state	х	Х	х	х	х	×	н	Н	Z	z	z	Z	Z	Z	z	Z	Qo ⁰	Q7 ⁰

Note 1. Qn⁰: level of Q before the indicated steady-state input conditions were established

X : Irrelevant

 \uparrow : Transition from low to high (positive edge trigger)

Dn : $D_0/Q_0 \sim D_7/Q_7$ function as inputs. Q_0' and Q_1' are set to the same status as D_0 and D_7 , respectively.

Z : High-impedance state. Status of flip-flops before $D_0/Q_0 \sim D_7/Q_7$ were put in the high-impedance mode is held.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Par	ameter	Conditions	Limits	Unit
Voc	Supply voltage			-0.5~+7	V
Vı	Input voltage			-0.5~+15	· V
	Output valence	D ₀ /Q ₀ ~D ₇ /Q ₇	Off-state	-0.5~+5.5	٧
V ₀	Output voltage	Qó, Qí	High-level state	-0.5~+V _{CC}	٧
Topr	Operating free-air ambient	t temperature range		−20~+75	°°
Tstg	Storage temperature range			-65~ + 150	℃

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol		. Parameter				14-14	
Зуппоот				Min	Тур	Max	Unit
Vcc	Supply voltage			4.75	5	5.25	V
1	High-level	$D_0/Q_0 \sim D_7/Q_7$	V _{OH} ≥2.4V	0		-2.6	mΑ
ЮН	output current	Qó, Qí	V _{OH} ≥2.7V	0		- 400	μА
		D (0 D (0	V _{OL} ≤0.4V	0		12	mA
IOL	Low-level	$D_0/Q_0 \sim D_7/Q_7$	V ₀ L≤0.5V	0		24	mA
'OL	output current	Q0, 07	V ₀ L≤0.4V	0		4	mA
		V0, V7	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol		Parameter	Test co	nditions		Limits		Unit
Symbol		i a differe	Test Co	inditions	Min	Тур 🛊	Max	Onit
ViH	High-level input volt	age		, ,	2			V
VIL	Low-level input volta	age .					0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	— 18mA			-1.5	٧
Voн	High-level	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =4.75V	I _{OH} = -2.6mA	2.4	3.1		٧
∨он	output voltage	Qố, Q7	$V_l=0.8V$, $V_l=2V$	I _{OH} = -400 μA	2.7	3.4		٧
		Dn/On~D7/O7	V 4 75V	I _{OL} =12mA		0.25	0.4	٧
	Low-level	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	V
VoL	output voltage	0/0/	V ₁ =0.8V V ₁ = 2 V	I _{OL} = 4 mA		0.25	0.4	٧
i	1	Qó, Qớ	V = 2 V	IOL= 8 mA		0.35	0.5	٧
lozh	Off-state high-level output current	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{CC} =5.25V, V _I =2	V, V ₀ =2.7V			40	μΑ
l _{ozL}	Off-state low-level output current	D ₀ /Q ₀ ~D ₇ /Q ₇	V _{OC} =5.25V, V _I =2	V, V ₀ =0.4V			400	μА
		D ₀ /Q ₀ ~D ₇ /Q ₇ , M/C ₁ , M/C ₂			· · · · ·		40	μА
		Onputs other then D ₀ /Q ₀ ~D ₇ /Q ₇ , M/C ₁ , M/C ₂	$V_{CC}=5.25V, V_{I}=2$. / V			20	μА
Iн	High-level input current	D ₀ /Q ₀ ~D ₇ /Q ₇		V ₁ =5.5V			100	μΑ
	,	M/C ₁ , M/C ₂	$V_{OO} = 5.25V$				200	μА
		Onputs other then D ₀ /Q ₀ ~ D ₇ /Q ₇ , M/C ₁ , M/C ₂		V _I =10V			100	μА
	Low-level	M/C ₁ , M/C ₂	V _{CC} =5.25V				-0.8	mA
l IL	input current	Onput other then M/C ₁ , M/C ₂	$V_1 = 0.4V$				-0.4	mA
1.	Short-circuit	D ₀ /Q ₀ ~ D ₇ /Q ₇	V _{CC} =5.25V		-30		-130	mA
los	output current	Qó, Q7	$V_0 = 0V$		-20		– 100	mA
loo	Supply current		V _{CC} =5.25V		1	33	53	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $Ta = 25^{\circ}\text{C}$, unless otherwise noted)

				Limits		Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		25	28		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0 45.50		20	33	ns
t _{PHL}	time from input T to outputs Qo, Q7	C _L =15pF (Note 4)		20	39	ns
t _{PHL}	High-to-low-level output propagation time, from input \overline{R}_D to outputs Q_0' , Q_7'	. '		18	40	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			17	25	ns
tpHL	time, from input T to inputs/outputs D ₀ /Q ₀ ~D ₇ /Q ₇	C ₁ = 45 pF (Note 4)		23	39	ns
t _{PHL}	High-to-low-level output propagation time, from inputs $\overline{R_D}$ to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$	- C_ 40p; (1000)/		20	40	ns
t _{PZH}	Output enable time to high-level	$R_L=665\Omega$, $C_L=45pF$ (Note 4)		12	21	ns
tpZL	Output enable time to low-level	$R_L=665\Omega$, $C_L=45pF$ (Note 4)		15	30	ns
t _{PHZ}	Output disable time from high-level.	$R_L=665\Omega$, $C_L=5pF$ (Note 4)		12	15	ns
t _{PLZ}	Output disable time from low-level	$R_L=665\Omega$, $C_L=5pF$ (Note 4)		12	15	ns

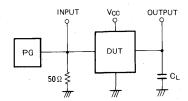
TIMING REQUIREMENTS ($V_{OC} = 5 \text{ V}$, $Ta = 25 ^{\circ}\text{C}$, unless otherwise noted)

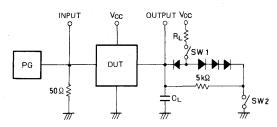
Cumbal	Parameter	Test conditions		Limits				
Symbol	raidifictor	lest conditions	Min	Тур	Max	Unit		
tw(TH)	Clock input T high pulse width		20	13		ns		
tw(TL)	Clock input T-low pulse width		20	17		ns		
tw(RDL)	Direct reset input low pulse width		20	7		ns		
tsu(M/C)	Setup time M/C ₁ , M/C ₂ to T		35	18		ns		
tsu(D)	Setup time D _{SR} , D _{SL} , $D_0/Q_0 \sim D_7/Q_7$ to T		20	10		ns		
th(M/C)	Hold time M/C ₁ , M/C ₂ to T		10	-12		ns		
th(D)	Hold time D _{SR} , D _{SL} , D ₀ /Q ₀ ~D ₇ /Q ₇ to T		· 0	- 5		ns		
trec(RD)	Recovery time Rp to T		20	15		ns		

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: Iccis measured with inputs T and OC at 4,5V.

Note 4: Measurement circuit



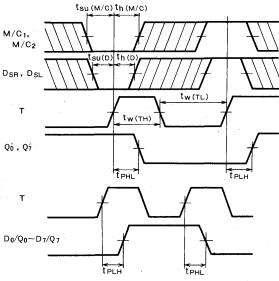


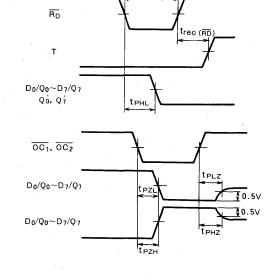
Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P =3 V_P -P, Z_O =50 Ω
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) CL includes probe and jig capacitance

tw(RDL)

TIMING DIAGRAM

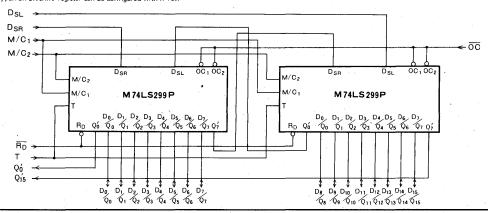




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance,

APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74LS299P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



DESCRIPTION

The M74LS323P is a semiconductor integrated circuit containing an 8-bit serial/parallel input/parallel output shift register function equipped with 3-state outputs and synchronous reset input.

FEATURES

- Synchronous serial/parallel input/serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Synchronous reset input
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs M/C_1 and M/C_2 .

(1) Parallel read

M/C₁: High; M/C₂: High

(2) Right shift

M/C₁: High; M/C₂: Low

(3) Left shift

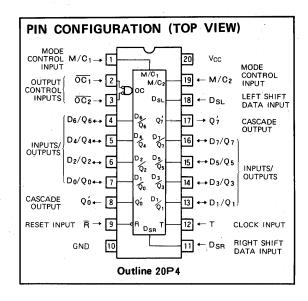
M/C₁: Low; M/C₂: High

(4) Clock inhibit

 M/C_1 : Low; M/C_2 : Low

With parallel read, the 8-bit parallel data are applied to inputs/outputs $D_0/Q_0{\sim}D_7/Q_7$ and when the clock input T changes from low to high, the data are stored in each of the respective flip-flops.

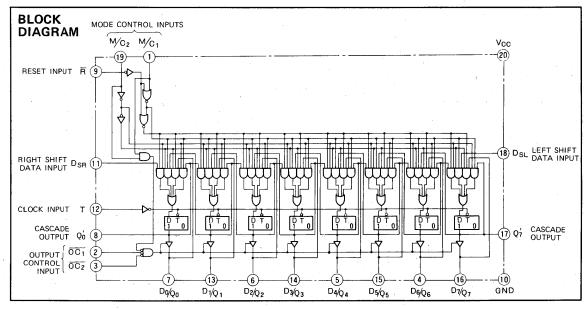
With right shift, when the parallel data are applied to the right shift data input D_{SR} , a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.



With left shift, when the parallel data are applied to the left shift data input D_{SL} , a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.

With clock inhibit, the flip-flop status does not change since the clock pulses are inhibited from being applied to the flip-flop.

When one or both $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all $D_0/Q_0 \sim D_7/Q_7$ outputs are put in the high-impedance mode "Z." The contents of the flip-flop do not change even if $\overline{OC_1}$ and $\overline{OC_2}$ are changed.



When \overline{R} is set low if \overline{T} is changed from low to high, all the flip-flops are set low.

Cascade outputs Q'0 and Q'7 are used for expansion of

the respective bit numbers. Reference should be made to the application example.

FUNCTION TABLE (Note 1)

Operational mode	R	Т	M/C ₁	M/C ₂	D _{SR}	DSL	OC ₁	OC2	D ₀ /Q ₀	D ₁ /Q ₁	D ₂ /Q ₂	D ₃ /Q ₃	D4/Q4	D ₅ /Q ₅	D ₆ /Q ₆	D7/Q7	Qά	Qí
Dt	L	1	L	х	X	Х	L	L	L	L	L	L	L	L	L	L	L	L
Reset	L	1	×	L	×	×	L	L	L	L	L	L	L	L	L	L	L	L
Right shift	Ι	1	н	٦	L	×	L	L	L	Q ₀ 0	Q 1 ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	L	Q ₆ 0
night shirt	Ι	1	Н	L	Н	х	L	L	Н	Q ₀ ⁰	Q i ⁰	Q2 ⁰	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	Н	Q ₆ ⁰
Left shift	Н	1	L	Н	х	L	L	L	Q 1 ⁰	Q ₂ ⁰	Q ₃ ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰	L	Q1 ⁰	L
Lett Sill(Ι	1	L	н	X	Н	L	L	Q 1 ⁰	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰	Q	Q 1 ⁰	Н
Parallel read	Н	1	н	Н	×	×	L	L	D ₀	Dı	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₇
Clock inhibit	Η	×	L	L	X	X	L	L	Q_0^0	Q 1 ⁰	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q ₇ 0	Q_0^0	Q7 ⁰
Glock ministr	Н	L	х	x	X	×	L	L	Q_0^0	Q 1 ⁰	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q ₇ 0	Q_0^0	Q7 ⁰
Output inhibit	X	X,	×	х	×	×	Н	L	z	Z	Z	Z	Z	Z	Z	z	Q_0^0	Q7 ⁰
(D0/Q0~D7/Q7 are put) in the high-impedance	×	×	×	×	×	X	L	H	z	z	z	Z	Z	z	Z	z	Ο ₀	Q7 ⁰
state	X	Х	Х	X	Х	×	Н	н	z	z	z	Z	Z	z	z	· Z	Q ₀ 0	Q ₇ 0

Note 1 $\,$ Qn⁰: level of Q before the indicated steady-state input conditions were established

X : Irrelevant

† : transition from low to high (positive edge trigger)

 $\text{Dn}~:~\text{D}_0/\text{Q}_0{\sim}\text{D}_7/\text{Q}_7$ were put in the high-impedance mode is held.

 $Z \hspace{0.1in} : \hspace{0.1in} \text{High-impedance state. Status of flip-flops before } \hspace{0.1in} D_0/Q_7 \sim D_7/Q_7 \hspace{0.1in} \text{were put in the high-impedance mode is held.}$

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Par	ameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
VI ·	Input voltage			-0.5~+15	V
	Output voltage	D ₀ /Q ₀ ~D ₇ /Q ₇	Off-state	-0.5~+5.5	V
V _O	Output voltage	Qó, Qí	High-level state	-0.5 ~ V _{CC}	V
Topr	Operating free-air ambie	nt temperature range		−20~+75	°C
Tstg	Storage temperature ran	ge		−65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol				11-2			
Зуппоот	1	Parameter	Min	Тур	Max	Unit	
Vcc	Supply voltage	,		4.75	5	5.25	V
IOH High-level output curren	High-level	gh-level D ₀ /Q ₀ ~D ₇ /Q ₇		0		-2.6	mA
	output current	Qá Q7	V _{0H} ≥2.7V	. 0		400	μΑ
		D (0 - D (0	V _{OL} ≤0.4V	0		12	mA
	Low-level	$D_0/Q_0 \sim D_7/Q_7$	V _{OL} ≤0.5V	0		24	mA
lor	output current	21 21	V _{OL} ≤0.4V	0		. 4	mA
		Qó. Qʻ7	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter			Tost con		Unit			
Symbol				Test con	Min	Typ *	Max	Unit	
VIH	High-level input voltage					2			V
VIL	Low-level input voltage							0.8	٧ .
Vic	Input clamp voltage			V _{CC} =4.75V, I _{IC} =-	– 18mA			-1.5	V
	High-level	D ₀ /Q ₀ ~E) ₇ /Q ₇	V _{CC} =4.75V	I _{OH} = -2.6mA	2.4	3.1		V
Voн	output voltage	Qó, Q7		$V_1 = 0.8V, V_1 = 2V$	I _{OH} = 400 μA	2.7	3.4	-	٧
,		D ₀ /O ₀ ~E)- /O-	V _{CC} =4.75V	I _O L = 12 mA		0.25	0.4	٧
1/	Low-level	D ₀ /Q ₀ ~L	לע.ער	V _I =0.8V	IoL = 24mA		0.35	0.5	٧
V _{OL}	output voltage	0' 0'		1 '	IoL = 4 mA		0.25	0.4	٧
		Qá, Qớ		V₁= 2 V	IoL = 8 mA		0.35	0.5	٧
lozh	Off-state high-level or	Off-state high-level output current D ₀ /Q ₀ ~D ₇ /Q ₇			V _{CC} =5.25V, V _I = 2 V, V _O =2.7V			40	μΑ
lozL	Off-state low-level ou	output current D ₀ /Q ₀ ~D ₇ /Q ₇		V _{CC} =5.25V, V _I =2			- 400	μΑ	
		1 Dn/On~D7/O7						40	μА
	High-level			$V_{CC}=5.25V, V_{I}=2$			20	μА	
I _{IH}					V _I =5.5V			100	μΑ
	input current	M/C ₁ , M/C ₂	/C ₂	V _{CC} =5.25V				200	μА
		Inputs othe D ₀ /Q ₀ ~D	r then 17/Q7, M/C ₁ , M/C ₂		V _I =10V			100	μА
L	Low-level	M/O ₁ , M/	′O ₂	V _{CC} =5.25V				-0.8	mA
ارر	input current	Inputs other then M/C ₁ , M/C ₂		V ₁ =0.4V				-0.4	mA
1.	Short-circuit	D ₀ /Q ₀ ~D	7/Q7	V _{CC} =5.25V		-30		— 130	mA
los	output current (Note 1)	Qá, Qź		V ₀ = 0 V		-20		-100	mA
loc	Supply current			V _{CC} =5.25V (Note 2)			33	53	mA:

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Daywasa	Test conditions	Limits			Linia
Symbol	Parameter	rest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		25	28		MHz
tpLH	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		20	33	ns
t _{PHL}	time, from input T to outputs Q0, Q7			20	39	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L = 45 pF (Note 4)		17	25	ns .
t _{PHL}	time, from input T to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$	0[-45pi (Note 4)		- 23	39	ns
tpzH	Output enable time to high-level	R _L =665Ω, C _L =45pF (Note 4)		12	21	ns
t _{PZL}	Output enable time to low-level	R _L =665Ω, C _L =45pF (Note 4)		15	30	ns
t _{PHZ}	Output disable time from high-level	$R_L=665\Omega$, $C_L=5$ pF (Note 4)		12	15	ns
t _{PLZ}	Output disable time from low-level	$R_L=665\Omega$, $C_L=5$ pF (Note 4)		12	15	ns

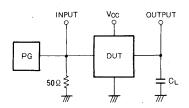
TIMING REQUIREMENTS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

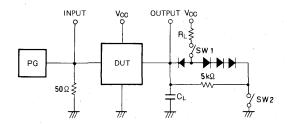
Symbol	Parameter	Test conditions				
	rarameter	rest conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		- 30	13		ns
tw(TL)	Clock input T low pulse width		30	17		ns
tsu(M/C)	Setup time M/C ₁ , M/C ₂ to T		35	18		ns
tsu(D)	Setup time DSR, DSL, D0/Q0 \sim D7/Q7 to T		20	10		ns
tsu(R)	Setup time R to T		30	23	-	ns
th(M/C)	Hold time M/C ₁ , M/C ₂ to T		10	-12		ns
th(D)	Hold time D SR, D SL, D0/Q0 \sim D7/Q7 to T		0	- 5		ns
th(R)	Recovery time R to T	1	0	- 8		ns

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with inputs T and OC at 4.5V..

Note 4: Measurement circuit

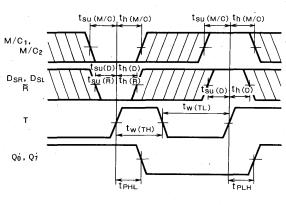


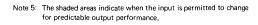


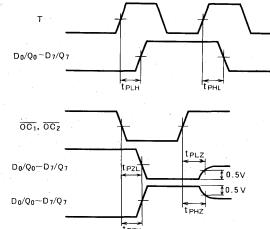
Symbol	SW 1	SW2		
t _{PZH}	Open	Closed		
t PZL	Closed	Open		
t PLZ	Closed	Closed		
t _{PHZ}	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$.
- (2) All diodes are switching diodes ($t_{rr} \leq 4ns$)
- (3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

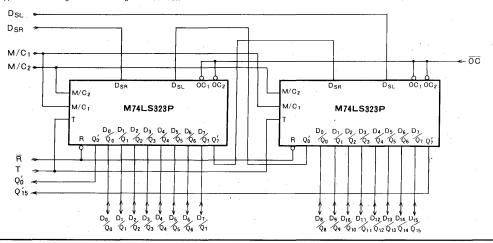






APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74LS323P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE (INVERTED)

DESCRIPTION

The M74LS352P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits.

FEATURES

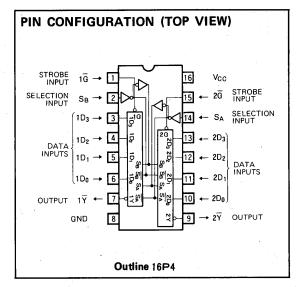
- Inverted outputs provided
- Strobe inputs provided independently for each circuit
- Selection inputs common to both circuits
- Low output impedance
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

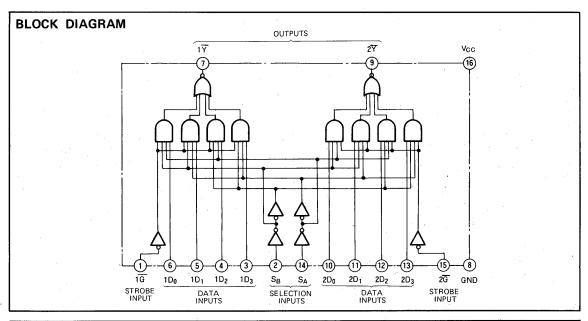
This IC has two data selector circuits which provide 1-line selection of 4 input signals and two multiplexer circuits which convert the 4-bit parallel data into serial data with time-sharing. When 4-line signals are applied to the data inputs D_0 , D_1 , D_2 and D_3 and 1 data is specified from among the data by selection inputs S_A and S_B , the input signal is output at \overline{Y} . By applying 4-bit parallel data to D_0 , D_1 , D_2 and D_3 , and connecting a synchronous divide-by-4 counter output to S_A and S_B , the D_0 , D_1 , D_2 and D_3 data appear in the order of D_0 , D_1 , D_2 and D_3 synchronized with the clock pulse. S_A and S_B are common to both circuits while strobe inputs $1\overline{G}$ and $2\overline{G}$ are independent. When $1\overline{G}$ and $2\overline{G}$ are set high, $1\overline{Y}$ and $2\overline{Y}$ are set high irrespective of the status of the input.



FUNCTION TABLE (Note 1)

SB	SA	D ₀	D ₁	D ₂	D ₃	Ğ	Ÿ
Х	Х	X	Χ	×	Х	н	Н
L	L	L	×	×	×	L	Н
L	L	I	X	×	×	L	L
L	Н	X	L	×	X	L	Н
L	н	X	Η	. X	. X	L	٦
Н	L	X	X	L.	X	L	Ι
н	L	X	X	н	Х	L	L
Н.	Н	Х	Χ	×	L	L	Ι.
Н	Н	Х	Х	Х	н	L	L

Note 1 X : Irrelevant



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits '	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		−20~+75	°C
Tstg	Storage temperature range		−65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75 ^{\circ}C$, unless otherwise noted)

C b l	D			Limits	,	Dista
Symbol	Parameter	Parameter		Тур	Max	Unit
Vcc	Supply voltage	,	4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≦0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

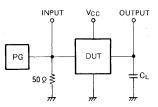
Constant	Parameter	T			Limits		11.5
Symbol	rarameter	Test condit	ions	Min	Typ ∗	Max	Unit
ViH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	, V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	8mA		-	-1.5	ı V
	High-level output voltage	V _{CC} =4.75V, V _I =0.8V	/	0.7			
VoH	Tright-level output vortage	$V_{I} = 2 V, I_{OH} = -400 \mu$	ıΑ ·	2.7	3.4		V
V	Low-level output voltage	V _{CC} =4.75V	IOL= 4 mA		0.25	0.4	V
Vol	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	V
1	High-level input current	V _{CC} =5.25V, V _i =2.7V	<i>i</i>			20	μΑ
I _{IH}	riigh-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA.
lıL	Low-level input current	V _{CC} =5.25V, V _I =0.4V	/			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 V		-20		100	mA
lcc	Supply current	V _{CC} =5.25V (Note 3)		†	6.2	10	mA

f * : All typical values are at V_{CC}=5V, T_a=25°C.

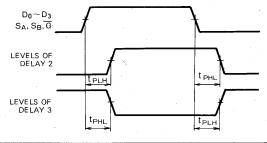
SWITCHING CHARACTERISTICS ($V_{CC}=5$ V, Ta=25°C, unless otherwise noted)

Symbol	Baramatar	Parameter Test conditions		Limits			
Symbol	r arameter	Test conditions	Min	Тур	Max	Unit	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			7	20	ns	
t _{PHL}	time, from inputs D ₀ ~ D ₃ to output			7	26	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	0. 45:5 (1): (1)		9	29	ns	
tehl	time, from inputs S_A , S_B to output \overline{Y}	C _L = 15pF (Note 4)		14	38	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	24	ns	
t _{PHL}	time, from input $\overline{\mathbf{G}}$ to output $\overline{\mathbf{Y}}$			13	32	ns	

Note 4: Measurement circuit



- The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
- (2) C_L includes probe and jig capacitance



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

M74LS353P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS353P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

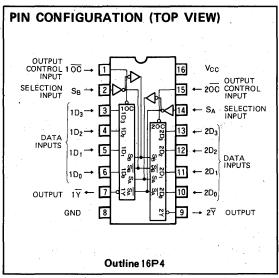
- Inverted outputs provided
- Output control inputs separate for each circuit
- Selection inputs common to both circuits
- 3-state outputs
- Wide operating temperature range $(T_a = -20^+ + 75^\circ C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signals two multiplexer circuits which convert the 4-bit parallel data into serial data by timesharing. When 4-line signals are applied to the data inputs D₀, D₁, D₂ and D₃, and 1 data is specified from among the data input by selection inputs SA and SB, the input signal is output at \overline{Y} . By applying 4-bit parallel data to data inputs D₀, D₁, D₂ and D₃ and by connecting the output of a synchronous divide-by-four counter to SA and SB, data Do, D_1 , D_2 and D_3 appear in the order of D_0 , D_1 , D_2 and D_3 , synchronized with the clock pulse. SA and SB are common to both circuits while output control inputs 100 and 200 are separate. When $1\overline{OC}$ and $2\overline{OC}$ are set high, $1\overline{Y}$ and $2\overline{Y}$ are put in the high-impedance state ("Z") irrespective of the status of the inputs.

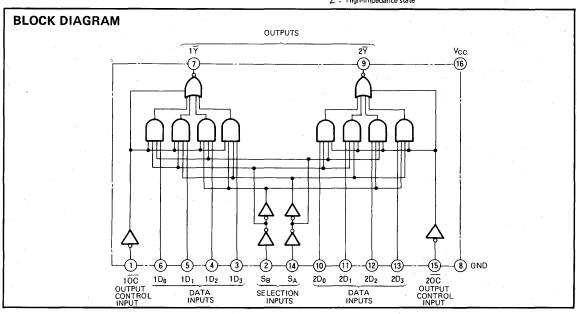


FUNCTION TABLE (Note 1)

SB	SA	D ₀	D ₁	D ₂	D ₃	оc	Y
Χ	×	×	×	×	×	н	Z
L	L	L	×	×	×	L	Н
L	L	Н	×	×	×	L	L
L	Н	Х	L	×	×	L	Н
L	н	Х	н	Х	×	L	L
Н	L	×	×	L	·×	L	Н
Н	L	Х	×	Н	×	L	L
Н	Н.	Х	×	×	L	L	н
Н -	Н	Х	×	Х	Н	L	L

Note 1 X: Irrelevant

Z: High-impedance state



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}$), unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage		· ·	-0.5~+7	V
Vı	Input voltage			-0.5~+15	V
Vo	Output voltage	Off-state		 -0.5~+5.5	V
Topr	Operating free-air ambient temperature range			 −20~+75	°C
Tstg	Storage temperature range			−65~+150	°

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Symbol Parameter			Limits	Unit	
Symbol	Faramet	21	Min	Тур	Max]
Vcc	Supply voltage		4.75	5	5.25	V
Гон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mΑ
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

Combal	Parameter	Took one die			Limits		11.2
Symbol	Parameter	Test conditions		Min	Тур 🛊	Max	Unit
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-1	I8mA			-1.5	V
VoH	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-2.6V$		2.4	3.1		٧
V _{OL}	Low-level output voltage	$V_{CC}=4.75V$ $V_{I}=0.8V, V_{I}=2V$	I _{OL} = 4 mA		0.25	0.4	V
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I = 2 V	, V ₀ =2.7V			20	μΑ
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I = 2 V	, V _O =0.4V			-20	μΑ
1	High-level input current	V _{CC} =5.25V, V ₁ =2.7	V			20	μА
Iн	riigii-ievei iriput current	V _{CC} =5.25V, V _I =10V	,			0.1	mA
liL	Low-level input current	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
İoś	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O = 0 \	/	-30		— 130	mA
ICCL	Supply current, all inputs low	V _{CC} =5.25V (Note 3)			7	12	mA
lccz	Supply current, all outputs off	V _{CC} =5.25V (Note 4)			8.5	14	mA

^{* :} All typical values are at V_{CC}= 5 V, Ta = 25 ℃

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Syllibol	Farantetel	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	25	ns
t _{PHL}	time, from inputs $D_0 \sim D_3$ to output \overline{Y}	C ₁ = 15pF (Note 5)		6	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OL 1301 (110 to 5)		14	45	ns
t _{PHL}	time, from inputs S_A , S_B to output \overline{Y}			14	32	ns
t _{PZH}	Output enable time to high-level	$R_L = 2 k\Omega$, $C_L = 15pF$ (Note 5)		14	23	ns
t _{PZL}	Output enable time to low-level	$R_L = 2 k\Omega$, $C_L = 15pF$ (Note 5)		. 15	23	ns
t _{PHZ}	Output disable time from high-level	$R_L = 2 k\Omega$, $C_L = 5 pF$ (Note 5)		14	4 1	ns
t _{PLZ}	Output disable time from low-level	$R_L = 2 k\Omega$, $C_L = 5 pF$ (Note 5)		9	27	ns

Note 2: All measurements should be done quickly and not more than one output should

be shorted at a time.

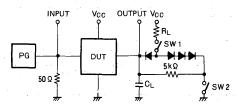
Note 3: I_{CCL} is measured with all inputs at $\underline{0V}$.

Note 4: I_{CCZ} is measured with $1\overline{OC}$ and $2\overline{OC}$ at 4.5V and all other inputs at 0V.

M74LS353P

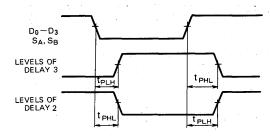
DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

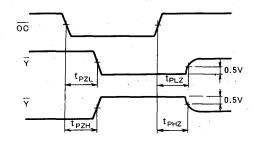
Note 5: Measurement circuit



Symbol	SW1	SW2
tрzн	Open	Closed
tezu	Closed	Open
tPLZ	Closed	Closed
tpHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r =6ns, t_f =6ns, t_w =500ns, V_P =3 $V_{P,P}$, Z_O = 50 Ω . All diodes are switching diodes.
- C_L includes probe and jig capacitance





MITSUBISHI LSTTLS M74LS365AP

HEX BUS DRIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS365AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $\overline{OC_1}$ and $\overline{OC_2}$, which are common to six circuits.

FEATURES

- Provided with output control inputs common to 6 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- High breakdown input voltage (V_I ≥ 15V)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ} C$)

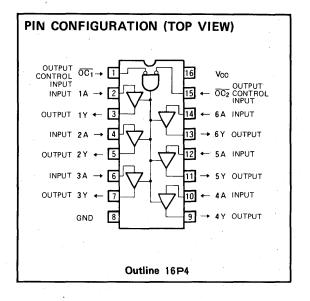
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When $\overline{OC_1}$ and $\overline{OC_2}$ are both low, high appears at the output Y if input A is high and low appears if A is low.

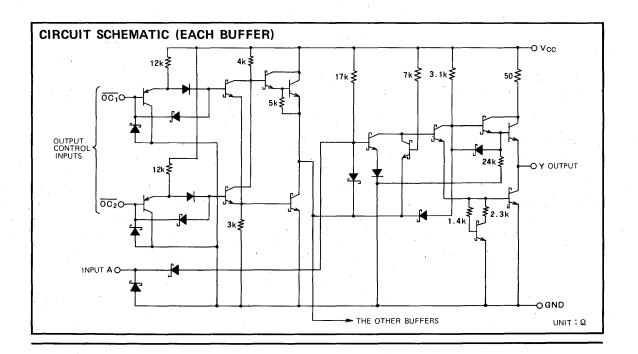
When either $\overline{OC_1}$ or $\overline{OC_2}$ or both are high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.



FUNCTION TABLE (Note 1)

OC ₁	OC ₂	Α	Y
	Ĺ	L	L
L	L	Н	Н
Н	X	Х	Z
· X	н	Х	Z

Note 1: X: irrelevant Z: high-impedance



HEX BUS DRIVER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits Unit
Vcc	Supply voltage		-0.5~+7 V
Vı	Input voltage		-0.5~+15 V
Vo -	Output voltage	Off-state	-0.5~+5.5 V
Topr	Operating free-air ambient temperature range		-20~+75 ℃
Tstg	Storage temperature range		-65~+150 ℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Unit		
Symbol			Min	Тур	Max	
Voc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{0H} ≥2.4V	0		-2.6	mA
I _{OL} Low-level output current	V _{OL} ≤0.4V	0		12	mA	
	Low-level output current	V _{OL} ≤0.5V	0		24	mΑ

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Too	t annditions		Limits		Unit	
Symbol			les	Test conditions		Typ *	Max	Omit	
ViH	High-level input voltage	4.7			2			٧	
VIL	Low-level input voltage						0.8	٧	
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC}	= - 18mA			-1.5	V	
Voн	High-level output voltage		V _{OC} =4.75V, V _I = V _I =2V, I _{OH} =-		2.4	3.1	-	٧	
.,			V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V	
VoL	Low-level output voltage		V ₁ =0.8	V _I =0.8V	I _{OL} =24mA		0.35	0.5	٧
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I (OC)=2V, V ₀ =2.4V			20	μΑ	
lozL	Off-state low-level output current	$V_{CC}=5.25V, V_1(\overline{OC})=2V, V_0=0.4V$				-20	μА		
1			V _{CC} =5.25V, V _I =	2.7V			20	μΑ	
ин	High-level input current		V _{CC} =5.25V, V _I =	= 10 V			0.1	mĄ	
		OC	V _{CC} =5.25V, V ₁ =	= 0.4V			-0.4	mA	
· 1 _H _	I IL Low-level input current A		V _{CC} =5.25V	$V_1(\overline{OC}) = 0.4V$ $V_1 = 0.4V$			-0.4	mA	
-		VGC = 5.25V	$V_1(\overline{OC}) = 2V$ $V_1 = 0.5V$			20	μΑ		
los	Short circuit output current (Note 2) V _{OC} =5.25V, V _O =0V		=0V	- 40		-225	mA		
loc	Supply current		V _{CC} =5.25V, V _I =	$\overline{OV, V_I(\overline{OC})} = 4.5V$		14	24	mA	

^{* :} All values are at $V_{CC} = 5V$, $T_a = 25$ °C

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

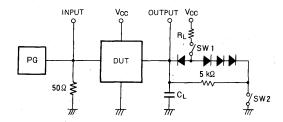
Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L =45pF		7	16	ns
t _{PHL}	propagation time, from input Ato output Y	(Note 3)		10	22	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		13	35	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	40	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		13	30	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		16	35	ns



Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

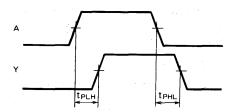
HEX BUS DRIVER WITH 3-STATE OUTPUT

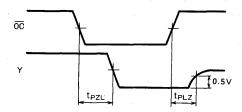
Note 3: Measurement circuit

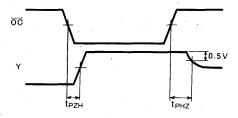


Symbol	SW 1	SW2
t PZH	Open	Closed
t PZL	Closed	Open
tpLZ	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, v_P = 3 v_P .p., z_O = 50 Ω .
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance







MITSUBISHI LSTTLS M74LS366AP

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS366AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $\overline{OC_1}$ and $\overline{OC_2}$, which are common to six circuits.

FEATURES

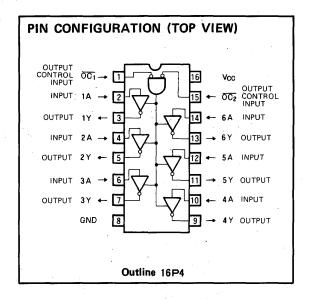
- Provided with output control inputs common to 6 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- High breakdown input voltage $(V_1 \ge 15V)$
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When OC_1 and OC_2 are both low, low appears in the output Y if input A is high and high appears if A is low. When either $\overline{OC_1}$ or $\overline{OC_2}$ both are high, all outputs Y are put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

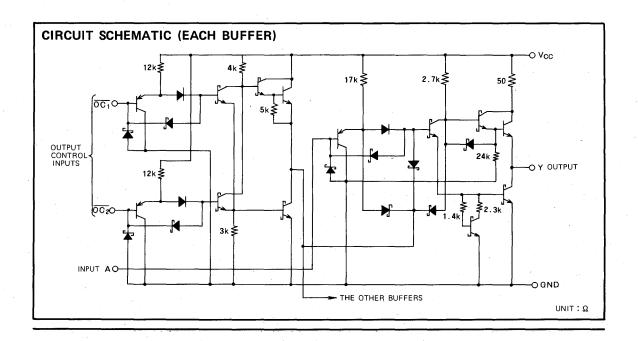


FUNCTION TABLE (Note 1)

OC1	OC2	Α	Υ
L	L	L	Τ
L	L	Н	L
Н	Х	Х	Z
Х	Н	Х	Z ·

Note 1: X: irrelevant

Z: high-impedance



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	$-0.5 \sim +5.5$	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Sumbol	Symbol Parameter			Limits				
Symbol			Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	· V		
Юн	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA		
	Low-level output current	V ₀ L ≤ 0.4V	0		12	mA		
loL		V _{OL} ≤ 0.5V	0		24	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Tout sound			Limits		
Symbol	i arametei		rest cond	Test conditions		Тур \star	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage	2	V _{CC} =4.75V, I _{IC} =-	18mA			1.5	V
Vон	High-level output voltage		V _{CC} =4.75V, V _I =0.1	8V, I _{OH} = -2.6mA	2.4	3.1		V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL			$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24 mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I (OC)	=2V, V ₀ =2.4V			20	μА
lozL	Off-state low-level output current		$V_{CC}=5.25V, V_I(\overline{OC})$	=2V, V ₀ =0.4V			-20	μΑ
1	Link In all in the second		V _{CC} =5.25V, V _I =2.7	v			20	μА
Іін	High-level input current		V _{CC} =5.25V, V _I =10V	/			0.1	mA
100		ōc	V _{CC} =5.25V, V _I =0.4	ıv.			-0.4	mA
In⊑	Low-level input current		V 5 05V	$V_l(\overline{OC}) = 0.4V$ $V_l = 0.4V$			-0.4	mA
		A	V _{CC} =5.25V	$V_{I}(\overline{OC}) = 2 V$ $V_{I} = 0.5 V$			-20	μΑ
los	Short-circuit output current (Note 2) V _{CC} =5.25V, V _O =0V		,	— 40		-225	mA	
loc	Supply current		V _{CC} =5.25V, V _I =0V	$V_{I}(\overline{OC}) = 4.5V$		12	21	mA

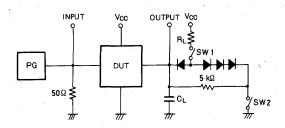
^{* :} All values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

	Parameter	Test conditions	Limits			Unit
Symbol		rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF		7	15	ns
t _{PHL}	time, from input A to output Y	(Note 3)		7	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		10	35	ns
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)		18	45	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		13	32	ns
tpLZ	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		14	14	ns .

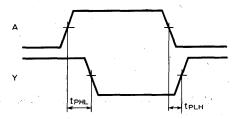
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

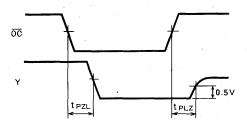
Note 3: Measurement circuit

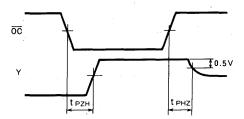


Symbol	SW1	SW2
t pzH	Open	Closed
t _{PZL}	Closed	Open
t PLZ	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω .
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.







M74LS367AP

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS367AP is a semiconductor integrated circuit constaining 6 buffers with 3-state output and is provided with output control inputs 1OC and 2OC, which are common to 4 circuits and 2 circuits, respectively.

FEATURES

- Provided with output control inputs common to 4 circuits and 2 circuits.
- High fan-out
- High breakdown input voltage
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

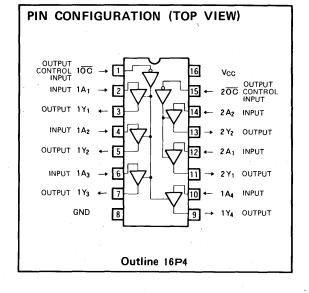
When \overline{OC} is low, high appears in the output Y if input A is high, and low appears if A is low. When \overline{OC} is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

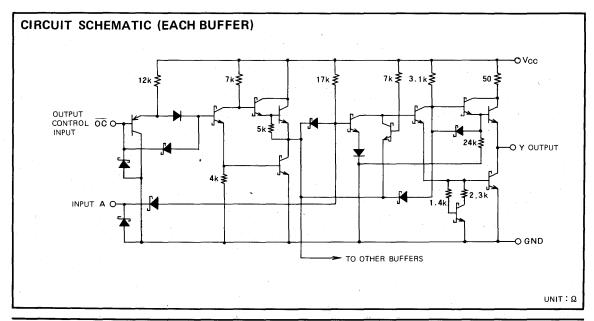
FUNCTION TABLE (Note 1)

ōc	Α	Υ
L	L	L
L	Н	Ι
Н.	X	Z

Note 1: X: irrelevant

Z: high-impedance





HEX BUS DRIVERS WITH 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
Vı	Input voltage		-0.5~+15	·V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20-+75	င
Tstg	Storage temperature range		−65∼+150	င

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Unit		
Symbol			Min	Тур	Max	Omi
V _{CC}	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mA
	Low-level output current	V _{OL} ≤0.4V	0		12	mA.
loL		V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Baramatar	Parameter		Test conditions		Limits		Unit
Зуппон	Farameter		rest conditions		Min	Тур*	Max	Onit
ViH	High-level input voltage				2			V -
VIL	Low-level input voltage					-	0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	- 18mA			-1.5	. V
VoH	High-level output voltage		$V_{CC}=4.75V, V_1=0$ $V_1=2V, I_{OH}=-2.0$		2.4	3.1		V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} = 12 mA		0.25	0.4	V
VoL			V ₁ =0.8V	I _{OL} =24 mA		0.35	0.5	V
lozн	Off-state high-level output current		V _{CC} =5.25V, V _I (00	$\bar{0})=2V, V_0=2.4V$			20	μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I (00	$\bar{0})=2V, V_0=0.4V$			-20	μА
1	Like local input accept	*	V _{CC} =5.25V, V _I =2	.7V			20	μА
ин	High-level input current		V _{CC} =5.25V, V _I =10	V			0.1	mA
		ōc	V _{CC} = 5.25V, V ₁ = 0	1.4V			-0.4	mA
T _B E	Low-level input current A		V _{CC} =5.25V	$V_1(\overline{OC}) = 0.4V$ $V_1 = 0.4V$			-0.4	mA
		V ₀₀ = 5.25V	$V_{I}(\overline{OC}) = 2V$ $V_{I} = 0.5V$			- 20	μА	
los	Short-circuit output current		V _{CC} =5.25V, V _O =0V		-40		-225	mA
Icc	Supply current		V _{CC} =5.25V, V _I =0	$V, V_1(\overline{OC}) = 4.5V$		14	24	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

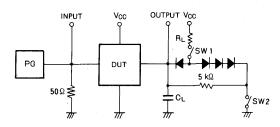
Symbol	Parameter	Test conditions	Limits			11
Symbol		rest conditions	Min	Тур	Max	Unit
t _{PLH}	Lwo-to-high-level, high-to-low-level output propagation	C _L =45pF		7	16	ns
t _{PHL}	time, from input A to output Y	(Note 3)		10	22	ns
t _{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		13	35	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		. 15	40	ns
t _{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5 pF$ (Note 3)		13	30	ns
t _{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5$ pF (Note 3)		16	35	ns

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

M74LS367AP

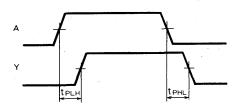
HEX BUS DRIVERS WITH 3-STATE OUTPUTS

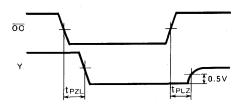
Note 3: Measurement circuit

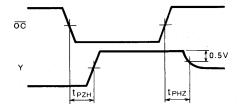


Symbol	SW1	SW2
t pzн	Open	Closed
t pzL	Closed	Open
t PLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- (2) All diodes are switching diodes (t_{rr} ≤ 4ns)
- (3) C_L includes probe and jig capacitance.







DESCRIPTION

The M74LS368AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $1\overline{OC}$ and $2\overline{OC}$, which are common to 4 circuits and 2 circuits respectively.

FEATURES

- Provided with output control inputs common to 4 circuits and 2 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = -2.6mA)
- High breakdown input voltage (V_I ≥ 15V)
- Wide operating temperature range $(T_a = -20^{\circ} +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When \overline{OC} is low, low appears in the output Y if input A is high and high appears if A is low. When \overline{OC} is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

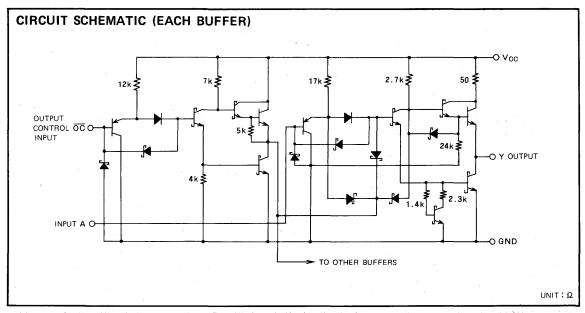
PIN CONFIGURATION (TOP VIEW) OUTPUT CONTROL 100 20C CONTROL INPUT 1A1 OUTPUT 1Y1 INPUT OUTPUT OUTPUT 1Y2 INPUT OUTPUT INPUT 1A3 INPUT OUTPUT 1Y3 GND OUTPUT Outline 16P4

FUNCTION TABLE (Note 1)

ОC	Α .	Y
L	L	Н
L	Н	L
Н	Х	Z

Note 1: X: irrelevant

Z: high-impedance



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Voc	Supply voltage		-0.5~+7	٧
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	. V
Topr	Operating free-air ambient temperature range		-20~+75 _.	°C
Tstg	Storage temperature range		. −65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Complete	Paramete	_		Limits		11-14
Symbol	raianiete		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mΑ
	Low-level output current	V _{OL} ≤0.4V	0		12	mA
IOL		V _{OL} ≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test condi	Test conditions		Limits		Unit
Symbol	rarametei	rarameter				Тур*	. Max	Onit
ViH	High-level input voltage				2			٧
VIL	Low-level input voltage		JA**				0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
VoH	High-level output voltage		V _{CC} =4.75V, V _I =0.8	SV, I _{OH} =-2.6mA	2.4	3.1		V
	Lauren autoria ratean		V _{CC} =4.75V	I _{OL} = 12 mA		0.25	0.4	٧
VoL	Low-level output voltage		V ₁ =0.8V, V ₁ =2V	I _{OL} =24mA		0.35	0.5	٧
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I (OC)	=2V, V ₀ =2.4V			20	μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I (OC)	$=2V, V_0=0.4V$		-	-20	μΑ
			V _{CC} =5.25V, V _I =2.7	V			20	μА
Іін	High-level input current	-	V _{CC} =5.25V, V _I =10\	1			0.1	mA
		<u>oc</u>	V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
- 1 L	Low-level input current . A			$V_{I}(\overline{OC}) = 0.4V$ $V_{I} = 0.4V$			-0.4	mA ·
		V _{CC} =5.25V	$V_{l}(\overline{OC}) = 2 V$ $V_{l} = 0.5 V$			-20	μА	
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _O =0V		- 40		-225	m A
loc	Supply current		V _{CC} =5.25V, V _I =0V	$V_1(\overline{OC}) = 4.5V$		12	21	mA

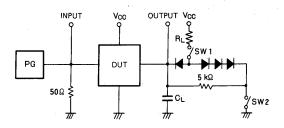
 $[\]pmb{*}$: All values are at $V_{CC}\!=\!5V,\ T_{a}\!=\!25^{\circ}\!C$, unless otherwise noted

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

0 1 1	D	Task sandisiana	Limits			11.34
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit ,
t _{PLH}	Low-to-high level, high-to-low-level output propagation	C _L =45pF		7	15	ns
t _{PHL}	time, from input A to output Y	(Note 3)		7	18	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)		16	35	ns
t _{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		18	45	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		13	32	ns -
· t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)		18	35	ns

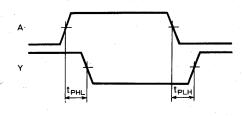
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

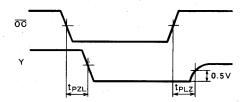
Note 3: Measurement circuit

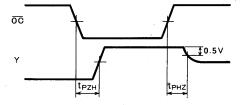


Symbol	SW 1	SW2
t PZH	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P.P}$, $Z_O = 50\Omega$. (2) All diodes are switching diodes ($t_{rr} \le 4$ ns)
- (3) C_L includes probe and jig capacitance.







OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS373P is a semiconductor integrated circuit containing 8 D-type latch circuits with 3-state output and is provided with an output controlling input and an enable input common to all circuits.

FEATURES

- 3-state, high fan-out output
- Since pnp transistor input is used in output control and enable inputs, the input load factor is small
- The enable input has high noise margin (Hysterisis = 400mV typical)
- · Package density is high with 8 circuits in one package
- Provided with output control and enable inputs which are common to all 8 circuits.
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

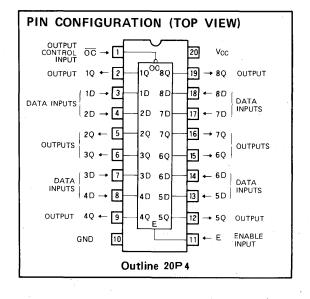
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Since the 8 D-type latches use pnp transistor input for the output control input \overline{OC} and enable input E, which are common to all 8 circuits, the input load factor is small. With a hysteretis of 400mV (typical) specially given to the input circuit E, noise margin is high.

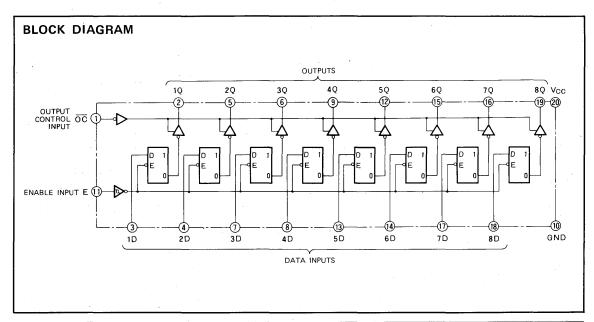
When E is high, the information from the data input D appears in the output \mathbf{Q} .

When the D signal changes, the signal that appears in Q also changes. When E changes from high to low, the status of D



immediately before the change is latched. While E is low, the status of Ω does not change even if the D is changed.

When \overline{OC} is high, 1Q-8Q are all put in the high-impedance state irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver. For application, see M74LS374P.



M74LS373P

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

	ōc	E	D	Q
ĺ	L	н	Η	H
ĺ	L	Η,	L	L
I	L	L	. х	Q ⁰
.1	н	×	Х	Z

Note 1: Q^0 : level of Q before the indicated steady-state input conditions were established

Z : high-impedance

X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol Parameter		Parameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	٧
V _I	Input voltage		-0.5~+15	٧
Vo	Output voltage	Off-state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	•	2		Limits			
Symbol	Paramete	er	Min	Тур	Max	Unit	
Voc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mΑ	
		V _{OL} ≦0.4V	0		12 .	mA	
lor	Low-level output current V ₀ L≤0.5V		0		24	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		T			Limits		Unit
Symbol	r arameter		l est condit	Test conditions		Тур*	Max	Onit
ViH	High-level input voltage				2			V
.,	Laurent innue voltege	E		,			0.75	V
V_{IL}	Low-level input voltage	D, OC					0.8	ľ
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	I8mA			-1.5	V
.,			V _{CC} =4.75V, V _I =0.8	V	2.4			٧
V _{OH}	High-level output voltage	ut voltage		V _I =2V, I _{OH} =-2.6mA	Α	2.4	3.1	
.,	Law law Law Law Law Law Law Law Law Law Law L			I _{OL} =12 mA		0.25	0.4	٧
VoL	Low-level output voltage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	٧
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =2V,	$V_0 = 2.7V$			20	μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =2V,	V ₀ = 0.4V			-20	μА
	I list I selling to a series		V _{CC} =5.25V, V _I =2.7	V		· ·	20	μΑ
Ιн	High-level input current		V _{CC} =5.25V, V _I =10V				0.1	mA
l _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4	V			-0.4	· mA
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _C =0V		-30		- 130	mA
looz	Supply current, all outputs off		V _{CC} =5.25V (Note 3)			24	40	mA

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3:} I_{CCZ} is measured with $\overline{\text{OC}}$ input at 4.5V.

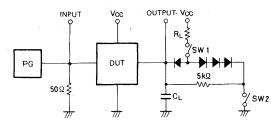
M74LS373P

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
- Jyllibol	raiameter	rest conditions	Min	Тур	Max	Onit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			9	18	ns
tpHL	time, from input 1D~8D to output 1Q~8Q	C ₁ = 45 pF (Note 4)		11	18	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	OL - 45 pr (146(6.4)		14	30	ns
t _{PHL}	time, from input E to output 1Q~8Q			13	30	ns
t _{PZH}	Output enable time to high-level	R _L =667 Ω, C _L =45 pF (Note 4)		13	28	ns
t _{PZL}	Output enable time to low-level	R _L =667 Ω, C _L =45 pF (Note 4)		14	36	ns
tpHZ	Output disable time from high-level	R _L =667 Ω, C _L = 5pF (Note 4)		16	20	ns
t _{PLZ}	Output disable time from low-level	R _L =667Ω, C _L = 5pF (Note 4),		8	25	ns

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

Note 4: Measurme Measurement circuit

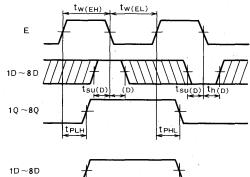


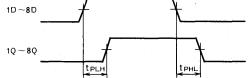
Symbol	SW 1	SW2
t _{PZH}	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

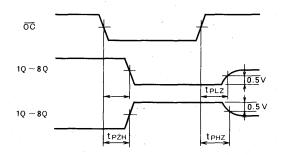
- (1) The pulse generator (PG) has the following
- PRR = 1MHz, $t_f = 6ns$, $t_f = 6ns$, $t_{W} = 500ns$, $V_P = 3V_{P,P}, Z_0 = 50\Omega$ (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$ unless otherwise noted)

, , ,		Test conditions		Limits		
Symbol	Parameter		Min	Тур	Max	Unit
tw (EH)	Enable input E high pulse width		15	11 -		ns
tw (EL)	Enable input E low pulse width		15	10		ns
tsu	Setup time 1D∼8D to E		5	-2		ns
th	Hold time 1D∼8D to E	- ·	20	7		ns







Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS374P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flipflop circuits with 3-state output, and is provided with an output control input and a clock input, which are common to all the circuits.

FEATURES

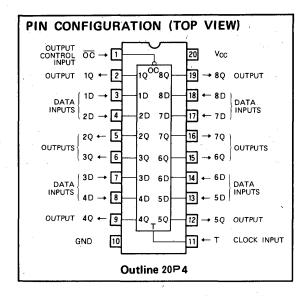
- Positive edge triggering
- 3-state, high fan-out output
- The use of pnp transistor input for the output control and clock inputs has made the input load factor small
- The clock input has high noise margin.
 (Hysterisis = 400mV typical)
- Package density is high with 8 circuits in one package
- Provided with output control and clock inputs which are common to all 8 circuits.
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

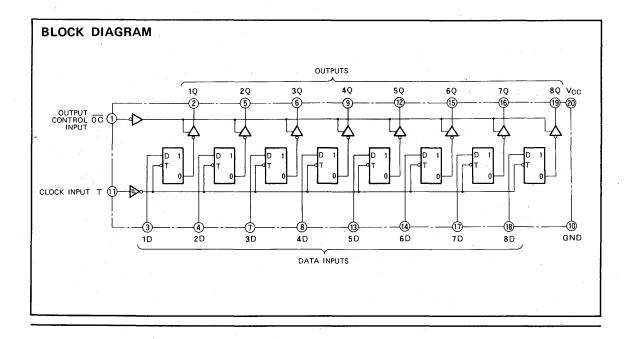
FUNCTIONAL DESCRIPTION

Since the 8 D-type ege-triggered flip-flop circuits use a pnp transistor input for the output control input \overline{OC} and clock input T, which are common to all 8 circuits, the input load factor is small. With a hysterisis of 400mV (typical) specially given to the input circuit T, noise margin is high.



When T changes from low to high, the information of data input D immediately before the change appears in the output Q in accordance with the function table.

When \overline{OC} is high, 1Q - 8Q are all put into the high-inpedance state, irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver.



M74LS374P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

	ōc	Т	D	Q
	L	1	Н	Н
i	L	1	L	· L
	L	L	Х	Q ⁰
1	Н	X	Х	Z

Note 1: \uparrow : transition from low to high level

 Q^0 : level of Q before the indicated steady-state input conditions were established

Z : high-impedance

X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5∼+7	V
Topr	Operating free-air ambient temperature range		−20 ~ + 75	°C
Tstg	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

C b				Limits			
Symbol	Parameter		Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	٧	
Іон	High-level output current	V _{OH} ≥2.4V	0		-2.6	mΑ	
	Law Israel autorit arresent	V _{OL} ≤0.4V	0		12	mΑ	
loL	Low-level output current V ₀ L≤0.5V		. 0		24	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

0		Test cone	#!#!		Limits -		Unit			
Symbol	Parameter	rest cone	aitions	Min	Тур*	Max	Unit			
ViH	High-level input voltage			2			· V			
VIL	Low-level input voltage					0.8	V			
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	٧			
	De la la casa de	V _{CC} =4.75V, V ₁ =0.	V _{CC} =4.75V, V ₁ =0.8V		3.1		.,			
V _{OH}	High-level output voltage	V _I =2V, I _{OH} =-2.6	n A	2.4	2.4 3.1	2.4 3.1	2.4 3.1	2.4 3.1		V
.,		V _{CC} = 4.75 V	I _{OL} =12mA		0.25	0.4	V			
VoL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	V			
lozh	Off-state high-level output current	V _{CC} =5.25V, V _I =2V	, V ₀ =2.7V			20	μА			
lozL	Off-state low-level output current	V _{CC} =5.25V, V _I =2V	', V ₀ =0.4V			-20	μА			
	Ulah larah lamut arranga	V _{CC} =5.25V, V _I =2.	7V			20	μΑ			
Іін	High-level input current	V _{CC} =5.25V, V _I =10V				0.1	mA			
hг	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.4	mA			
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V		-30		- 130	mA			
lccz	Supply current, all outputs off	V _{CC} =5.25V (Note 3)			27	45	mA			

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

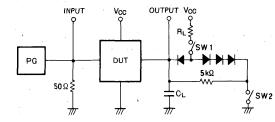
^{3:} I_{CCZ} is measured with OC input at 4.5V.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Total conditions		Unit		
Symbol		Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		35	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF (Note 4)	1 1	10	28	ns
t _{PHL}	time, from input T to output 1Q~8Q			13	28	ns
t _{PZH}	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 4)		14	28	ns
tpzL	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 4)		14	28	ns
t _{PHZ}	Output disable time from high-level	R _L =667Ω, C _L = 5pF (Note 4)		16	20	ns
t _{PLZ}	Output disable time from low-level	R _L =667Ω, C _L = 5pF (Note 4)		- 8	25	ns

Note 4: Measurement circuit

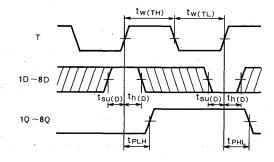


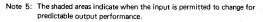
Symbol	SW 1	SW2
t PZH	Open	Closed
t PZL	Closed	Open
t _{PLZ}	Closed	Closed
t pHZ	Closed	Closed

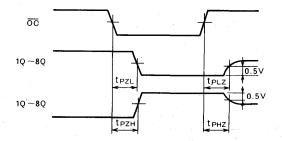
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_0 = 50Ω
- (2) All diodes are switching diodes ($t_{rr} \le 4ns$)
- (3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Total and distant	Limits			Unit
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
tw(TH)	Clock input T high pulse width		15	5		ns
t _{W(TL)}	Clock input T low pulse width	_	18	15		ns
t _{SU(D)}	Setup time 1D~8D to T		20	6		ns .
t _{h(D)}	Hold time 1D ~ 8D to T		4	1		ns





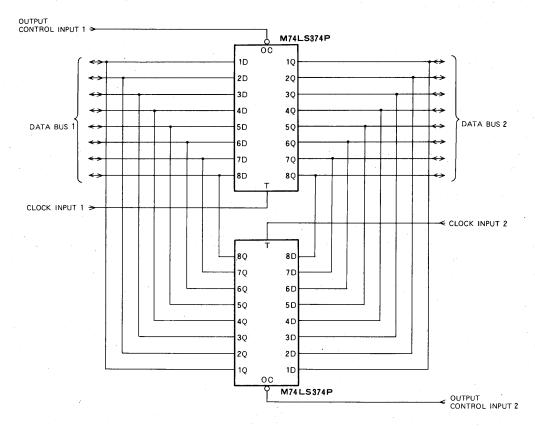


M74LS374P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

APPLICATION EXAMPLE

8-Bit shift register



MT4LS375P

4-BIT BISTABLE LATCH

DESCRIPTION

The M74LS375P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Q and \overline{Q} .

FEATURES

- Enable inputs common to two circuits each
- Q and Q outputs
- pin 8 GND, pin 16 V_{CC}
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and \overline{Q} . When the D signal changes, the signal that appears in outputs Q and \overline{Q} also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and \overline{Q} does not change even if D is changed.

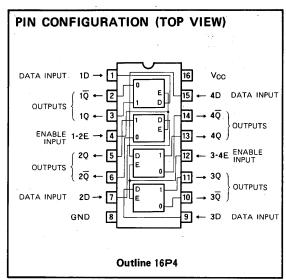
This IC has the same functions and electrical characteristics as M74LS75P and differs only in its pin configuration.

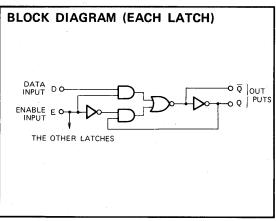
FUNCTION TABLE (Note 1)

E	D	Q	Q
Н	Н	Н	L
. н	L	L	Н
L	X	Q ⁰	Q ⁰

Note 1 $Q^0, \overline{Q^0}$: Level of Q and \overline{Q} before the indicated steady-state input conditions were established.

X: Irrelevant





ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
, Vcc	Supply voltage		-0.5∼+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	r
Tstg	Storage temperature range		-65~+150	r



4-BIT BISTABLE LATCH

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

C b.a.l	Symbol Parameter			Limits				
Symbol	rarameti	er	Min	Тур	Max	Unit		
Vcc .	Supply voltage		4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≥2.7V	0	,	-400	μА		
	Low-level output current	V _{OL} ≦0.4V	0		4	mA		
OL	Low-level output current	V _{OL} ≤0.5V	0		8	mΑ		

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

	December		Total and distant	_		Limits		Unit
Symbol	Parameter		Test condition	s .	Min	Тур 🗱	Max	·
V _I H	High-level input voltage				. 2			V
VIL	Low-level input voltage			*	,		0.8	٧
VIC	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18m	ıA			- 1.5	V
Voн	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.5		V
.,	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	٧
VoL	Low-level output vortage		$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35	0.5	V
		D	V _{CC} =5.25V				20	
		E	V _I = 2.7V				. 80	μΑ
Ηн	High-level input current	D	V _{CC} =5.25V				0.1	4
		E	V _i = 10 V				0.4	mA
		D	V _{CC} =5.25V				-0.4	
l _{IL}	Low-level input current	E	V _I = 0.4V				-1.6	mA
los	Short-circuit output current (No	te 2)	V _{CC} =5.25V, V _O = 0 V		- 20		— 100	mΑ
Icc	Supply current		V _{CC} =5.25V (Note 3)	• *		6.3	12	mA

^{* :} All typical values are at $V_{CC}=5V$, Ta=25%

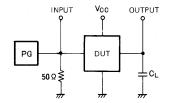
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at OV.

SWITCHING CHARACTERISTICS (Vcc=5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
Symbol	. a an eve	rest conditions	Min	Тур	Max	Unit	
tpLH	Low-to-high-level, high-to-low-level output propagation			12	27	ns	
t _{PHL}	time, from input D to output Q			8	17	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			10	20	ns	
t _{PHL}	time, from input D to output Q	0 - 15-5 (Note 4)		6	15	ns	
tplh	Low-to-high-level, high-to-low-level output propagation	C _L = 15pF (Note 4)		13	27	ns	
t _{PHL}	time, from input E to output Q			12	25	ns	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			12	30	ns	
t _{PHL}	time, from input E to output $\overline{\mathbb{Q}}$. 6	15	ns	

Note 4: Measurement circuit



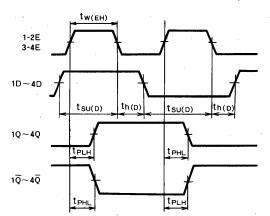
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
 - $V_P = 3V_{P.P}$, $Z_O = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

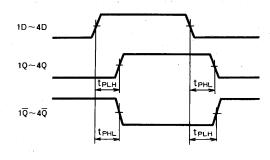
4-BIT BISTABLE LATCH

TIMING REQUIREMENTS (VCC=5V, Ta=25°C, unless otherwise noted)

Combal	De	Test conditions		Limits		Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	Onit
tw(EH)	Enable input E high pulse width		20	7		ns
tsu(D)	Setup time 1D ~ 4D to E		20	12		ns
th(D)	Hold time 1D ~ 4D to E		8	5		ns

TIMING DIAGRAM (Reference level = 1.3V)





High-level 3-4E, 1-2E

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

DESCRIPTION

The M74LS377P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common clock input and enable input.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Enable and clock inputs common to all 8 circuits
- Wide operating temperature range (T_a = −20~+75°C)

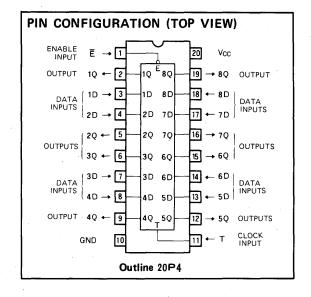
APPLICATION

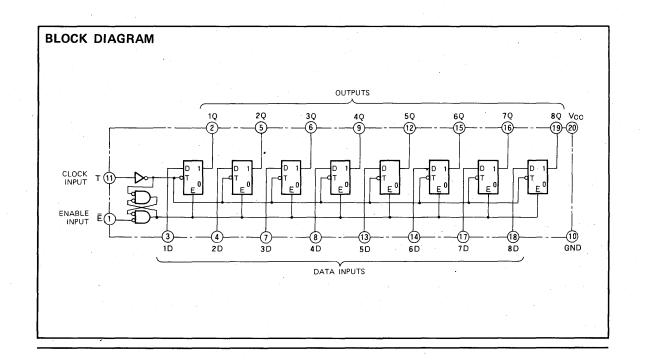
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with clock input \overline{E} common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

When \overline{E} is set high, the output status does not change irrespective of the status of the other input signals. Malfunctioning does not result even if \overline{E} is set from high to low or from low to high.





OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

FUNCTION TABLE (Note 1)

ſ	Ē	Т	. D	Q ·
Ī	Н	X	Χ.	Q ⁰
Ī	L	1	H	H
Ī	L	1	L	L
t	X		X	00

Note 1 ↑: Transition form low to high (positive edge trigger)

 $Q^{\scriptsize 0}$: Level of Q before the indicated steady-state input conditions were established.

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vi	input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	င
Tstg	Storage temperature range		-65~+150	~℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Paramet	or		Limits		Unit
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0	-	-400	μА
		V _{OL} ≤0.4V	0		4	mA
lor	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T		Limits			
Symbol	Parameter	l est cond	Test conditions		Тур 🛊	Max	Unit
ViH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
V _{OH}	High-level output voltage	$V_{OC} = 4.75V, V_1 = 0$ $V_1 = 2V, I_{OH} = -400$		2.7	3.4		٧
VoL	Low-level output voltage	$V_{CC} = 4.75V$ $V_{I} = 0.8V, V_{I} = 2V$	I _{OL} =4mA		0.25 0.35	0.4	V
		V _{OC} =5.25V, V _I =2.	7 V			. 20	μА
ΉΗ	High-level input current	V _{CC} =5.25V, V _I =10	V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0	V	20		-100	mA
ľoc	Supply current	V _{CC} =5.25V (Note 3)			17	28	mA

 $[\]boldsymbol{*}$: All typical values are at $V_{CC}\!=\!5V$, $T_a\!=\!25^{\circ}\!C$

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	T di diffetei	. rest conditions	Min	Тур	Max	Oilit
f _{max}	Maximum clock frequency		30	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =15pF (Note 4)		11	27	ns
t _{PHL}	time, from T to 1Q~8Q			11	27	ns

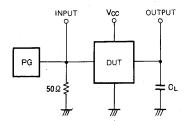


Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current is measured after 1D \sim 8D are set to 0V and T has been changed from 0V to 4.5V.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

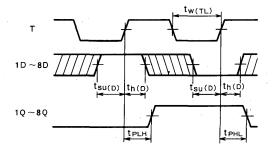
Note 4: Measurement circuit

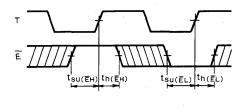


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns. V_P = $3V_{P-P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{OO}=5V$, $T_a=25^{\circ}C$, unless otherwise noted.)

Combal	Downston	Total one distinguish	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{W(TL)}	Clock input T low pulse width		20	8		ns
t _{SU(D)}	Setup time 1D~8D to T		20	6		ns
t _{SU} (ĒH)	Setup time high E to T	•	10	0		ns
t _{SU(ĒL)}	Setup time low E to T		25	. 9		ns
t _{h (D)}	Hold time 1D∼8D to T		5	- 5		ns
th(EH)	Hold time high E to T		5	- 5		ns
th (EL)	Hold time low E to T		5	1		ns





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74LS386P is a semiconductor circuit containing four integral circuits configured into dual input exclusive OR gates.

FEATURES

- Capable of withstanding high input voltages $(V_1 \ge 15V)$
- Low power dissapation (P_d = 30.5mW typical)
- High operating speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment

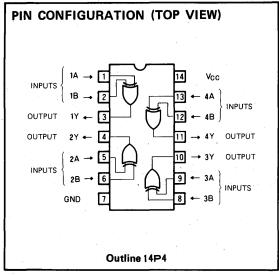
FUNCTIONAL DESCRIPTION

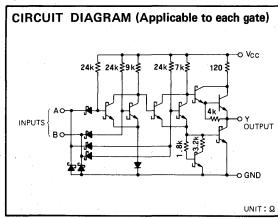
The use of Shottky TTL technology has enabled the achievement of high input voltages, high speed, low power dissipation, and high fan-out.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

Α	В	Y
L	Ļ	٦
Н	L	н
L	Н	н
Н	Н	L





ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	٧
VI	Input voltage		-0.5~+15	V
V _O	Output voltage	High-level state	-0.5~V _{CC}	V
Topr -	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65~+150	°C



QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	D			Limits		Unit
Symbol	Paran	neter	Min	Тур	Max	Unit
Vcc	Supply voltage	· · · · · · · · · · · · · · · · · · ·	4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ
	Law level output ourrant	V ₀ L≤0.4V	0		4	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

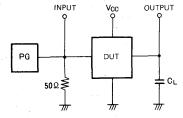
		-		Limits		
Symbol	Parameter	Test conditions	Min	Typ *	Max	Unit
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
VoH	High-level output voltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$	2.7	3.4		V
		V _{CC} =4.75V	mA	0.25	0.4	V V V
V _{OL}	Low-level output voltage	V _l =0.8V, V _l =2V	mA	0.35	0.5	V
	I Code Inc. 1	V _{CC} =5.25V, V _I =2.7V		1.	40	μА
I _{IH}	High-level input current	V _{CC} =5,25V, V _I =10V			0.2	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.8	mA
Ios	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _O =0V	-20	1	-100	mA
Icc	Supply current	V _{CC} =5.25V (Note 2)		6.1	10	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

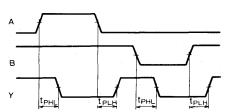
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

	Parameter	Test conditions		Unit		
Symbol	raianetei	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L =15pF, Other inputs low (Note 3)		8	23	ns
t _{PHL}	propagation time			12	17	ns
tpLH	Low-to-high-level, high-to-low-level output	0 155 Other in the high (Nature 2)		8	30	ns
t _{PHL}	propagation time	C _L =15pF, Other inputs high (Note 3)		10	22	ns

Note 3. Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_{\rm f}$ = 6ns, $t_{\rm f}$ = 6ns, $t_{\rm W}$ = 500ns, Vp = 3Vp.p, $Z_{\rm O}$ = 50 Ω .
- (2) C_L includes probe and jig capacitance.



Note 1. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{2.} I_{CC} is measured with all inputs grounded.

MITSUBISHI LSTTLs

M74LS390P

DUAL DECADE COUNTER

DESCRIPTION

The M74LS390P is a semiconductor integrated circuit containing two asynchronous decade counters with direct reset inputs

FEATURES

- High mounting density with 2 circuits equivalent to LS90 and LS290
- Direct reset inputs independent for both circuits
- Usable independently as binary and divide-by-5 counters
- High-speed counting (fmax = 80MHz typical)
- Wide operating temperature range (T_a = -20~+75°C)

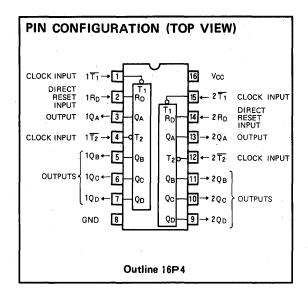
APPLICATION

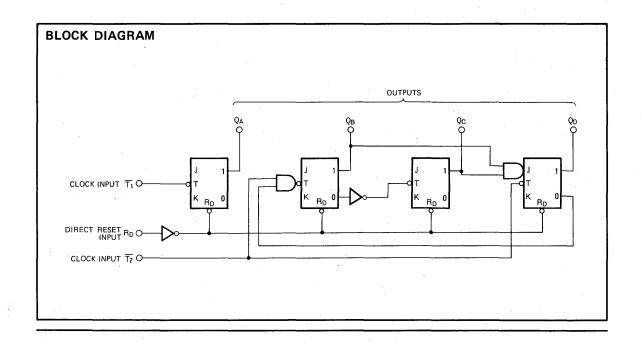
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and outputs Q_B , Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, the pure binary code output appears in the Q_A , Q_B , Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and divide-by-5 counters can be reset simultaneously by setting direct reset input R_D high. For use as a counter, R_D is set low.





DUAL DECADE COUNTER

FUNCTION TABLE (Note 1)

Ŧ	RD	QA	Qв	Qc	Q _D
Х	н .	L	L	L	L
1	L		Co		

Note 1 \downarrow : Transition from high to low (negative trigger)

X : Irrelevant

Count number	QΔ	Qв	Q _C	QD
0	L	L	L.	L
1	Н	L	L	L
2	L	Н	L	L
3	Ι	н	L	L
4	L	L '	Н	L
5	Н	L	Н	L
6	L	н	Н	L
7	Н	н	Н	L
8	L	L	L	Ħ
9	Н	L	L	Н

Valid when $\Omega_{\mbox{\scriptsize A}}$ and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	V
.,	Input voltage	Inputs T ₁ , T ₂	-0.5~+5.5	V
Vı	Input voltage	Input R _D	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V .
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		−65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	ol Parameter			Limits			
Зупьоі			Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V _{0H} ≥2.7V	0		-400	μA	
		V ₀ L≦0.4V	0		4	mA	
loL	Low-level output current	V ₀ L≦0.5V	0	-	8	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parame	***	Test cons	ditions		Limits		Unit
Symbol	Parame	Parameter Test conditions		Min	Тур*	Max	Unit	
VIH	High-level input voltage							V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	٧
VoH	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.$ $V_{I}=2V, I_{OH}=-400.$)	2.7	3.4		٧
	Low-level output voltage	I I I I I I I I I I I I I I I I I I I		V _{CC} =4.75V I _{OL} =4 mA (Note 2)		0.25	0.4	V
VoL	Low-level output voltage		$V_{I}=0.8V \cdot V_{I}=2V$	I _{OL} = 8mA (Note 2)		0.35	0.5	V
		R _D					20	
		T ₁	V _{CC} =5.25V, V _I =2.	7V [100	μ A
L	High-level input current	T ₂					200	
Iн	I figir-lever input current	RD	V _{CC} =5.25V, V _I =10	v			0.1	
		<u>T</u> 1	V _{CC} =5.25V, V _I =5.5	= \/			0.2	0.2 mA
		T ₂	VCC=5.25V, VI-5.				0.4	
		R _D				* 4.1	-0.4	
կ∟՛	Low-level input current	T ₁	V _{CC} =5.25V, V _I =0.4	1V .			1.6	, mA
	*	T ₂					-2.4	
los	Short-circuit output current	(Note 3)	V _{CC} =5.25V, V _O =0V	<i>'</i>	- 20		- 100	mA
loc	Supply current		V _{CC} =5.25V (Note 4)			15	26	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: Output Q_A should be tested with input $\overline{T_2}$ connected to output Q_A .

Note 3: All measurements should be done quickly not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_D has been set from 4.5V to 0V.

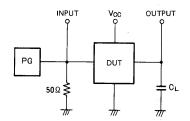


DUAL DECADE COUNTER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

0	, Daniel Control	Test conditions	Limits .			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output $\overline{Q_A}$		25	80		MHz
fmax	Maximum clock frequency, from input T ₂ to output Q _B		12.5	35		MHz
tpLH	Low-to-high-level, high-to-low-level output			8	20	ns
tenL	propagation time, from input $\overline{T_1}$ to output Q_A			8	20	ns
tp∟H	Low-to-high-level, high-to-low-level output			24	60	ns
tPHL	propagation time, from input $\overline{T_1}$ to output Q_C			24	60	ns
t _{PLH}	Low-to-high-level, high-to-low-level output	C _L =15 pF (Note 5)		10	21	ns
tpHL	propagation time, from input T2 to output QB			10	21	ns
t _{PLH}	Low-to-high-level, high-to-low-level output			17	39	ns
t _{PHL}	propagation time, from input $\overline{T_2}$ to output Q_C			17	39	ns
t _{PLH}	Low-to-high-level, high-to-low-level output		-	10	21	ns
t _{PHL}	propagation time, from input \overline{T}_2 to output Q_D			. 10	21	ns
t _{PHL}	High-to-low-level output propagation time, from input RD to outputs QA, QB, QC, QD			11	39	ns

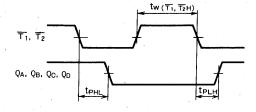
Note 5: Measurement circuit

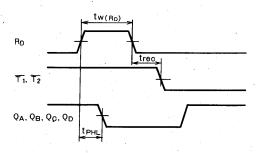


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $T_r=6ns$, $t_f=6ns$, $t_w=500ns$, $V_P=3V_{P.P}$, $Z_O=50\Omega$
- (2) C_{L_i} includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted).

Symbol	Parameter		Test conditions		Limits			
Symbol		1	rest conditions	Min	Тур	Max	Unit	
$t_{W}(\overline{T_1}H)$	Clock input T ₁ high pulse width		-	20	4		ns	
t _W (T₂ H)	Clock input T ₂ high pulse width			40	12		ns	
tw(RD)	Direct reset R _D pulse width			20	4.		ns	
tr	Clock pulse rise time				400	100	ns	
tf	Clock pulse fall time				300	100	ns	
trec(R _D)	Recovery time R _D to T ₁ , T ₂			25	8		ns	





DUAL 4-BIT BINARY COUNTERS

DESCRIPTION

The M74LS393P is a semiconductor integrated circuit containing two 4-bit binary (hexadecimal) asynchronous counter circuits with direct reset inputs

FEATURES

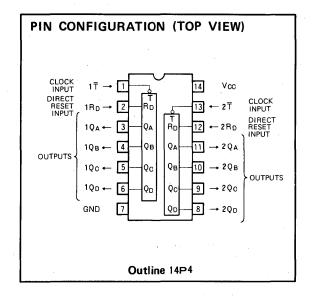
- High package density with 2 circuits equivalent to LS93 or LS293
- 2 discrete direct reset inputs
- High-speed counting (f_{max} = 75MHz typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

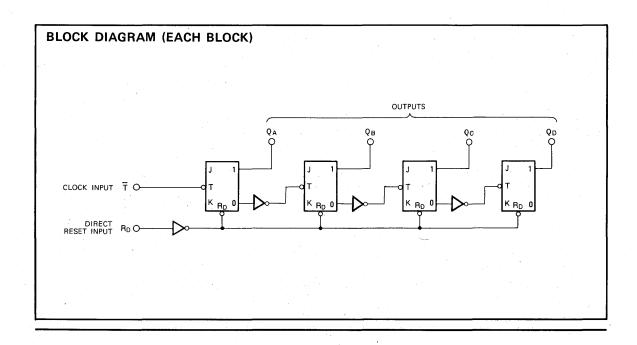
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a count pulse is fed to the clock input \overline{T} , pure binary code appear in at outputs Q_A , Q_B , Q_C , and Q_D . Counting is performed when \overline{T} changes from high to low. Reset is affected by making the direct reset input R_D high. For use as a counter, hold R_D low.





DUAL 4-BIT BINARY COUNTERS

FUNCTION TABLE (Note 1)

Г	Ŧ	ŔD	QA	Qв	Q _O	Q _D
Г	Х	н	L	L	L.	L
	1	L	Count			

Note 1: \downarrow : transition from high to low-level

X: irrelevant

Count	QA	Qв	Q _C	QD
0	L	L	L	L
. 1	н	L	L	L
. 2	L	н	L	L
3 .	, н	н	L	L
4	L	Ľ	Н	L
5	H	L.	н	L
6	L	Н	Н	L
7	Н	н	н	, L
8	L	L	L	н
9	Н	L	L	н
10	L	н	L	H
11	Н	Н	L	Н
12	L.	L	• н	Η
13	Н	L	Н	Н.
14	L	н	н	Н
15	ı	Н	Н	Н

ABSOLUTE MAXIMUM RATINGS

($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit	
Voc	Supply voltage		-0.5~+7	V	
· · · · · · · · · · · · · · · · · · ·	land along	T input	-0.5~+5.5		
VI	Input voltage	R _D input	-0.5~+15	1 '	
Vo	Output voltage	High-level state	-0.5~V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	°C	
Tstg	Storage temperature range		-65~+150	°C	

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

				11-14		
Symbol	Paramete	Min	Тур	Max	Unit	
V _{CC}	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0		-400	μА
	1	V _{OL} ≤0.4V	0		4	mA
loL	Low-level output current V _{OL} ≤0.5V		0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits		
Symbol			l est conditions	Min	Тур*	Max	Unit
VIH	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
Vон	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8V$ $V_{I} = 2V, I_{OH} = -400 \mu A$	2.7	3.4		٧
VoL	Low-level output voltage		V _{CC} =4.75V I _{OL} =4mA		0.25	0.4	٧
			$V_1 = 0.8V, V_1 = 2V$ $I_{OL} = 8 \text{ mA}$		0.35	0.5	V
	High-level input current	R _D	V _{CC} =5.25V, V _I =2.7V			20	μА
1		T				100	
ИН,		RD	V _{CC} =5.25V, V _I =10V			0.1	[™] mA
		Ŧ	V _{CC} =5.25V, V ₁ =5.5V			0.2	mA
1 _{IL}		RD	V 5 05V V 0 4V			-0.4	m A
	Low-level input current	Ŧ	$V_{CC} = 5.25V, V_{I} = 0.4V$			-1.6	
los	Short-circuit output current (Note 2)		V _{CC} =5.25V, V _C =0V	-20		- 100	mA
100	Supply current		V _{OC} =5.25V (Note 3)		15	26	m A

*: All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: I_{CC} is measured with T input grounded and a momentary 4.5V, then grounded, applied R_D input.

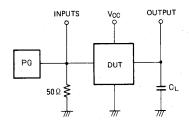


DUAL 4-BIT BINARY COUNTERS

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol		rest conditions	Min	Тур	Max	Offit
f _{max}	Maximum clock frequency		25	75		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	20	ns
t _{PHL}	time, from input \overline{T} to output Q_A	C _L =15pF (Note 4)		. 8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			36	60	ns
t _{PHL}	time, from input T to output QD			3.6	60	ns
t _{PHL}	High-to-low-level output propagation time, from input R _D to output Q _A , Q _B , Q _C , Q _D			11	39	ns

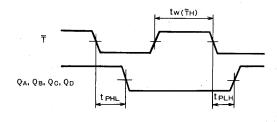
Note 4: Measurement circuit

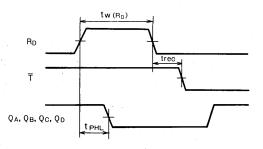


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_P , P, Q = 50 Ω
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

	_	Test conditions			Unit	
Symbol	Parameter	l est conditions	Min	Тур	Max	Oilit
tw(TH)	Clock input T high pulse width		20	4		ns
t _W (R _D)	Direct reset input R _D pulse width		20	4		ns
tr	Clock pulse rise time	·		400	100	ns
tf	Clock pulse fall time			300	100	ns .
trec(R _D)	Recovery time R _D to T		25	7		ns





MITSUBISHI LSTTLS M74LS395AP

4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS395AP is a semiconductor integrated circuit containing a 3-state output 4-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

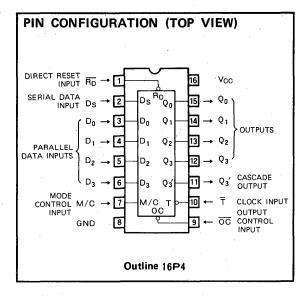
- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Output control input provided
- Q₀~Q₃ usable in AND-Tie connection (3-state output provided)
- Bit number can be expanded
- Wide operating temperature range (T_a = −20~+75°C)
- High fan-out (I_{OL} = 24mA, I_{OH} = -2.6mA)

APPLICATION

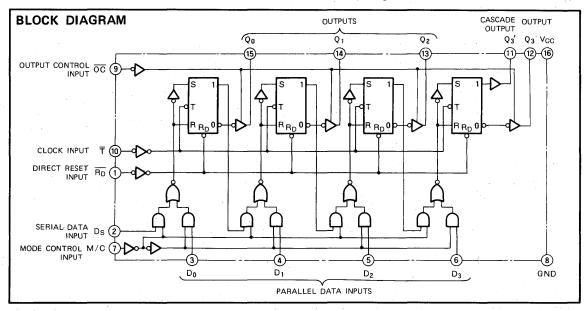
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-series/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in low, the serial data are applied to the serial data input D_S and the clock pulse is applied to the clock input \overline{T} , the serial data are shifted sequentially to outputs $Q_0{\sim}Q_3$ and $Q_3{'}$ in synchronization with the clock pulse. When M/C is kept in high, the parallel data are applied to parallel data inputs $D_0{\sim}D_3$ and the 1-bit clock pulse is applied to the \overline{T} , signals $D_0{\sim}D_3$ appear in outputs $Q_0{\sim}Q_3$ and $Q_3{'}$. When \overline{T} changes from high to low, the right shift or parallel data read operation is performed. When M/C is kept in high, Q_3 is



connected to D₂, Q₂ to D₁ and Q₁ to D₀, the serial data are applied to D₃, and the clock pulse is applied to \overline{T} , the left shift operation is performed. When a high-level state is applied to output control input \overline{OC} , $Q_0 \sim Q_3$ are put in a high-impedance state and AND-Tie connection is made possible. There will be no effect on the shift and parallel data reading operations even when \overline{OC} is changed. Cascade output Q₃' is used for bit number expansion. Even if \overline{OC} is changed in this state, there is no effect on the shifting and parallel data reading. By setting direct reset input \overline{R}_D and \overline{OC} low, $Q_0 \sim Q_3$ ' are reset low irrespective of the status of the other input signals.



4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

				In	put					· 3-state	output		Cascade output
Function mode		14/0	=			Paralle	l input						0.1
,	R_D	M/C	I	Ds	Do	D ₁	D ₂	D ₃	Qo	Q ₁	Q ₂	Q3	Q3
Direct reset	L	×	Х	×	X	×	×	X	L	L	L	L	L
Output hold	н	Н	Н	×	×	×	×	х	Q ₀ 0	Q1 ⁰	Q ₂ 0	Q3 ⁰	Q ₃ 0
Parallel output	Н	Н	1	×	D ₀	D ₁	D ₂	D ₃	Do	D ₁	D ₂	D ₃	D3
Output hold	н	L	Н	×	×	×	X	х	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q3 ⁰	Q ₃ 0
Right shift	н	L	1	↓ н	х	х	х	Х	Н	Q ₀ 0	Q1 ⁰	Q2 ⁰	Q2 ⁰
Right shift	Н	L	1	L	х	Х	X	X	L	Q ₀ 0	Q10	Q ₂ 0	Q2 ⁰

Note 1. 1: Transition from high to low (negative edge trigger)

X : Irrelevant

Q0: Level of Q before the indicated steady-state input conditions were established

Output impedance state is high when OC is high.

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Param	neter	Conditions	Limits	Unit
Vcc	Supply voltage	-		-0.5~+7	V
VI	Input voltage			-0.5~+15	V
.,	0	Q ₀ ~ Q ₃	Off-state	-0.5~+5.5	V
Vo	Output voltage	Q3'	High-level output	-0.5~V _{CC}	V
Topr	Operating free-air ambient te	mperature range	**	-20~+75	ొ
Tstg	Storage temperature range			-65~ + 150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75\%$, unless otherwise noted)

0		Parameter			Limits			
Symbol		Parameter		Min	Тур	Max	Unit	
Vcc	Supply voltage			4.75	5	5.25	٧ .	
14	IOH High-level output current	$Q_0 \sim Q_3$	V _{OH} ≥2.4V	0		-2.6	mΑ	
TOH		Q3	V _{OH} ≥2.7V	0		-400	μА	
		0.0	V _{OL} ≤ 0.4 ∨	0		12	mΑ	
	Low-level	Q ₀ ~ Q ₃	V _{OL} ≤0.5V	0		24	mΑ	
lo _L	output current	0 /	V _{OL} ≤0.4V	0		4	mΑ	
		Q3'	V _{OL} ≤ 0.5 V	0		8 .	mΑ	

$\textbf{ELECTRICAL CHARACTERISTICS} \; (\texttt{Ta} = -20 \sim +75 \, \texttt{°C}, \; \texttt{unless otherwise noted})$

Symbol	Parameter		Tank and dis			Limits		Unit
Symbol	Farameter	*	Test conditi	ons	Min	Тур	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	
Vic	Input clamp voltage		V _{CC} = 4.75V, I _{IC} = -1	8mA			-1.5	V
Voн	High-level output voltage	Q ₀ ~Q ₃	V _{CC} =4.75V, V _I =0.8V	I _{OH} = -2.6mA	2.4	3.1		V
VOH	Ingil-level output voltage	Q ₃	V _I = 2 V	$I_{OH} = -400 \mu A$	2.7	3.4		V
		00-		I _{OL} = 12mA		0.25	0.4	V
Voi	VOL Low-level output voltage	$Q_0 \sim Q_3$	V _{CC} = 4.75V	I _{OL} = 24mA	*	0.35	0.5	
VOL COW-level output vortage	Q ₃ ′	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 4 mA		0.25	0.4	V	
		Q3		IOL = 8 mA		0.35	0.5	V
lozh	Off-state high-level output current	Q ₀ ~Q ₃	V _{CC} =5.25V, V _I =2V,	V _O = 2.7 V			20	μΑ
lożL	Off-state low-level output current	Q0~Q3	V _{CC} =5.25V, V _I =2V,	V _O =0.4V			-20	μF
hн	High-level input current		V _{CC} =5.25V, V _I =2.7\	/			20	μΑ
чн	Thigh-level hipot carrent		$V_{CC} = 5.25V, V_1 = 10V$				0.1	m.A
HE.	Low-level input current		V _{CC} =5.25V, V _I =0.4\	/			-0.4	m.A
los	Short-circuit output current (Note 2)	$Q_0 \sim Q_3$	Vcc = 5.25V, Vc = 0 V		-30		- 130	m.A
פטיי	Chart subart carrent (140te 2)	Q3	VCC -3.23V, VC - UV		-20		- 100	m.A
loc	Supply current		V _{CC} = 5.25V (Note 3)			21	31	m.A
locz	Supply current, all outputs off	-	V _{CC} = 5.25V (Note 4)			22	34	m.A

All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

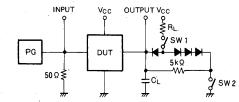
Note 3: Supply current $|_{CC}$ should be measured with \overline{RD} , D_S and M/C at 4.5V and $D_D \sim D_3$, \overline{OC} and \overline{T} at 0V. Note 4: $|_{OCZ}$ is measured with \overline{RD} , D_S , M/C and \overline{OC} at 4.5V, and $D_0 \sim D_3$ at 0V after \overline{T} has been set from 3V to 0V.

4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	rarameter	lest conditions	Min	Тур	Max	Unit
fmax	Maximum clock frequency		30	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	1		14	30	ns
t _{PHL}	time, from input \overline{T} to outputs $Q_0 \sim Q_3$, Q_3'	C _L =15pF (Note 5)		16	30	ns
tpHL	High-to-low-level output propagation time, from input $\overline{R_D}$ to output $Q_0 \sim Q_3$, Q_3'			20	35	ns
tezh	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		13	25	ns
tezL	Output enable time to low-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 5)		15	25	ns
t _{PHZ}	Output disable time from high-level	R _L =2kΩ, C _L =5pF (Note 5)		11	.17	ns
tplz	Output disable time from low-level	R _L =2kΩ, C _L =5pF (Note5)		10	20	ns

Note 5: Measurement circuit

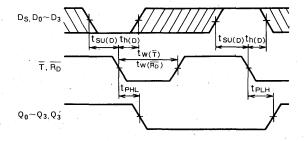


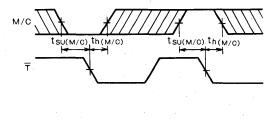
Symbol	SW1	SW2
tpzh	Open	Closed
tpzL	Closed	Open
tpLz	Closed	Closed
tpHz.	Closed	Closed

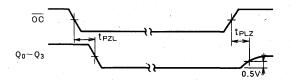
- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
- $V_P = 3V_{P.P}$, $Z_O = 50\Omega$. (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance

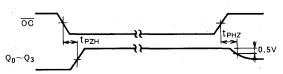
TIMING REQUIREMENTS (V_{CC}=5V, Ta = 25°C, unless otherwise noted)

0	Parameter	Test conditions	Limits			Unit
Symbol		Test conditions	Min	Тур	Max	Offic
tw(Ŧ)	Clock input T high pulse width		25	10		ns
tw(RD)	Direct reset RD pulse width		20	5		ns
tsu(D)	Setup time D to T	·	20	9 .		ns
tsu(M/C)	Setup time M/C to T	· .	40	16		ns
t _{h(D)}	Hold time D to T	}	10	-1		ns
th(M/C)	M/C hold time to T		10	-12		ns









Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

NEW PRODUCT

MT4LS423P

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

DESCRIPTION

The M74LS423P is a semiconductor integrated circuit containing two retriggerable monostable multivibrator circuits with direct reset inputs.

FEATURES

- Long pulse widths can be generated using the retriggerable function
- Output pulses can be stopped at any time with direct reset inputs
- A, B complementary inputs provided
- Direct reset pulses with no one-shot operation.
- High input breakdown voltage (V₁ ≥ 15V)
- Q and Q outputs
- Wide operating temperature range (T_a=-20~+75°C)

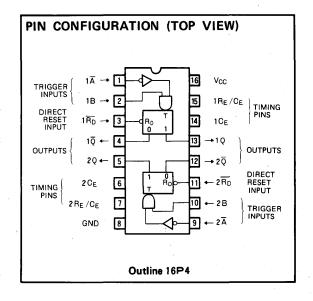
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Positive pulses appear in output Q and negative pulses in output \overline{Q} by connecting external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E , as shown in Fig. 1 on the next page, and by applying a trigger from input \overline{A} or B. (Fig. 2(a)) The width tw of the pulses appearing in the outputs is set by R_T and C_T . When \overline{A} changes from high to low or when B changes from low to high, the trigger is applied.

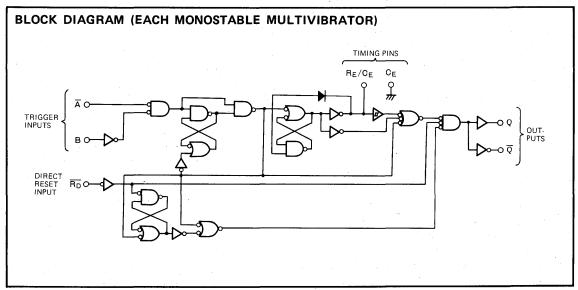
The retriggerable function is used to obtain long output pulse widths and when the trigger is applied from \overline{A} or B immediately before the output pulse is completed, the



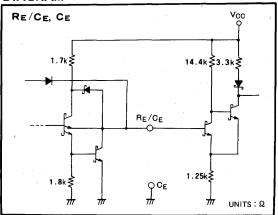
output pulse width can be extended. (Fig. 2(b))

Q can be reset immediately low and \overline{Q} high by setting direct reset input \overline{R}_D low irrespective of the status of the outputs. The output pulse width can therefore be made as short as preferred by the \overline{R}_D signal. (Fig. 2(c))

The above functions are the same as for the M74LS123P. However, when \overline{R}_D changes from low to high with \overline{A} at low and B at high for the M74LS123P, the trigger is applied and one-shot operation takes place, whereas with the M74LS423P one-shot operation does not take place for the same change in \overline{R}_D .



TIMING TERMINAL EQUIVALENT CIRCUIT DIAGRAM



FUNCTION TABLE (Note 1)

R _D	Ā	В	Q	lo
L	X	X	L.	н
Х	н	Х	L	н
Х	X.	L.	L	н
Н	L	1	77.	7.5
Н	↓ ·	н	5	5

Note 1 . \uparrow : Transition from low to high. (positive edge triggering)

1 : Transition from high to low. (negative edge triggering)

☐: Positive one-shot operation.

☐: Negative one-shot operation.

X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and capacitor C_T are connected to timing pins R_E/C_E and C_E . Connect the positive to the R_E/C_E side and the negative to the C_E side when using C_T with polarity. In this case, it is not necessary to connect a switching diode required with the same type of TTL IC. With malfunctions caused by noise, connect C_E to the GND line (neighboring on pin 8) as shown by the dotted line in Fig. 1.

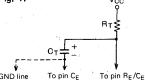


Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

2. Output pulse width tw

The output pulse width t_w is set by R_T and C_T

2-1. When CT is greater than 1000pF

$$t_W = K \cdot R_T \cdot C_T \text{ (ns)} \times (1+0.1)$$

Depending on the product, fluctuations of about $\pm 10\%$ may arise.

Refer to K- C_T characteristics indicated in TYPICAL CHARACTERISTICS for value of K. (No change is brought to K by value of R_T .)

 R_{T} is measured in kilohms and C_{T} in picofarads Depending on the product, fluctuations in the order of 3/-10%may occur.

R_T is measured in kilohms and C_T in picofarads

2-2. When CT is equal to or less than 1000pF

Refer to the output pulse width versus—C_T, R_T given in the typical characteristics.

3. Output pulse width control

The output pulse width can be controlled in 3 ways by using, or not using, the trigger signal and \overline{R}_D signal.

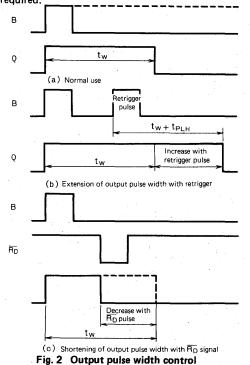
3-1. Normal use

This is the normal method of use as a regular monostable multivibrator such as that shown in Fig. 2(a) and the output pulse width t_w can be set as for the formula and figure in section 2 above.

3-2. Extension of output pulse width with retrigger func-

As shown in Fig. 2(b), the output pulse width can be extended as desired by applying a trigger pulse before the output pulse is completed.

3-3. Shortening of the output pulse width with $\overline{R_D}$ signal As shown in Fig. 2(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.



4. Precautions with use

- 4-1. Apply the retrigger pulse after a wait of 0.22C_T (ns) upon application of the trigger pulse. C_T is measured in picofarads. The retrigger pulse during this period is ineffective.
- 4-2. In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible (less than 3cm) and avoid signal wires which may be conducive to noise.
- 4-3. Connect an external capacitor of 0.01~0.1μF with good high-frequency characteristics between pins V_{CC} and GND.
- 4-4. The output pulse is generated when the power is switched on.

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level stage	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

Symbol	Paramete				Unit	
Symbol	ratamet	er .	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Іон	High-level output current	V _{OH} ≥2.7V	0	-	400	μА
	Low-level output current	V _{OL} ≤0.4V	0		4	mA
lor	V _{OL} ≤0.5V		0		8	mA
R _T	External timing resistance	<u> </u>	5		260	kΩ
Ст	External timing capacitance	None			_	
CR	RE/CE pin wiring capacitance	capacitance 50			pF	

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75℃, unless otherwise noted)

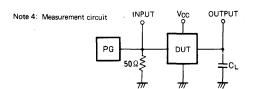
Symbol	Parameter	Test on	nditions		Limits		11-14
Зупцоі	raidilleter	lest co	nutions	Min	Typ *	Max	Unit
V _{IH}	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC} =	18mA			-1.5	V
VoH	High-level output voltage	V _{CC} =4.75V, V _I =0	.8V	2.7	3.5		v
VOH.	Ingili level output voltage	V _I =2V, I _{OH} =-40	0μΑ	2.1	3.5		
V _{OL}	Low-level output voltage	V _{CC} =4.75V	I _{OL} = 4 mA		0.25	0.4	V
VOL	Low-level output voltage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} = 8 mA		0.35	0.5	٧
Iн	High-level input current	V _{CC} =5.25V, V _I =2	2.7V			20	μΑ
чн	riigh-level input current	V _{CC} =5.25V, V _I =1	0 ∨			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I =0	1.4V			-0.4	mΑ
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =	0∨	- 20		— 100	mΑ
Icc	Supply current	V _{CC} =5.25V (Note 3	3)		12	20	mΑ

^{* :} All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time. Note 3: I_{CC} is measured with R_E/C_E and C_E open, 4.5V applied to $\overline{R_D}$, \overline{A} and B and \overline{A} set from 0V momentarily to 4.5V.

SWITCHING CHARACTERISTICS ($V_{QQ} = 5 \text{ V}$, $T_a = 25^{\circ}\text{C}$, unless otherwise noted)

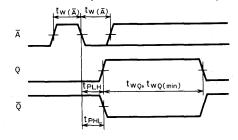
Counched	Downston	Took and distant	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level output propagation time, from input \$\overline{A}\$ to output \$\overline{Q}\$				33	ns
t _{PLH}	Low-to-high-level output propagation time, from input B to output Q	1			44	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{\mathbf{A}}$ to output $\overline{\mathbf{Q}}$	C _T = 0 pF			45	ns
t _{PHL}	High-to-low-level output propagation time, from input B to output $\overline{\mathbb{Q}}$	R _T = 5 kΩ			56	ns
t _{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q	C _L =15pF (Note 4)			27	ns
t _{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output \overline{Q}	1			45	ns
twQ (min)	Minimum output pulse width, from inputs A , B to output Q	1 !			200	ns
t _{WQ}	Output pulse width, from inputs $\overline{\mathbf{A}}$. $\overline{\mathbf{B}}$ to output \mathbf{Q}	$C_T=1000 pF$, $R_T=10 k\Omega$ $C_L=15 pF$ (Note 4)	4		5	μs

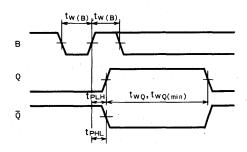


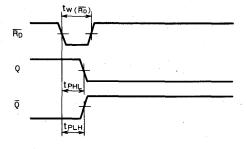
- (1) The pulse generator (PG) has the following characteristics:
- PRR=1MHz (100kHz with t_{WQ} measurement), t_r =6ns, t_f =6ns, $t_w \ge 40$ ns, V_P =3 $V_{P,P}$, Z_O =50 Ω .
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC} = 5 \text{ V}$. $T_a = 25^{\circ}\text{C}$. unless otherwise noted)

Symbol	Parameter	Parameter Test conditions		Limits		
Symbol	rarameter	lest conditions	Min	Тур .	Max	Unit
tw(A)	Trigger input A pulse width		40			ns
t _{W(B)}	Trigger input B pulse width		40			ns
tw (Ro)	Direct reset input pulse width RD		40			ns

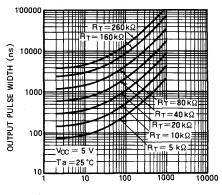






TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH VS C_T, R_T (C_T≤1000pF)

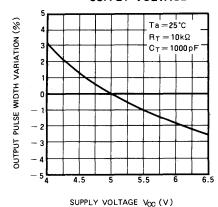


EXTERNAL CAPACITANCE CT (pF)

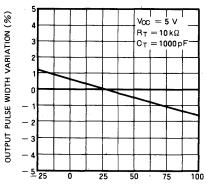
Note 5: The error of the output pulse width in the above graph is within ±20%.

EXTERNAL CAPACITANCE CT (pF)

OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



AMBIENT TEMPERATURE Ta (°C)

MITSUBISHI LSTTLS

M74LS490P

DUAL 4-BIT DECADE COUNTER

DESCRIPTION

The M74LS490P is a semiconductor integrated circuit containing a dual circuit asynchronous decade counter with direct reset input and direct 9-set input.

FEATURES

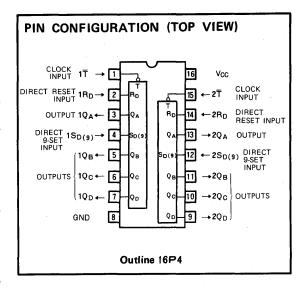
- Two integral circuits (the functional equivalent of LS90 and LS290) provide high mounting density capability
- Individual clock, direct clear, and set-to-9 inputs for each decade counter
- High-speed counting (f_{max} = 35MHz typical)
- Wide operating temperature range $(T_a = -20 \sim +75^{\circ}C)$

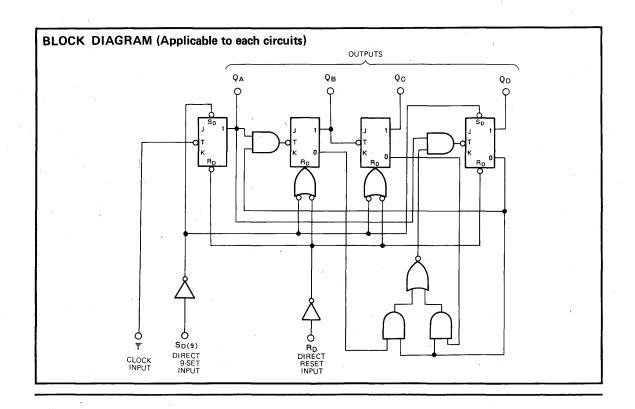
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions to produce binary-coded decimal output at Q_A , Q_B , Q_C , and Q_D in response to count pulse input at clock input \overline{T} . Counting occurs when \overline{T} transits from high to low-level. A high-level status at direct reset input R_D or direct 9-set input $S_{D(9)}$ initiates reset or a setting to 9 respectively. When operated as a counter, R_D and $S_{D(9)}$ are set low-level.







DUAL 4-BIT DECADE COUNTER

FUNCTION TABLE (Note 1)

1	Ŧ	RD	S _{D(9)}	QA	Qв	Q _C	QD		
	X	H	L	L ·	L	L	L		
	Х	L	- , Н	Н	L	L	Ι		
1	↓	L	L	Count					

Note 1. 👃 : Transition from high to low

(negative edge trigger)

X : Irrelevant

Count	Q_{A}	QB	Qc	Q _D
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	Н	H	L	L
4	·L	L ·	н	L
5	н	L	н	L
6	L	Н	н	L
7	н	н	н	L
8	L	L	L	н
9	Н	L	L	Н

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	, Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
	INPUT T		-0.5~+5.5	V
Vı	Input voltage	INPUT RD, SD(9)	-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter			Limits			
Symbol	Parame	ster	Min	Тур	Max	Unit	
V _{CC}	Supply voltage		4.75	5	5.25	٧.	
Гон	High-level output current	V _{OH} ≧2.7V	0		-400	μΑ	
		V _{OL} ≤0.4V	0 ,		4	mA	
lor	Low-level output current	V _{OL} ≦0.5V	. 0		8	mA	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter		The anadiate		Limits			:
Symbol	Param	raiametei		Test conditions		Тур 🗱	Max	Unit
ViH	High-level input voltage							V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage	,	V _{CC} =4.75V, I _{IC} =-18	mA			-1.5	V
V _{OH}	High-level output voltage		$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400 \mu A$		2.7	3.4		٧
	Low-level output voltage		V _{CC} =4.75V	I _{OL} =4mA		0.25	0.4	V
VoL			V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	V
1		R _D , S _{D(9)}	V -5 05V V 0 7V				20	
	Lish level is a second	Ŧ	$V_{CC}=5.25V, V_1=2.7V$				100	μΑ
Тін.	High-level input current	R _D , S _{D (9)}	V _{CC} =5.25V, V _I =10V			,	0.1	mΑ
		Ŧ	V _{CC} =5.25V, V _I =5.5V				0.2	mA
	Law lavel innut average	R _D , S _D (9)	V 5 05 V V 0 4 V				-0.4	^
lic.	Low-level input current	Ŧ	$V_{CC}=5.25V, V_{I}=0.4V$				-1.6	mA
los	Short-circuit output current	Note 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
lcc	Supply current		V _{CC} =5.25V (Note 3)			15	26	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

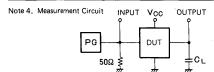
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

^{3.} Icc is measured with all outputs open, both Ro and Spig) inputs grounded following momentary connection to 4.5V; all other inputs grounded.

DUAL 4-BIT DECADE COUNTER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

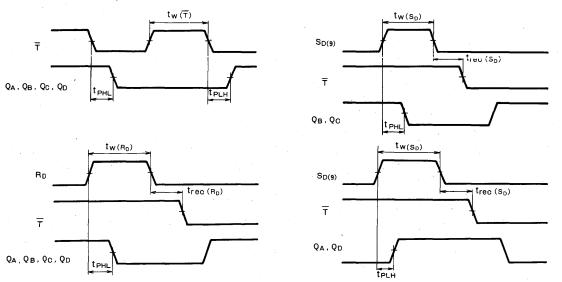
	D	Test conditions		Limits		Unit
Symbol	Parameter	rest conditions	Min	Тур	Max	
fmax	Maximum clock frequency (from input \overline{T} to output Q_A)		25	35		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			8	20	ns
t _{PHL}	time, from input \overline{T} to output Q_{A}	· ·		8	20	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			20	39	ns
t _{PHL}	time, from input \overline{T} to outputs Q_B , Q_D			22	39	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	C ₁ = 15pF (Note 4)		30	54	ns
t _{PHL}	time, from input \overline{T} to output Q_C			30	54	ns
t _{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A , Q_B , Q_C , Q_D			11	39	ns
t _{PLH}	Low-to-high-level output propagation time, from input $S_{D(9)}$ to outputs Q_A , Q_D			11	39	ns
t _{PHL}	High-to-low-level output propagation time, from input Sp(g) to outputs QB, QC			12	36	ns



- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
 C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	•	Total	Limits			Unia
	Parameter	Test conditions	Min	Тур	Max	Unit
tw(Ŧ)	Clock input T pulse width		20	5		ns
tw(RD)	Direct reset R _D pulse width		20	4		ns
tw(sD)	Direct 9-set S _{D(9)} pulse width	·	20	4		ns
tr	Clock pulse rise time			400	100	ns
tf	Clock pulse fall time			300	100	ns
trec (Ro)	R_D recovery time to \overline{T}		25	8		ns
trec (Sp)	S _{D(9)} recovery time to T		25	. 8		ns





OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS540P is a semiconductor integrated circuit containing 1 block of buffer with 3-state inverted output and common output control input for all 8 discrete circuits.

FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage (V₁≥5V)
- Output control inputs provided (OC₁, OC₂)
- High fan-out, 3-state output
 (I_{OL} = 24mA, I_{OH} = -15mA)
- Data flow-thru pin out
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

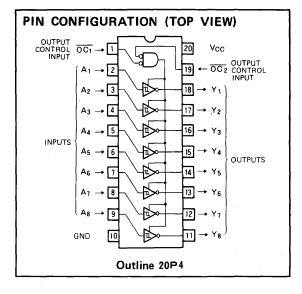
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuits has enabled the achievement of small input load factor and input high break-down voltage. With hysteresis characteristics, the buffer has a 3-state inverted output with high noise margin. When output control inputs \overline{OC}_1 and \overline{OC}_2 are low, a high-level signal appears at output Y if input A is low and a low-level signal appears if it is high.

All outputs are set to the high-impedance state regardless of the status of A when $\overline{OC_1}$ and $\overline{OC_2}$ are in any other state,

The input and output pins are arranged for facilitated



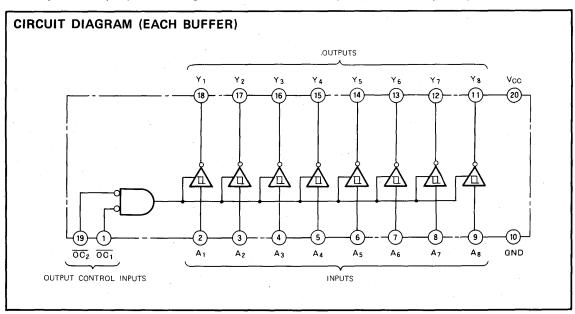
FUNCTION TABLE (Note 1)

Α	CC ₁	OC2	Y
L	L	. L	Ι
Н	L	L	Ļ
X	L	Н	Z
Х	Н	L	Z
X	н	н	Z

Note 1: Z: high-impedance

X: irrelevant

board layout (data flow-thru pin out).



OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

				Limits		Unit V mA
Symbol	mbol Parameter		Parameter Min Typ		Max]
Vcc	Supply voltage		4.75	5	5.25	V
		V _{0H} ≥2.4V	0		-3	mA
Іон	High-level output current	V _{OH} ≥ 2 V	0		- 15	mA
		V _{0L} ≤0.4V	0		12	mA
IOL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75^{\circ}C$, unless otherwise noted)

Combal	B	Total conditions	L	Limits		Unit V V V V V V V AAAAAAAAAAAAAAAAAAAAAA
Symbol	Parameter	Test conditions	Min	Typ*	Max	Onit
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	٧
V_{T} , $-V_{T}$	Hysteresis	V _{CC} =4.75V	0.2	0.4		V
VIC	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	. V
	$V_{CC} = 4.75V$ $V_{I} = 0.8V$, $I_{OH} = -3$ mA		mA 2.4	3.4		V
VoH	High-level output voltage	$V_1 = 2V$ $V_1 = 0.5V$, $I_{OH} = -1$	5mA 2			V
	Low-level output voltage	V _{CC} =4.75V I _{OL} =12r	nΑ	0.25	0.4	V
V _{OL} Low-level output voltage	Low-level output voltage	V _I =0.8V, V _I =2V I _{OL} =24r	nΑ	0.35	0.5	V
lozн	Off-state high-level output current	V _{CC} =5.25V, V _I =2V, V _O =2.7V			20	μА
lozL	Off-state low-level output current	V _{CC} =5.25V, V ₁ =2V, V ₀ =0.4V			20	μА
1	High-level input current	V _{CC} =5:25V, V _I =2.7V			20	μА
Ιн	High-lever input current	V _{CC} =5.25V, V _I =10V			0.1	mA
lı_	Low-level input current	V _{CC} =5.25V, V _I =0.4V			-0.2	mA
los	Short-circuit output current (Note 2)	V _{CC} =5.25V, V _O =0V	-40		-225	mA
Гссн	Supply current, all outputs high	V _{CC} =5.25V, V _I =0V		13	25	mA
CCL	Supply current, all outputs low	$V_{CC} = 5.25V, V_l = 0V, V_l = 4.5V$		24	45	mΑ
locz	Supply current, all outputs off	V _{CC} =5.25V, V _I =4.5V		30	52	mA

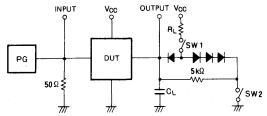
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	rarameter	rest conditions	Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF			15	ns
t _{PHL}	time, from input A to output Y	(Note 3)			15	ns
t _{PZL}	Output enable time to low-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)			38	ns
tpzH	Output enable time to high-level	R _L =667Ω, C _L =45pF (Note 3)			25	ns
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)			25	ns
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)			18	ns

 $[\]star$: All typical values are at V_{CC} = 5V, Ta = 25°C. Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

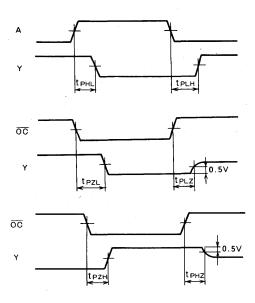
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

Note 3: Measurement circuit



SW 1	SW2
Open	Closed
Closed	Open
Closed	Closed
Closed	Closed
	Open Closed Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
 - $V_P = 3V_{P-P}$, $Z_O = 50\Omega$
- (2) All diodes are switching diodes (t_{rr} ≤ 4ns) (3) C_L includes probe and jig capacitance.



OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS541P is a semiconductor integrated circuit containing 1 buffer block with 3-state non-inverted outputs and is provided with output control inputs which are common to 8 circuits and which are independent.

FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (=400mV typical)
- High breakdown input voltage (V₁ ≥ 15V)
- Output control inputs provided (OC₁, CO₂)
- High fan-out 3-state outputs (I_{OL} = 24mA, I_{OH} = -15mA)
- Data flow-thru pin out
- Wide operating temperature range (T_a=-20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment,

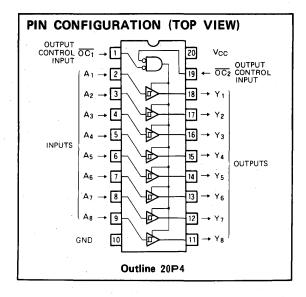
FUNCTIONAL DESCRIPTION

Since pnp transistors are used for the input circuits, the input load factor is small and a input high breakdown voltage is provided. The 3-state non-inverted output buffers have a high noise margin due to hysteresis.

When $\overline{OC_1}$ or $\overline{OC_2}$ is low, low appears in output Y if input A is low, and high appears in Y if A is high.

All outputs are set to the high-impedance state when $\overline{OC_1}$ and $\overline{OC_2}$ are in any other state.

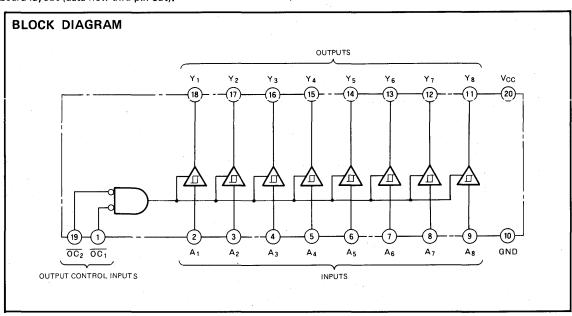
The input and output pins are arranged for facilitated board layout (data flow-thru pin out).



FUNCTION TABLE (Note 1)

Α	A OC1		Υ .
L	L	L	L
Н	L	L	I
Χ.	L	Н	Z
×	Н	L	Z
X	Н.	Н	Z

Note 1 Z : High-impedance X : irrelevant



OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Con	nditions	Limits	Unit	
Vcc	Supply voltage			-0.5~+7		
Vı	Input voltage			-0.5~+15	V	
Vo	Output voltage	Off-state		-0.5~+5.5	V	
Topr	Operating free-air ambient temperature range			-20~+75	°C	
Tstg	Storage temperature range			-65~ + 150	℃	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

	Paramet			Limits		Unit V
Symbol	raramet	ter	Min	Тур	Max	Unit
Voc	Supply voltage	4.75	5	5.25	V	
	Lifet level even a service	V _{OH} ≥2.4V	0		-3	mA
Іон	High-level output current	V _{OH} ≧ 2 V	0		15	mA
	Low love out to the second	V _{OL} ≤0.4V	0		12	mA
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

			F			Limits		Unit	
Symbol	Parameter		Test condition	ns	Min	Typ *	Max	Onit	
VIH	High-level input voltage				2			V	
VIL	Low-level input voltage						0.8	V	
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V			0.2	0.4		V	
V _{IC}	Input clamp voltage	V _{CC} =4.75V,	V _{CC} =4.75V, I _{IC} =-18mA				-1.5	٧	
.,	High-level output voltage	V _{CC} =4.75V	V _{CC} =4.75V V ₁ =0.8V, I _{OH} =-3mA		2.4	3.4		V	
Voн	nign-level output vortage	$V_1 = 2V$ $V_1 = 0.5V, I_{OH} = -15m$, I _{OH} = — 15mA	2			V	
	Low lovel autout value	V _{CC} =4.75V	V _{CC} =4.75V I _{OL} =12mA			0.25	0.4	٧	
V _{OL}	Low-level output voltage	V _I =0.8V, V _I =	=2V	I _{OL} =24mA		0:35	0.5	V	
lozh	Off-state high-level output current	V _{CC} =5.25V,	V _I =2V, V	0=2.7V			20	μА	
lozL	Off-state low-level output current	V _{CC} =5.25V,	V _I =2V, V	0=0.4V			-20	μА	
	High-level input current	V _{CC} =5.25V,	V _I =2.7V				20	μА	
Iн	nigh-level input current	V _{CC} =5.25V,	V _{CC} =5.25V, V _I =10V				0.1	mA	
IιL	Low-level input current	V _{CC} =5.25V,	V _I =0.4V				-0.2	mA	
los	Short-circuit output current (Note 2)	V _{CC} =5.25V,	V _{CC} =5.25V, V _O =0V				-225	mA	
Госн	Supply current, all outputs high	V _{CC} =5.25V,	$V_{CC} = 5.25V, V_{I} = 0V, V_{I} = 4.5V$			18	32	mA	
ICCL	Supply current, all outputs low	V _{CC} =5.25V,	$V_{CC} = 5.25V, V_i = 0V, V_i = 4.5V$			30	52	mA	
locz	Supply current, all outputs disabled	V _{CC} =5.25V,	V _I =0V, V	i=4.5V		32	55	mA	

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

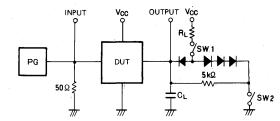
$\textbf{SWITCHING} \ \ \textbf{CHARACTERISTICS} \ \ (V_{CC} = 5V, \ T_{\textbf{a}} = 25^{\circ}\text{C} \ , \ \ \text{unless otherwise noted} \)$

Complete	Deventor	Test conditions	Limits			Unit	
Symbol	Parameter	rest conditions	Min	Тур	Max	Offic	
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C _L =45pF			15	ns	
t _{PHL}	time, from input A to output Y	(Note 3)			18	ns	
t _{PZL}	Output enable time to low-level	R _L =667Ω, C _L =45pF (Note 3)			38	ns	
t _{PZH}	Output enable time to high-level	$R_L = 667\Omega$, $C_L = 45pF$ (Note 3)			32	ns	
t _{PLZ}	Output disable time from low-level	$R_L = 667\Omega$, $C_L = 5 pF$ (Note 3)			29	ns	
t _{PHZ}	Output disable time from high-level	$R_L = 667\Omega$ $C_L = 5 pF$ (Note 3)		Ī .	18	ns	

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

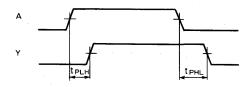
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

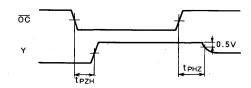
Note 3: Measurement circuit

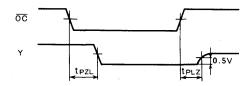


Symbol	SW 1	SW2
t pzH	Open	Closed
t pzL	Closed	Open
t PLZ	Closed	Closed
t phz	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$
- (3) C_L includes probe and jig capacitance.







DESCRIPTION

The M74LS595P is a semiconductor integrated circuit containing an 8-bit serial input/parallel output shift register function with a 3-state output latch.

FEATURES

- 8-bit serial in, parallel out shift register with latch
- Shift register has direct reset (RSFT)
- Independent clock input pins (T_{SFT}, T_{LAT})
- 3-state, high fan-out outputs $(Q_0 \sim Q_7)(I_{OL} = 24 \text{ mA}, I_{OH} = -2.6\text{mA})$
- Cascade output pin provided (Q₇')
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATIONS

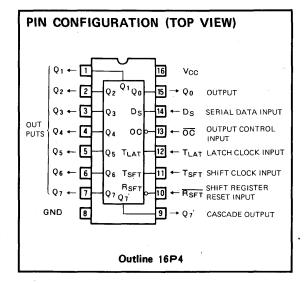
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The shift register bits are each composed of two flip-flops. Separate clocks are used for shifting and latching.

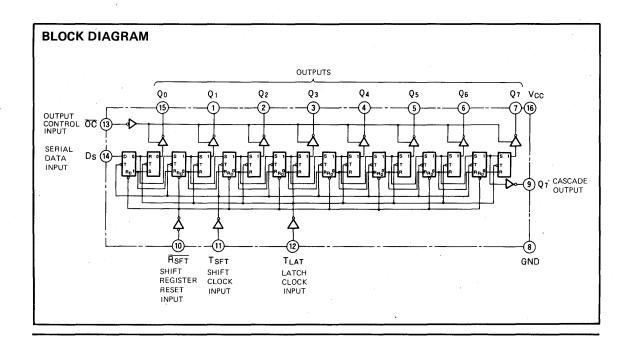
The shift clock input T_{SFT} and latch clock input T_{LAT} are independent, and the shift or latch operation is performed when the respective pin changes from low to high,

Serial data input D_s is the data input of the first stage shift register and when it is high and a pulse is applied to T_{SFT} , the high signal enters the shift register in sequence. When D_s is low and a pulse is applied to T_{SFT} , the low signal enters the shift register in sequence.



When the pulse is applied to T_{LAT} , the contents of the shift register are stored in the latch register and appear at $Q_0 \sim Q_7$. $Q_0 \sim Q_7$ are 3-state outputs with buffers. Cascade output Q_7 at which the output of the eighth shift register appears is used for expanding the number of bits.

When T_{SFT} and T_{LAT} are connected for use, the shift register state with a 1 clock delay is output to $Q_0 \sim Q_7$.



When shift register reset input R_{SFT} is set low, the shift register and Q_7 are reset. In order to reset $Q_0 \sim Q_7$, the state of T_{LAT} must be changed from low to high after the shift register has been reset by $\overline{R_{SFT}}$.

When a high signal is applied to output control input \overline{OC} , $O_0 \sim O_7$ are put in a high-impedance state but O_7 does not change. \overline{OC} status changes have no effect on the shift operation.

FUNCTION TABLE (Note 1)

0				Input						3-stat	e output	-			Cascade
Operati	Operating mode		T _{SFT}	TLAT	Ds	ōc	Q ₀	Q1	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	output Q'7
Reset	Shift t ₁	L	Х	Х	Х	L	Q_0^0	Q ₁ 0	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰	L
Heset	Latch t ₂	×	Х	1	Х	L	L	L	L	L	L	L	L	L	L
	Shift t ₁	н	1	×	Ξ	L	Q ₀ 0	Q ₁ 0	Q2 ⁰	Q ₃ 0	Q ₄ ⁰	Q ₅ 0	Q ₆ 0	Q7 ⁰	9 6 ⁰
Shift/latch	Latch t ₂	Н	Х	1	Х	L	Н	900	q 1 ⁰	92 ⁰	930	94 ⁰	95 ⁰	96 ⁰	9 ₆ 0
operation	Shift t ₁	Н	1	Х	L	L	Q ₀ 0	Q1 ⁰	Q ₂ ⁰	Q ₃ 0	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q7 ⁰	96 ⁰
	Latch t ₂	ιн	Х	1	Х	L	L	900	q 1 ⁰	92 ⁰	93 ⁰	940	95 ⁰	96 ⁰	96 ⁰
3-s	tate	×	×	х	X	н	z	z	z	z	Z	Z	z	Z	. 97

Note 1. ↑: transition from low to high level (positive edged trigger)

 Q^0 : level of Q before the indicated steady-state input conditions were established

X : Irrelevant

q0 : contents of shift register before $T_{\mbox{\scriptsize SFT}}$ is applied

q: shift register contents

 $t_{\,1},\,t_{\,2}$: $\,t_{\,2}$ is set after $t_{\,1}$ has been set

Z: high-impedance state

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

Symbol	Para	meter	Test conditions	Limits	Unit
Vcc	Supply voltage		Supply voltage		V
Vi	Input voltage			-0.5~+15	V
	0	Q0~Q7	High-level state	-0.5~+5.5	V
V ₀	Output voltage	Q7	Off-state	-0.5~V _{CC}	V
Topr	Operating free-air ambient to	emperature range		-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter				Unit		
Зутьог				Min	Тур	Max	Onit
Vcc	Supply voltage			4.75	5	5.25	V
	High-level output	Q0~Q7	V _{OH} ≥2.4∨	0		-2.6	mA
1он	current	Q1	V _{OH} ≥2.7V	0		-400	μА
			V _{OL} ≤0.4V	0		12	mA
	Low-level output	Q0~Q7	V _{OL} ≤0.5V	0		24	mΑ
loL	current		V _{OL} ≤0.4V	0		4	mΑ
		Q ₁ '	V _{OL} ≤0.5V	0		8	mΑ

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test condi	tions		Limits		Unit
Зупівої	rarameter		l est condi	ŲO11S	Min	Typ *	Max	. Onit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.8	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
.,	High-level output voltage	Q0~Q7	V _{CC} =4.75V	I _{OH} =-2.6mA	2.4	3.1		V
VoH	Thigh-level output voltage	Q ₇ ′	V _I =0.8V, V _I =2V	I _{OH} = -400μA	2.7	3.4		V
				I _{OL} =12mA		0.25	0.4	٧
	l and land and an indicate	Q ₀ ~Q ₇	V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	V
V _{OL}	OL Low-level output voltage	0.	V _I =0.8V	I _{OL} =4mA		0.25	0.4	V
		Q ₁ '	V ₁ =2V	I _{OL} =8mA	,	0.35	0.5	V
lozh	Off-state high-level output current	Q ₀ ~Q ₇	V _{CC} =5.25V, V _I =0.8V, V _I =2V, V _O =2.7V			1.	20	μА
lozL	Off-state low-level output current	Q ₀ ~Q ₇	V _{CC} =5.25V, V _I =0.8V,	V _I =2V, V _O =0.4V	1		-20	μΑ
1.	in the same of the		V 5 05V	V ₁ =2.7V		,	20	μА
li _H	High-level input current		V _{CC} =5.25V	V _I =10V			0,1	mA
	Low-level input current	Ds					-0.4	mA
I _{IL}	Low-level input current	Input except Ds	V _{CC} =5.25V, V _I =0.4	· '			-0.2	mA
	Chart day in the control of the cont	Q ₀ ~Q ₇			-30		-130	mΑ
los	Short-circuit output current (Note 2)	Q ₇ ′	$V_{CC}=5.25V, V_{O}=0V$		-20		-100	mA
Госн	High-level supply current		V _{CC} =5.25V, V _I =0V, V _I =4.5V			29	50	mA
ICCL	Low-level supply current		V _{CC} =5.25V, V _I =0V, V _I =4.5V			39	65	mA
I _{CCZ}	Off-state supply current		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		41	65	mA

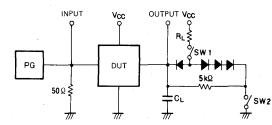
^{* :} All typical values are at $V_{CC} = 5V$, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Cumbal	Parameter	Test conditions		Unit		
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
f _{max}	Maximum repeat frequency		20	25		MHz
t _{PLH}	Low-to-high, high-to-low output propagation time, from			11	18	ns
t PHL	input T _{SFT} to output Q' ₇	C ₁ = 15pF (Note 3)		16	25	115
t _{PHL}	High-to-low output propagation time from input $\overline{R_{SFT}}$ to output Q_7^{\prime}	OL- 19PF (Note 3)		19	35	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from	C ₁ = 45 pF (Note 3)		12	18	ns
t _{PHL}	input T_{LAT} to outputs $Q_0 \sim Q_7$	CL=45 pr (Note 3)		22	35	115
t _{PZH}	Output enable time to high level	B -557 O C -450 E (Nov. 2)		16	30	ns
t _{PZL}	Output enable time to low level	$R_L=667 \Omega$, $C_L=45pF$ (Note 3)		20	38	ns
t _{PHZ}	Output disable time to high level	$R_1 = 667 \Omega$, $C_1 = 5pF$ (Note 3)		22	30	ns
t _{PLZ}	Output disable time to low level			17	38	ns

Note 3. Measurement circuit



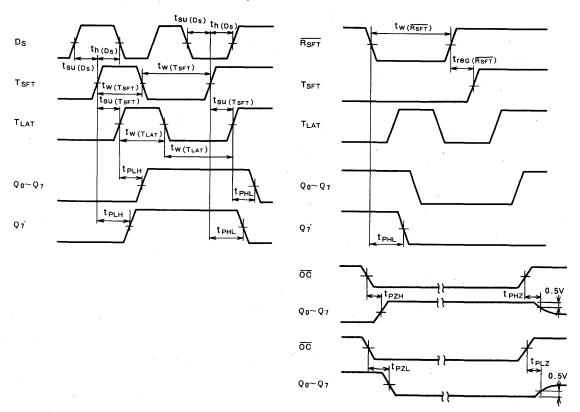
Paramete	er SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_t = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 ohms.
- (2) All diodes are switching diodes $(t_{rr} \le 4ns)$.
- (3) C_L includes probe and jig capacitance.



TIMING REQUIREMENTS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$, unless otherwise noted)

	Parameter	Total and distance		Unit		
Symbol	rarameter	Test conditions	Min	Тур	Max	Unit
tw(Tsft)	Shift clock input pulse width ,		25	22		ns
tw(TLAT)	Latch clock input pulse width		20	12		ns
tw(R _{SFT})	Shift register reset pulse width	·	20	10		ns
t _{su(Ds)}	Setup time D _s to T _{SFT}	·	20	12		ns
t _{h (Ds)}	Hold time D _s to T _{SFT}		2	-1		ns
t _{rec(RsfT})	Recovery time R _{SFT} to T _{SFT}		20	12		ns
t _{su (TsfT})	Setup time T _{SFT} to T _{LAT}		40	12		ns



DESCRIPTION

The M74LS596P is a semiconductor integrated circuit containing an 8-bit serial input/parallel output shift register function with an open collector output latch.

FEATURES

- 8-bit serial in parallel out shift register with latch.
- Shift register has direct reset (RSFT)
- Independent clock input pins (T_{SFT}, T_{LAT})
- Open-collector, high fan-out outputs (Q₀~Q₇) (I_n= 24mA)
- Cascade output pin provided (Q'₇)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATIONS

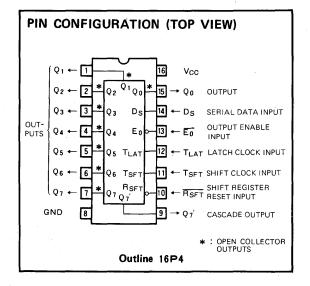
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The shift register bits are each composed of two flip-flops Separate clocks are used for shifting and latching.

The shift clock input T_{SFT} and latch clock input T_{LAT} are independent, and the shift or latch operation is performed when the respective pin changes from low to high.

Serial data input D_s is the data input of the first stage shift register and when it is high and the pulse is applied to Tsft, the high signal enters the shift register in sequence. When D_s is low and a pulse is applied to T_{SFT} , the low signal enters a shift register in sequence.

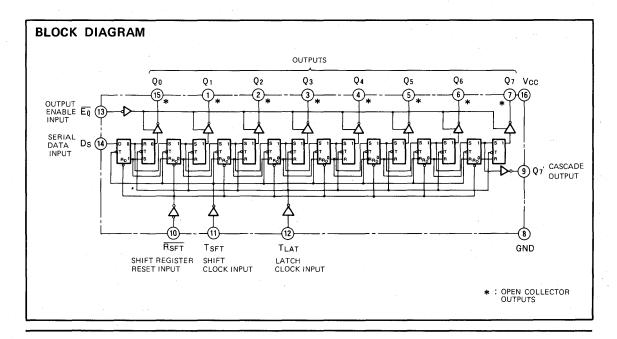


When a pulse is applied to T_{LAT} , the contents of the shift register are stored in the latch register and appear at $Q_0 \sim Q_7$. $Q_0 \sim Q_7$ are open collector outputs with buffers.

Cascade output Ω_7 ' at which the output of the eighth shift register appears is used for expanding the number of bits.

When T_{SFT} and T_{LAT} are connected for use, the shift register state with a 1 clock delay is output to $Q_0 \sim Q_7$.

When shift register reset input $\overline{R_{SFT}}$ is set low, the shift



register and Q'_7 are reset. In order to reset $Q_0 \sim Q_7$, the state of T_{LAT} must be changed from low to high after the shift register has been reset by $\overline{R_{SFT}}$.

When a high signal is applied to output enable input $\overline{E_0}$, $Q_0 \sim Q_7$ are set high but Q_7 does not change. $\overline{E_0}$ status changes have no effect on the shift operation.

FUNCTION TABLE (Note 1)

				Input					(Open colle	ctor outpu	it .			Cascade
Operatir	ng mode	RSFT	TSFT	TLAT	Ds	Εo	Qo	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	output Q'7
_	Shift t ₁	L	×	Х	×	L	Q_0^0	Q1 ⁰	Q ₂ 0	Q ₃ 0	Q4 ⁰	Q5 ⁰	Q ₆ 0	Q ₇ 0	L
Reset	Latch t ₂	Х	×	1	х	L	L	L	L	L	L	L	L	L	L
	Shift t ₁	Н	1	Х	Н	L	Q_0^0	Q1 ⁰	Q ₂ 0	Q3 ⁰	Q4 ⁰	Q5 ⁰	Q ₆ ⁰	Q ₇ 0	. 96 ⁰
Shift/latch	Latch t ₂	Н	. X	1	X	L	Н	900	q 1 ⁰	92 ⁰	93 ⁰	. q ₄ 0	95 ⁰	96 ⁰	96 ⁰
operation	Shift t ₁	Н	1	Х	L	L	Q ₀ 0	Q 1 ⁰	Q ₂ 0	Q ₃ ⁰	Q ₄ ⁰	Q ₅ 0	Q6 ⁰	Q ₇ 0	96 ⁰
-	Latch t ₂	Н	Х	1	×	L	L	90 ⁰	91 ⁰	92 ⁰	93 ⁰	94 ⁰	95 ⁰	96 ⁰	9 ⁰ 6
Output disab	ole	×	Х	Х	X	Н	Н	Н	Н	н	Н	Н	. H	Н.	q ₇

Note . ↑: transition from low to high level (positive edged trigger)

 Q^0 : level of Q before the indicated steady-state input conditions were established

X: irrelevant

q0: contents of shift register before $T_{\mbox{\scriptsize SFT}}$ is applied

q : shift register contents

t 1, t 2: t2 is set after t1 has been set

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 \, ^{\circ}C$, unless otherwise noted)

Symbol	Parameter Conditions				Limits	Unit
Vcc	Supply voltage				-0.5~+7	V
Vı	Input voltage				-0.5~+15	V
	0	Q0~Q7	I Patrick and Associated	i	-0.5~+7	V
Vo	Output voltage	Qį	High-level state		-0.5~V _{CC}	V
Topr	Operating free-air ambient ten	nperature range			−20~+75	°C
Tstg	Storage temperature range				-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter				Limits				
Symbol				Min	Тур	Max	Unit		
Vcc	Supply voltage			4.75	5	5.25	V		
,	High-level output	Q0~Q7	V ₀ =5.5V	0		100	μΑ		
ТОН	current	Q ₇ ′	V _{OH} ≥2.7V	0		-400	μА		
		Q0~Q7	V _{OL} ≤0.4V	0		12	mÀ		
•	Low-level output		V _{OL} ≤0.5V	0		24	mA		
loL	current	0.1	V _{OL} ≤0.4V	. 0		4	mA		
	1 1	Q i	V _{OL} ≤0.5V	0		8	mA		

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combal	D			Material Control		Limits		Unit
Symbol	Parameter		Test co	Min	Тур	Max	Unit	
V _{IH}	High-level input voltage				2			٧
VIL	Low-level input voltage					ļ	0.8	V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	-18mA			-1.5	٧
Vон	High-level output voltage	Q ₇ ′	$V_{CC}=4.75V, V_{I}=0.8V, V_{I}=2V, I_{OH}=-400 \mu A$		2.7	3.4		٧
Гон	High-level output voltage	Q ₀ ~Q ₇	V _{CC} =4.75V, V _I =0.8V, V _I =2V, V _O =5.5V				100	μА
		Q ₀ ~Q ₇	V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
V-	Low-level output voltage	V ₁ =0.8V	IOL=24mA		0.35	0.5	٧	
VoL	Low-level output voltage	Q ₇	$V_1=0.8V$ $V_1=2V$	I _{OL} =4mA		0.25	0.4	V
	,	Q7	V -2V	I _{OL} =8mA		0.35	0.5	V
IIH				V ₁ =2.7V			20	μА
'IH	High-level input current		V _{CC} =5.25V	V _I =10V			0.1	mΑ
1	Low-level input current	Ds	V _{CC} =5,25V, V _I =0	2.41/			-0.4	mA
1 ₁ L	Low-level input current	Input except Ds	VCC-5.25V, VI-1	J.4V			-0.2	mA
los	Short-circuit output current (Note 2)	Q ₇ ′	V _{CC} =5.25V, V _O =	0 V	— 20		-100	mA
Гссн	High-level supply current		V _{CC} =5.25V, V _I =0V, V _I =4.5V					mA
ICCL	Low-level supply current		V _{CC} =5.25V, V _I =0V, V _I =4.5V					mA
locz	Off-state supply current		V _{CC} =5.25V, V _I =	0V, V _I =4.5V				mA

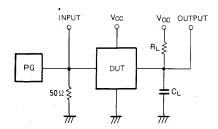
^{* :} All values are at $V_{CC} = 5V$, $T_a = 25$ °C

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

D. and and		Total		Unit		
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
f _{max}	Maximum repeat frequency from input T _{SFT} to output Q' ₇		20	25		MHz
t _{PLH}	Low-to-high, high-to-low output propagation time, from			16	21	
t _{PHL}	input T _{SFT} to output Q' ₇	$R_L=2k \Omega$, $C_L=15p F$ (Note 3)		12	30	ns
t _{PHL}	High-to-low output propagation time from input R _{SFT} to output Q' ₇			19	35	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from			24	42	
t _{PHL}	input T_{LAT} to outputs $Q_0 - Q_7$	P657.0. 0 -45.55 (Nov. 2)		23	35	ns
t _{PLH}	Low-to-high, high-to-low output propagation time, from	$R_L=667 \Omega$, $C_L=45 pF$ (Note 3)		30	60	
t _{PHL}	input $\overline{E_0}$ to output $Q_0 - Q_0$			12	38	ns

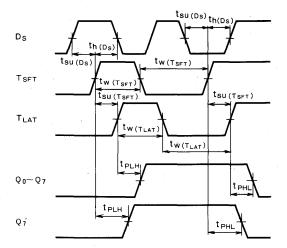
Note 3. Measurement circuit

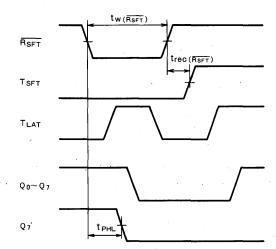


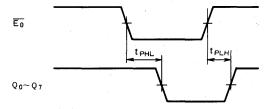
- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_o = 50 ohms.
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC} = 5V$, $Ta = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	Farameter	lest conditions	Min	Тур	Max	Unit
tw(TsfT)	Shift clock input pulse width		25	22		ns .
tw(TLAT)	Latch clock input pulse width		20	12		ns
tw(R _{SFT})	Shift register reset pulse width		20	9		ns
t _{su (Ds)}	Setup time D _s to T _{SFT}		20	12		ns
t _{h (Ds)}	Hold time D _s to T _{SFT}		2	-1		. ns
trec(R _{SFT})	Recovery time R _{SFT} to T _{SFT}		20	12	-	ns
t _{Su(TSFT)}	Setup time T _{SFT} to T _{LAT}		40	12		ns







DESCRIPTION

The M74LS620P is a semiconductor integrated circuit containing an octal bus transmitter/receiver with a tri-state inverted output.

FEATURES

- Two 8-bit data trains can be transmitted bidirectionally or as unidirectional pulses
- Input/output A and output/input B each exhibit hysteresis characteristics (Hysteresis width = 400mV typ)
- High fan-out capability (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment

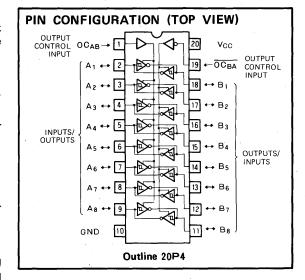
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state inverted outputs are made two-way buffers.

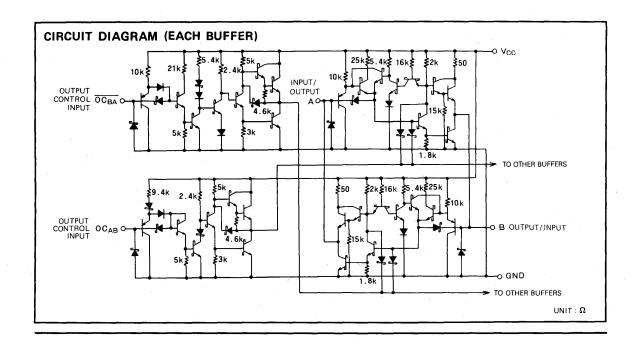
The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin.

The input/output direction is controlled by OC_{AB} and $\overline{OC_{BA}}$.

When OC_{AB} and $\overline{OC_{BA}}$ are high, A becomes the input pin, with output obtained at pin B. Conversely, when OC_{AB} are $\overline{OC_{BA}}$ are low, B is the input and A is the output.



A high impedance status is initiated at both pin A and B when OC_{AB} is low and $\overline{OC_{BA}}$ is high, isolating A from B. Precautions should be taken to guard against OC_{AB} being at a high while $\overline{OC_{BA}}$ is low. This condition will result in output from both A and B, and could result in the IC being destroyed.



FUNCTION TABLE (Note 1)

OCBA	OCAB	Α	В
L	L	0	1
,H	Н	ī	o
Н	L	Z	Z
L	Н	*	*

Note 1. | : Input pin

O : Output pin

Z: High-impedance (A and B isolated)

* : Inhibit (No output from either A or B)

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
	Input voltage A, B OCAB, OCBA		·	-0.5~+5.5	V
Vı				-0.5~+15	V
Vo	Output voltage		Off-state	-0.5~+5.5	٧
Topr	Operating free-air ambie	nt temperature range		-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

	Parameter		Limits			Unit
Symbol	Param	eter	Min	Тур	Max	Unit
Vcc	Supply voltage	Supply voltage		5	5.25	V
	High lovel output august	V _{OH} ≥2.4V	0		-3	mA
Гон	High-level output current V _{OH} ≥2V		0		-15	mA
		V _{OL} ≦0.4V	0		12	mA
IOL	Low-level output current	V _{0L} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75$ °C, unless otherwise noted)

Consideration	Parameter		T 1			Limits		Unit
Symbol	i al amete		Test conditions		Min .	Тур 🛊	Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage						0.6	٧
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
	High-level output voltage		V _{CC} =4.75V	$I_{OH} = -3 \text{mA}$	2.4	3.4		V
V _{OH}	riigii-ievei output voitage		$V_1 = 0.6 V, V_1 = 2 V$	I _{OH} = -15mA	2			V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧
V _{OL}	Low-level output voltage		$V_1 = 0.6 V, V_1 = 2 V$	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V,	$V_1 = 2V, V_0 = 2.7V$			20	μΑ
lozL	Off-state low-level output curre	ent	$V_{CC}=5.25V, V_{I}=0.6V, V_{I}=2V, V_{O}=0.4V$				-400	μА
		A, B	V 5 05 V V 0 7				20	μА
1	High-level input current	OCBA, OCAB	$V_{CC}=5.25V, V_{I}=2.7$	V			20	μΑ
li _H	riigit-lever input current	А, В	V _{CC} =5.25V, V _I =5.5	V .			0.1	mA
		OCBA, OCAB	V _{CC} =5.25V, V _I =10V		-		0.1	mΑ
fil	Low-level input current		V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output current (N	Note 2)	V _{CC} =5.25V, V _C =0V		-40		-225	mA
Гссн	Supply current, all outputs hig	jh .	V _{CC} =5.25V, V _I =0V,	V _I =4.5V		48	7Ò	mA
IccL	Supply current, all outputs low	v .	V _{CC} =5.25V, V _I =0V,	V _I =4.5V		62	90	mA
locz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V,	V _I =4.5V		64	95	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

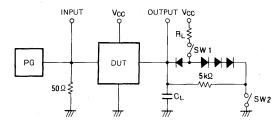


Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

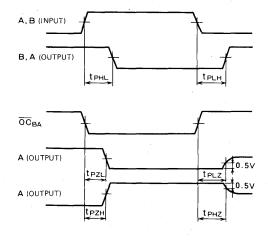
Symbol	Parameter Test conditions		Tost conditions	Limits			Unit
Symbol			rest conditions	Min Typ		Max	Unit
t	Low-to-high-level output From input A to output B			8	10	20	
tpLH	propagation time	From input B to output A	C ₁ = 45 pF (Note 3)		8	10	ns
•	High-to-low level output	From input A to outputB	CL=45pF (Note 3)		12	15	
t _{PHL}	propagation time	From input B to output A	•		12	15	ns
	Output enable time to	From input OCBA to output A			25	40	
t _{PZL}	low-level	From input OCAB to output B	B = 557.0 0 457.5 W 8		25	40	ns
	Output enable time to	From input OCBA to output A	R_{L} =667 Ω, C_{L} =45pF (Note 3)		23	40	
t _{PZH}	high-level	From input OCAB to output B			. 23	40	ns
	Output disable time from	From input OCBA to output A			17	25	
t _{PLZ}	low-level	From input OCAB to output B			17	25	ns
•	Output disable time from	From input OCBA to output A	$R_{\perp}=667 \Omega$, $C_{\perp}=5pF$ (Note 3)		19	25	
t _{PHZ}	high-level	From input OCAB to output B	·		19	25	ns

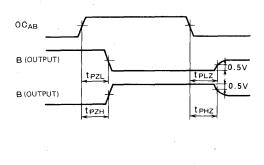
Note 3: Measurement Circuit



Paramete	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
tpLZ	Closed	Closed
t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_{P-P} , Z_Ω = 50 Ω .
- t_W = 500ns, V_P = 3V_{P.P.}, Z_O = 50Ω. (2) All diodes have high-speed switching characteristics (t_{rr} ≤ 4ns)
- (1_{rr} ≥ 4ns)
 (3) C_L includes probe and jig capacitance.





MITSUBISHI LSTTL:

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS640P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

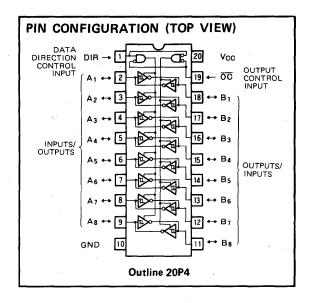
FUNCTIONAL DESCRIPTION

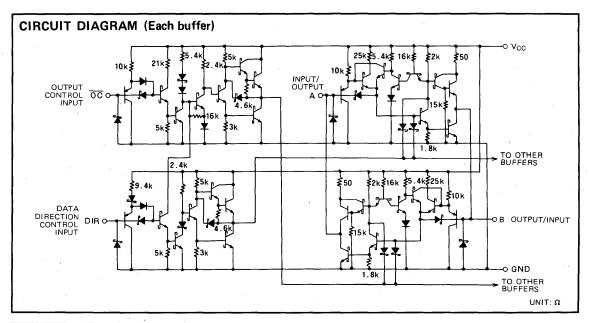
The inputs and outputs of the two buffer circuits with 3-state inverted outputs are connected together to form bidirectional buffers. Having hysteresis characteristics in the input section of input/output A and output/input B, noise margin is high.

The data direction control input DIR controls the direction of input and output. When DIR is high, A is the input terminal and B is the output terminal and when DIR is low, A is the output terminal and B is the input terminal.

When the output control input \overline{OC} is high, both A and B are put in the high-impedance state so the buffers are isolated.

A device, M74LS640-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.





FUNCTION TABLE (Note 1)

ŌŌ	DIR	Α	8
L	L	σ	l
L	н	1	· ō
Н	x	Z	Z

Note 1: I: Input pin

O: Output (inverted output) pin

Z: High impedance (A and B separated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Parameter Supply voltage		Conditions	Limits	Unit
Vcc				-0.5~+7	٧
.,	Input voltage	А, В		$-0.5 \sim +5.5$	V
V	Input voltage	DIR, OC		-0.5~+15	V
Vo	Output voltage		Off state	−0 .5~+5.5	V
Topr	Operating free-air ambie	nt temperature range		-20~+75	ా
Tstg	Storage temperature ran	ge		-65~+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	rarameter			Тур	Max	Unit	
Voc	Supply voltage	Supply voltage		5	5.25	V	
	I Patrick	V _{OH} ≥2.4V	0		-3	mA	
ТОН	High-level output current	V _{OH} ≥2V	0		- 15	mA	
1		V _{0L} ≤0.4V	0		12	mA	
, I OL	Low-level output current	V _{0L} ≤0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \degree$, unless otherwise noted)

Committee of	Parameter		Toot oons	Test conditions		Limits		
Symbol	Parameter		rest conditions		Min	Typ *	Max	Unit
ViH	High-level input voltage				2			V
VIL	Low-level input voltage				-		0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	-18mA			-1.5	V
.,			V _{CC} =4.75V	I _{OH} = - 3 mA	2.4	3.4		٧
Voн	High-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OH} = - 15mA	2			V
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VOL	Low-level output voltage		V _I =0.6V, V _I =2V	I _{OL} =24mA		0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V	$V_1 = 2V_1 V_0 = 2.7V$			20	μA
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V, V _I =2V, V _O =0.4V				-400	μΑ
		A, B	V _{CC} =5.25V, V _I =2.	7\/			20	μА
1	High-level input current	DIR, OC	V _{CC} =5.25V, V _I =2.				20	μА
ЧН	ringit-level impat current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10	v			0.1	mΑ
I _I L	Low-level input current		V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note	2)	V _{CC} =5.25V, V _O =0V		- 40		-225	mA
Icch	Supply current, all outputs high	* .	V _{CC} =5.25V, V _I =0V	, V _I =4.5V		48	70	mA
ICCL	Supply current, all outpus low		V _{CC} =5.25V, V _I =0V, V _I =4.5V			.62	90	mΑ
lccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	', V _I =4.5V		64	95	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.

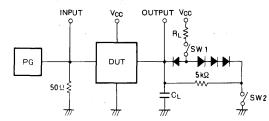
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25$ °C, unless otherwise noted)

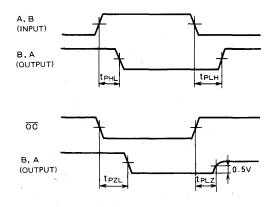
0		Parameter			Limits		Unit
Symbol	Parameter		Test conditions	Min	Тур	Max	Unit
	Low-to-high level output	From input A to output B			8	10	
t _{PLH}	propagation time	From input B to output A	0:45:5 (4:0)		8	10	n.s
	High-to-low level output	From input A to output B	C _L =45pF (Note 3)		12	15	
t _{PHL}	propagation time	From input B to output A			12	15	ns
		From input OC to output A			25	40	ns
tpZL	Low output enable time	From input OC to output B	$R_{\perp} = 667\Omega$ $C_{\perp} = 45pF$		25	40	. 115
	Ulah autaut asahia tima	From input OC to output A	(Note 3)		23	40	
t _{PZH}	High output enable time	From input OC to output B			23	40	ns
	1	From input OC to output A			17	25	
tpLZ	Low output disable time	From input OC to output B	$R_{\perp} = 667\Omega$ $C_{\perp} = 5pF$		17	25	ns
	High output disable time	From input OC to output A	(Note 3)		19	25	
t _{PHZ}	nigri output disable time	From input OC to output B			19	25	ns

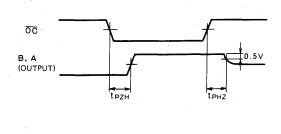
Note 3: Measurement circuit



Parameter	SW 1	SW2
t pzh	Open	Closed
t PZL	Closed	Open
t PLZ	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
- (2) All diodes are high speed switching diodes (trr < 4ns).</p>
- (t_{rr} ≤ 4ns).
 (3) C_L includes probe and jig capacitance.





M74LS640-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS640-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out ($I_{OL} = 48mA$, $I_{OH} = -15mA$)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

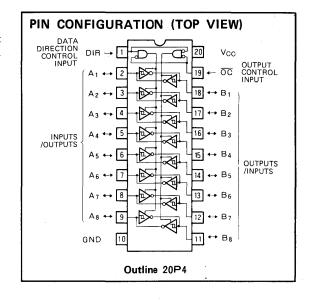
General purpose, for use in industrial and consumer equipment.

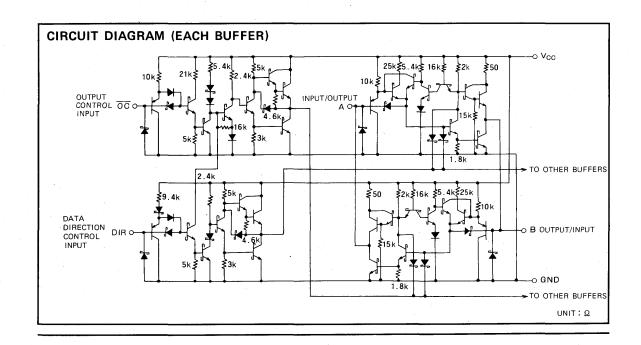
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When \overline{OC} is high, both A and B are put in the high-impedance state and A and B are isolated.





FUNCTION TABLE (Note 1)

ŌŌ	DIR	Α .	В
. L	L	ō	
. L	н	I	ō
н	×	Z	Z

Note 1: I : Input pin

Output (inverted) pin

Z: High-impedance (A, B isolated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 - +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
VI	Input voltage	A, B		-0.5~+5.5	V
		DIR, OC		-0.5~+15	V
Vo	Output voltage		Off-state	-0.5~+5.5	V.
Topr	Operating free-air ambier	nt temperature range		-20~+75	r
Tstg	Storage temperature rang	je		-65~+150	ာ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		,			
Зупрог	raramete	Min	Тур	Max	Unit	
Voc	Supply voltage		4.75	5	5.25	٧
1	High-level output current	V _{OH} ≧2.4V	0		-3	mA
ТОН		V _{OH} ≥2V	0		-15	· mA
loL	Low-level output current	V _{OL} ≦0.4V	. 0		12	mA
	Low-level output current	V _{OL} ≤0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	Parameter		Test conditions		Limits			
Symbol					Min	Тур 🛊	Max	Unit
V _{IH}	High-level input voltage	High-level input voltage						V
VIL	Low-level input voltage						0.6	V
VT+VT-	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
	High-level output voltage		V _{CC} =4.75V	I _{OH} = - 3 mA	2.4	3.4		V
Voн			$V_1 = 0.6V, V_1 = 2V$	I _{OH} = - 15mA	2			V
	Low-level output voltage		V _{CC} =4.75V V _I =0.6V, V _I =2V	I _{OL} =12mA		0.25	0.4	V
VoL				I _{OL} =24mA		0.35	0.5	V
				I _{OL} =48mA		0.4	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V	$, V_1 = 2V, V_0 = 2.7V$			20	μА
lozL	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V	$, V_1 = 2V, V_0 = 0.4V$			-400	μА
	High-level input current	A, B	Vcc=5.25V V=2.7V			20	μA	
Luc		DIR, OC	V _{CC} =5.25V, V =2.7V				20	μА
'ін		A, B	V _{CC} =5.25V, V _I =5.5	SV .			0.1	mA
	DIR, OC		V _{CC} =5.25V, V _I =10V				0.1	mA
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4V				-0.4	mA
los	Short-circuit output current (Note 2)		V _{CC} = 5.25V . V _O = 0V		-40		- 225	mA
1 _{OCH}	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		48	70	mA
IccL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V, V _I =4.5V			62	90	mA
locz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	, V _I =4.5V	_	64	95	mA

 $[\]star$: All typical values are at $V_{CC}=5V$, $Ta=25^{\circ}C$

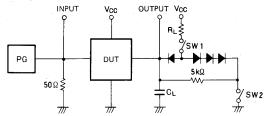
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

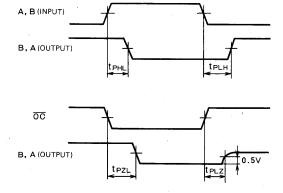
Symbol	Parameter		Test conditions	Limits			11.74	
Symbol	raianie	rtet	· rest conditions	Min	Тур	Max	Unit	
†	Low-to-high-level	Low-to-high-level From input A to o	From input A to output B			8	10	
t _{PLH}	output propagation time	From input B to output A	0 = 45=5 (N== 0)		8	10	ns	
	High-to-low level	From input A to output B	C _L =45pF (Note 3)		12	15		
t _{PHL}	output propagation time	From input B to output A			12	15	ns	
	Law level autout analyte time	From input OC to output A			25	40	ns	
t _{PZL}	Low-level output enable time	From input OC to output B			25	40	113	
	High-level output enable time	From input OC to outputA	4		23	40	ns	
t _{PZH}	PZH High-level output enable time	From input OC to outputB			23	40	118	
	Low-level output disable time	From input OC to outputA			17	25	ns	
t _{PLZ}		From input OC to output B	$R_1 = 667\Omega$ $C_1 = 5pF$ (Note 3)		17	25	113	
	High-level output disable time	From input OC to output A	n 00/2		19	25		
t _{PHZ}		From input OC to output B			19	25	ns	

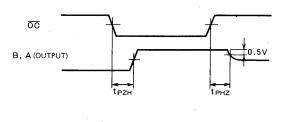
Note 3: Measurement circuit



Symbol	SW 1	SW2		
t _{PZH}	Open	Closed		
tpzL	Closed	Open		
t PLZ	Closed	Closed		
t _{PHZ}	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) All diodes are switching diodes $\{t_{rr} \le 4ns\}$.
- (3) C_L includes probe and jig capacitance.





MITSUBISHI LSTTL: M74LS641P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA)
- Wide operating temperature range. (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

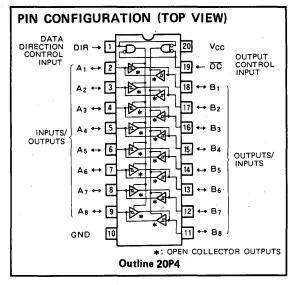
FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

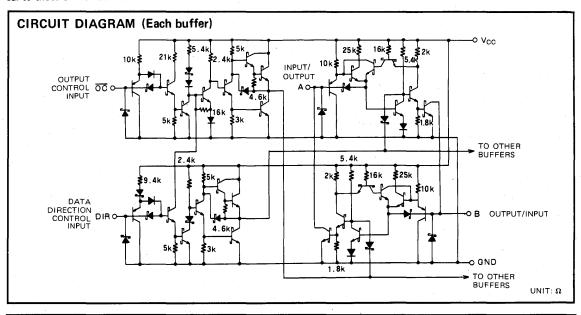
When DIR is high, A is the input pin and B is the output pin. When DIR is low then B is input terminal and A is the output terminal. When output control input OC is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.

The functions and pin connections of this IC are identical to those of M74LS645P.



A device, M74LS641-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



FUNCTION TABLE (Note 1)

ŌĈ	OC DIR		В
L	L	0	1
L	н	I	0
Н	X	Н	н

Note 1: 1: Input pin

O: Output (non-inverted output) pin

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Par	Parameter Conditions Supply voltage		Limits	Unit	
V _{CC} Supply voltage				Supply voltage		-
V _I Input voltage	А, В			-0.5~+7	V	
Vı	Input voltage	DIR, OC			-0.5∼+15	V
Vo	Output voltage		High-level state		-0.5~+7	V
Topr	Operating free-air ambie	ent temperature range			-20~+75	င
Tstg	Storage temperature ran	nge			-65~+150	င

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter					
Sympol	raran	- arameter			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		100	μА
	I am land an entered annual	V _{OL} ≤0.4V	0		12	mΑ
lor	Low-level output current	V ₀ ∟≦0.5∨	0		24	mA_

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}$, unless otherwise noted)

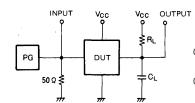
Symbol	Parameter		Tost oon	Test conditions		Limits		
Syllibol			l est com			Тур *	Max	Unit
V _{IH}	High-level input voltage				2.			V
VIL	Low-level input voltage						0.6	V
/ _{T +} - V _{T -}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			-1.5	V
Іон	High-level output current		V _{CC} =4.75V, V _I =0.6V, V	/ ₁ '=2V, V ₀ =5.5V			100	μА
VoL Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V	
	Low-level output voltage		$V_1 = 0.6V, V_1 = 2V$	IOL=24mA		0.35	0.5	V
	A, B					20	μА	
	Mate Investigation	DIR, OC	$V_{CC} = 5.25V, V_I = 2.7V$				20	μΑ
IIH	High-level input current	А, В	V _{CC} =5.25V, V _I =5.5	īV			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10V	V .			0.1	mA
liL.	Low-level input current		V _{CC} =5.25V, V _I =0.4	IV			-0.4	mA
Ісон	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V	,. V _I = 4.5V		48	70	mA
ICCL	Supply current, all outputs I	ow	V _{CC} =5.25V, V _I =0V	, V _I = 4.5V		62	90	mΑ
lccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	, V ₁ =4.5V		64	95	mΑ

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

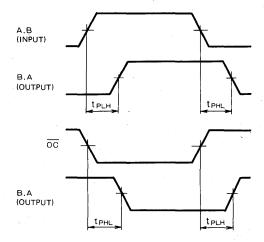
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, Ta = 25°C, unless otherwise noted)

Symbol	Do.	Parameter		Limits			Hele
	Par			Min	Тур	Max	Unit
t PLH Low-to-high level output propagation time	Low-to-high level output	From input A to output B	·		20	25	
	From input B to output A]		- 20	25	ns	
	High-to-low level output	From input A to output B	The second second		15	. 25	
t _{PHL}	propagation time	From input B to output A	0 45-5 0 667 0 (No2)		15	25	ns
	Low-to-high level output	From input OC to output A	$C_L=45pF$, $R_L=667\Omega$ (Note 2)		25	40	
t PLH propagation time	From input OC to output B	1	,	25	40	ns	
t PHL High-to-low level output propagation time	From input OC to output A]		30	50		
	From input OC to output B	1		30	50	ns	

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_W = 500ns, V_P = 3 V_P .P, Z_O = 50 Ω
- (2) CL includes probe and jig capacitance.



M74LS641-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with non-inverted outputs,

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

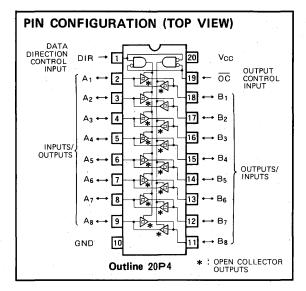
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with open collector non-inverted outputs are made two-way buffers.

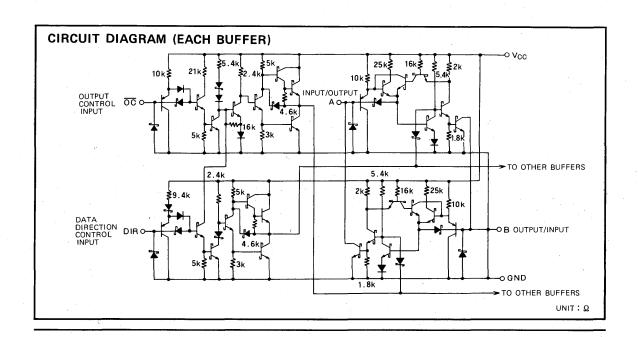
The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When output control input \overline{OC} is high,



both A and B go to high and are isolated.

The functions and pin connections of this device are identical to those of M74LS645-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.



FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	. L	0	I
L	Н	. 1	0
Н	Х	н	н

Note 1: | Input pin

O: Output (non-inverted) pin

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Pa	Parameter Conditions		Limits	⊍nit	
Vcc	Supply voltage		· ·	5	$-0.5 \sim +7$	V
		A, B			-0.5∼+7	٧
VI	Input voltage	DIR, OC			-0.5 ∼+15	, V,
Vo	Output voltage		High-level state		-0.5~+7	V
Topr.	Operating free-air ambier	nt temperature range			-20~+75	°C
Tstg	Storage temperature range	ge			−65 ~ + 150	င

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}C$, unless otherwise noted)

C	D	Parameter		Limits			
Symbol	Parame			Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	. V	
Іон	High-level output current	V ₀ =5.5V	0		100	μΑ	
Γ.	Low-level output current	V _{OL} ≤0.4V	0		. 12	mA	
lor	Low-level output current	V _{OL} ≤0.5V	0		48	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

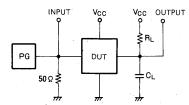
Symbol	Paramete		T	***	Limits			Unit
Symbol	raramete		Test conditions		Min	Тур 🗱	Max	Unit
V _{IH}	High-level input voltage	voltage			2			V
VIL	Low-level input voltage				. :		0.6	٧
V _{T +} - V _{T -}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	- 18 mA	,		-1.5	V
Гон	High-level output current		V _{CC} =4.75V, V _I =0.6V,	V ₁ = 2V, V ₀ = 5.5V			100	μΑ
V _{OL} Low-le			4.75	I _{OL} =12mA		0.25	0.4	٧
	Low-level output voltage		V _{CC} =4.75V V _I =0.6, V _I =2V	I _{OL} =24mA		0.35	0.5	٧
			VI=0.6, VI=2V	I _{OL} =48 mA		0.4	0.5	٧
		A, B	5 051/ 1/ 0			,	. 20	μΑ
	Liink lavat innut averant	DIR, OC	$V_{CC} = 5.25V, V_I = 2.7V$				20	μΑ
UH ·	High-level input current	A, B	V _{CC} =5.25V, V _I =5.	5V			0.1	mΑ
	* *	DIR, OC	V _{CC} =5.25V, V _I =10V				0.1	mA
lıL	Low-level input current		$V_{CC} = 5.25V, V_I = 0.$.4V			-0.4	mA
Госн	Supply current, all outputs high		$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$			48	70	mA
ICCL	Supply current, all outputs low		$V_{CC}=5.25V$, $V_1=0V$, $V_1=4.5V$			62	90	mA
locz .	Supply current, all outputs off		V _{CC} =5.25V, V _I =0\	V, V ₁ = 4.5V		64	95	mA

^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25$ °C

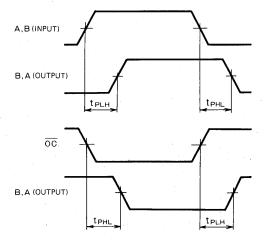
SWITCHING CHARACTERISTICS (V_{CC}=5V. Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Tost conditions	Limits			11.	
Symbol	rarameter		Test conditions	Min	Тур	Max	Unit
•	Low-to-high-level output propagation time	From input A to output B			20	25	
tpLH		From input B to output A			20	25	ns
+	t PHL High-to-low level output propagation time	From input A to output B			15	25	ns
¹ PHL		From input B to output A		* *	15	25	113
+	Low-to-high level output	From input OC to output A	$C_L=45pF$, $R_L=667 \Omega$ (Note 2)		25	40	
¹ PLH	PLH propagation time	From input OC to output B			25	40	ns
		From input OC to output A	÷		30	50	
^L PHL		From input OC to output B			30	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_0 = 50 Ω .
- (2) C_L includes probe and jig capacitance.



MITSUBISHI LSTTLS M74LS642P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

DESCRIPTION

The M74LS642P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA)
- Wide operating temperature range. ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

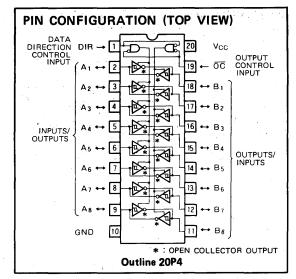
FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with inverted output open collectors are connected together to form bi-directional buffers.

The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

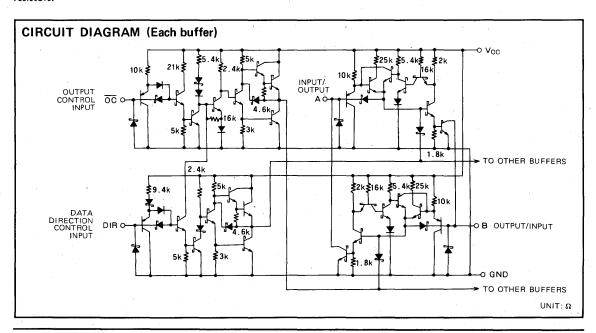
When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin. When output control input \overline{OC} is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.



The functions and pin connections of this IC are identical to those of M74LS640P.

A device, M74LS642-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	ō	I
L	н	, I	ō
Н	×	н	H

Note 1: 1: Input pin

0: Output (inverted output) pin

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter Supply voltage		Conditions	Limits	Unit
Vcc				-0.5~+7	V
	A, B			-0.5~+7	V
Vi	/I Input voltage DIR, OC	DIR, OC		-0.5~+15	V
V ₀	Output voltage		High-level state	-0.5~+7	V
Topr	Operating free-air ambie	ent temperature range		-20~+75	င
Tstg	Storage temperature ran	nge		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

C	Paran	neter		Limits			
Symbol	raidi				Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V ₀ =5.5V	0		100	μА	
	IoL Low-level output current	V _{OL} ≤0.4V	0	-	12	mA	
IOL		V _{OL} ≤0.5∨	0		24	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

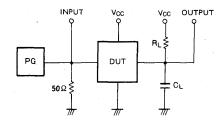
Comptend	Parameter		Test cond		Limits			Unit		
Symbol	raramet	er	rest cond	ittions	Min	Typ *	Max	Unit		
V _{IH}	High-level input voltage				2			V		
VIL	Low-level input voltage						0.6	V		
VT + - VT -	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V		
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	18 mA			- 1.5	V		
Гон	High-level output current	$V_{CC} = 4.75V, V_1 = 0.6V, V_1 = 2V, V_{OH} = 5.5V$				100	μА			
VoL	Low-level output voltage		V _{CC} =4.75V I _{OL} =12mA		V _{CC} =4.75V I _{OL} =12mA			0.25	0.4	V
	Low-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OL} =24 mA		0.35	0.5	V		
		A, B	V _{CC} =5.25V, V _I =2.7V				20	μΑ		
	III b lavel to a control of	DIR, OC					20	μА		
Iн	High-level input current	A, B	V _{CC} =5.25V, V _I =5.5	5V .			0.1	mA		
		DIR, OC	$V_{CC} = 5.25V, V_{\parallel} = 10V$				0.1	mΑ		
l _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4	4 V			-0.4	mA		
Гссн	Supply current, all outputs high $V_{CC} = 5.25V$, $V_I = 0V$, $V_I = 4.5V$, V _I = 4.5V		48	70	mA .			
ICCL	Supply current, all outputs lo	low $V_{CC} = 5.25V, V_1 = 0V, V_1 = 4.5V$		$V_{CC} = 5.25V, V_{I} = 0V, V_{I} = 4.5V$		62	90	mA		
locz	Supply current, all outputs off $V_{CC}=5.25V$, $V_1=0V$, $V_1=4.5V$			64	95	mA				

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.

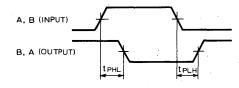
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

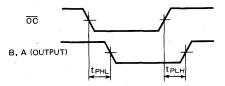
0	Parameter			Limits			Linit
Symbol			Test conditions	Min	Тур	Max	Unit
Tau I	Low-to-high level output	From input A to output B			16	25	
¹ PLH	propagation time	From input B to output A			16	25	ns
	t PHL High-to-low level output propagation time	From input A to output B			14	25	ns
LPHL		From input B to output A	C _L =45pF, R _L =667 Ω		14	25	
•	Low-to-high level output	From input OC to output A	(Note 2)		25	40	
^L PLH	PLH propagation time High-to-low level output propagation time	From input OC to output B			. 25	40	
+		From input OC to output A			30	60	
1 PHL		From input OC to output B			30	60	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P.p., Z_O = 50Ω
 (2) C_L includes probe and jig capacitance.





DESCRIPTION

The M74LS642-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with open collector inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (IOL = 48mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

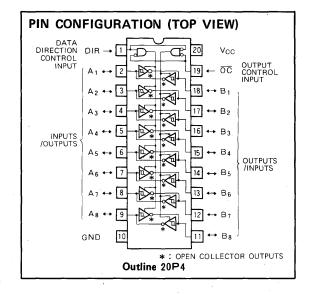
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

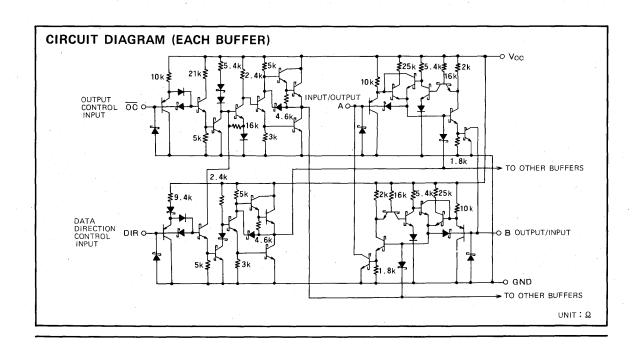
In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with open collector inverted outputs are made two-way buffers.

The input/output A and output/input B sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When \overline{OC} is high, both A and B are high and A and B are isolated.



The functions and pin connections of this device are identical to those of M74LS640-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.



FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	ō	I
·L	н	ı	ō
Н	X	н	н

Note 1: | : Input pin

0: Output (inverted) pin

X : Irrelevant

MAXIMUM ABSOLUTE RATINGS ($Ta = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

Symbol	Pa	rameter	Conditions	Limits	Unit
Vcc	Supply voltage			-0.5~+7	V
.,,		A, B		-0.5~+7	V
Vi	Input voltage DIR, O	DIR, OC		-0.5~+15	V
Vo	Output voltage		High-level state	-0.5~+7	V
Topr	Operating free-air ambie	nt temperature range		-20~+75	ာ
Tstg	Storage temperature ran	ge		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

			Unit			
Symbol	, Pa	Parameter			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧.
Гон	High-level output current	V ₀ =5.5V	0		100	μΑ
	Low lovel output avenue	V _{OL} ≦0.4V	0		12	mA
lor	Low-level output current	V _{OL} ≦0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

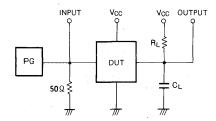
Symbol	Parameter		Task condit	Test conditions		Limits		
Symbol	raramet	ei 	l est condi	tions	Min	Тур 🛊	Max	Unit
VIH	High-level input voltage				2	1		V
VIL	Low-level input voltage						0.6	V
T + -VT-	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18 mA			- 1.5	V
Ioн ·	High-level output current		V _{CC} = 4.75V, V _I = 0.6V, V	$V_1 = 2V, V_0 = 5.5V$			100	μА
		V 4.75V	I _{OL} =12mA		0.25	0.4	٧	
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	٧
			V ₁ =0.6V, V ₁ =2V	I _{OL} =48mA		0.4	0.5	V
	A. B		V 5 05V V 0 3	V 5.05V V 0.7V			20	μА
	Other treatment and accommon	DIR, OC	V _{CC} =5.25V, V _I = 2.7	$V_{CC} = 5.25V, V_I = 2.7V$			20	μА
Чн	High-level input current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I = 10	V _{CC} =5.25V, V _I =10V			0.1	mA
IIĻ	Low-level input current		V _{CC} =5.25V, V _I = 0.4	V _{CC} =5.25V, V _I =0.4V			-0.4	mΑ
Госн	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V	, V _I = 4.5V		48	70	mΑ
ICCL	Supply current, all outputs lov	v	$V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V$			62	90	mA
Iccz	Supply current, all outputs off		$V_{CC} = 5.25V, V_1 = 0V, V_1 = 4.5V$			64	95	mA

 $[\]star$: All typical values are at $V_{CC} = 5V$, $Ta = 25 ^{\circ}C$

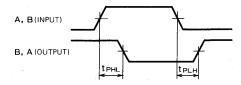
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

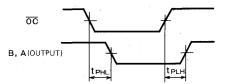
Symbol	Parameter		Test conditions	Limits			Unit
Symbol			lest conditions	Min	Тур	Max	Unit
Low-to-high-level output	From input A to output B			16	25		
[™] PLH	propagation time	From input B to output A	,		16	25	ns
	t PHL High-to-low level outpout propagation time	From input A to output B		•	14	25	
1 PHL		From input B to output A	0 45-5 8 667.0 (Nov. 2)		14	25	ns
•	Low-to-high level output	From input OC to output A	C _L =45pF, R _L =667 Ω (Note 2)		25	40	
t _{PLH}	propagation time	From input OC to output B			25	40	ns
1	High-to-low-level output propagation time	From input OC to output A			30	60	
PHL		From input OC to output B			30	60	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 $V_{P,P}$, Z_O = 50 Ω .
- (2) C_L includes probe and jig capacitance.





DESCRIPTION

The M74LS643P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

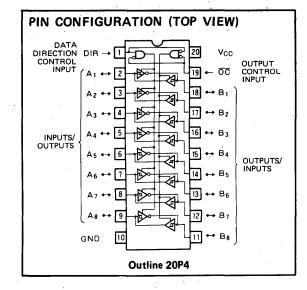
The inputs and outputs of the two buffer circuits with 3state outputs are connected together to form bi-directional buffers.

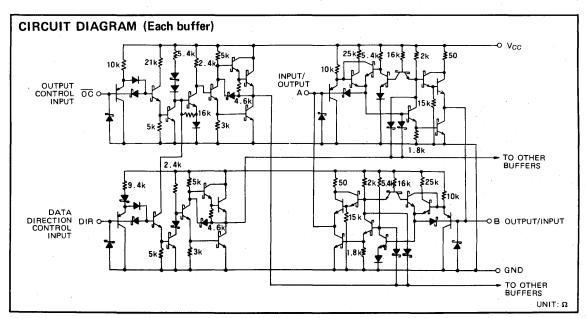
The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin.

When output control input \overline{OC} is high, both A and B are put in the high-impedance state so the buffers are isolated.

A device, M74LS643-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.





FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	0	ı
L	н	ı	ō
Н	×	Z	Z

Note 1: I: Input pin

O: Output (non-inverted output) pin

O: Output (inverted output) pin

Z: High impedance (A, B separated) X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit	
Vcc	Supply voltage		upply voltage		V	
V _I Input voltage	A, B		-0.5~+5.5	V		
	DIR, OC	·	-0.5~+15	V		
Vo	Output voltage		Off state	-0.5~+5.5	V	
Topr	Operating free-air ambi	ent temperature range		-20~+75	ဗ	
Tstg	Storage temperature ra	nge		-65~+150	° °C	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{C}$, unless otherwise noted)

Symbol	Para made		Limits			
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
1.	High-level output current	V _{OH} ≥2.4V	0		-3	mA .
Гон	i riigii-level output current	V _{OH} ≧ 2 V	0		15	mA
1	Low-level output current	V _{OL} ≤0.4V	0		12	mA
IOL	Low-level output current	V _{0L} ≤0.5V	0		24	′ mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \degree$, unless otherwise noted)

Symbol	Parameter		Test condi	tions	Limits			1.1-24
Symbol	rarameter		rest condi	LIONS	Min	Typ *	Max	Unit
ViH	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.6	. V
VT+ -VT-	Hysteresis width		V _{CC} =4.75V		0.2	0.4	1	V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			-1.5	V
.,			h-level output voltage V _{CC} =4.75V I _{OH} = - 3 mA		2.4	3.4		- V
VoH	High-level output voltage		V _I =0.6V, V _I =2V I _{OH} =-15mA		2			V
			V _{CC} =4.75V			0.25	0.4	V
VoL	Low-level output voltage					0.35	0.5	V
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V	$V_1 = 2V, V_0 = 2.7V$. 20	μА
lozL	Off-state low-level output curre	ent	V _{CC} =5.25V, V _I =0.6V	$V_1 = 2V_1 V_0 = 0.4V$			-400	μА
		A, B		V 5 05V V 0 3V			20	μА
	Little Lauret Communication	DIR, OC	$V_{CO} = 5.25V, V_{I} = 2.7$	' .			20	μА
Тін	High-level input current	A, B	V _{CC} =5.25V, V _I =5.5	V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10V				0.1	mA
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.4	V			-0.4	mA
los	Short-circuit output current (N	ote 2)	te 2) V _{CC} =5.25V, V _O =0V		-40		- 225	mA
Icch	Supply current, all outputs hig	1	V _{CC} =5.25V, V _I =0V, V _I =4.5V			48	70	mA
IccL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V, V _I =4.5V			62	90	mA
Iccz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V,	V _I =4.5V		64	95	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

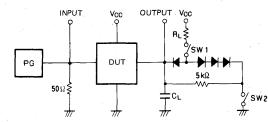
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

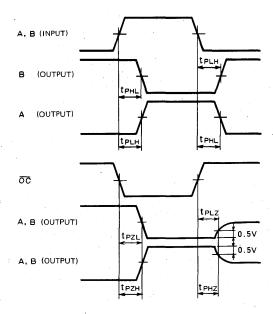
O mark at			Test conditions	Ĭ	Limits		
Symbol	Par	ameter	Test conditions	Min	Тур	Max	Unit
	Low-to-high level output	From input A to output B			8	10	
t _{PLH}	propagation time	From input B to output A	C _L =45pF (Note 3)		8	10	ns
	High-to-low level output	From input A to output B			12	15	
t _{PHL}	propagation time	From input B to output A			12	15	ns
	Low suspens spekla since	From input OC to output A		25	25	40	ns
tezL	Low output enable time	From input OC to output B	$R_L = 667\Omega$ $C_L = 45pF$		25	40	
	High output cookin time	From input OC to output A	(Note 3)		23	40	ns
t _{PZH}	High output enable time	From input OC to output B	1		23	40	115
	l ou autout disable time	From input OC to output A			17	25	ns
t _{PLZ}	Low output disable time	From input OC to output B	R _L =667Ω C _L =5pF		17	25	115
	High output disable time	From input OC to output A	(Note 3)		19	25	200
t _{PHZ}	I fight output disable title	From input OC to output B]		19	25	ns

Note 3: Measurement circuit



	Parameter	SW 1	SW2
	· t PZH	Open	Closed
	t PZL	Closed	Open
	t PLZ	Closed	Closed
,	t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, Vp = 3Vp.p, Z_O = 50Ω
 (2) All diodes are high speed switching diodes
- t_{rr} ≤ 4ns).
 C_L includes probe and jig capacitance.



M74LS643-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS643-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

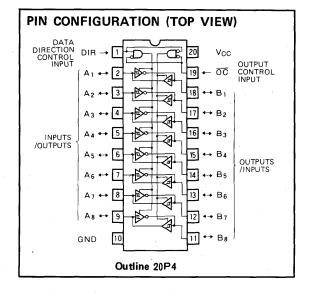
General purpose, for use in industrial and consumer equipment.

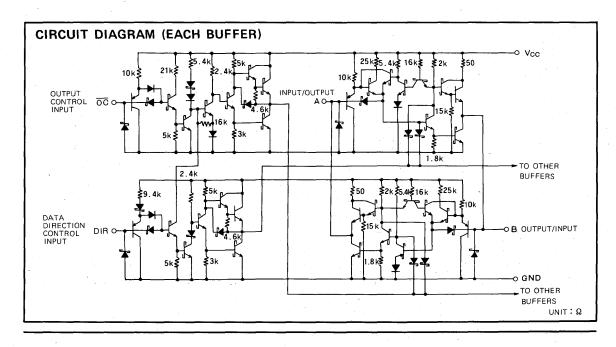
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are mutually connected and the buffers with non-inverted outputs and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When output control input \overline{OC} is high, both A and B are put in the high-impedance state and A and B are isolated.





FUNCTION TABLE (Note 1)

ōc	DIR	. А	В
L	L L	0	
L	Н	, 1	ō
Н	Х	Z	Z

Note 1: | : Input pin

O: Output (non-inverted) pin

O : Output (inverted) pin

Z: High-impedance (A, B are isolated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 ^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V _{CC}	Supply voltage			-0.5~+7	V
.,	Input voltage	A, B		-0.5~+5.5	V
Vi	input vortage	DIR, OC		-0.5~+15	V
Vo	Output voltage		Off-state	-0.5~+5.5	V
Topr	Operating free-air ambient ter	nperature range		-20~+75	°C
Tstg	Storage temperature range			−65∼ + 150	°C

RECOMMENDED OPERATING CONDITIONS (T $a = -20 \sim +.75$ °C, unless otherwise noted)

Symbol	Paramete	Donner atom		Limits			
Symbol	Faraniete		Min	Тур	Max	Unit	
Voc	Supply voltage		4.75	5	5.25	V	
1	High-level output current	V _{OH} ≥2.4V	0		-3	mA	
(он	Ingri-level output current	V _{OH} ≥ 2 V	0		15	mA	
i		V _{OL} ≤0.4V	0		12	mA	
OL	Low-level output current VoL≤0.5V		0		48	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 \,^{\circ}$ C, unless otherwise noted)

Symbol	Dore	Parameter Test conditions				Limits		Unit
Symbol	Para	ameter	l est condit	tions	Min	Тур 🛊	Max	Unit
VIH	High-level input voltage							V
VIL	Low-level input voltage						0.6	V
VT+-VT-	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			~ 1.5	V
.,	District of Assistance		V _{CC} =4.75V	I _{OH} = -3mA	2.4	3.4		V
Voн	High-level output voltage		$V_1 = 0.6V, V_1 = 2V$	I _{OH} = - 15mA	. 2			V
		,		I _{OL} =12mA		0.25	0.4	V
VOL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	V
			$V_1 = 0.6V, V_1 = 2V$	I _{OL} =48 mA		0.4	0.5	V
lozн	Off-state high-level outpu	t current	V _{CC} = 5.25V, V ₁ = 0.6V	$V_1 = 2V, V_0 = 2.7V$			20	μΑ
lozL	Off-state low-level output	current	$V_{CC} = 5.25V, V_1 = 0.6V,$	$V_1 = 2V$, $V_0 = 0.4V$			-400	μА
	4.	А, В	V 5 05V V 0.3				20	μА
. }	High-level input current	DIR, OC	$V_{CC} = 5.25V, V_1 = 2.7$	' V			20	μΑ
ЧΗ	riign-level input current	A, B	V _{CC} =5.25V, V ₁ =5.5	V .			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I = 10 ⁴	V			0.1	mA
I _I L	Low-level input current		V _{CC} =5.25V, V _I =0.4	V			-0.4	mA.
los	Short-circuit output curre	ent (Note 2)	V _{CC} =5.25V, V _O = 0	V	- 40		- 225	mA
Гссн	Supply current, all outpu	ts high	$V_{CC} = 5.25V, V_I = 0$	/, V _I = 4.5V		48	70	mA
ICCL	Supply current, all outpu	ts low	V _{CC} =5.25V, V _I = 0 \	/, V _I = 4.5V		62	90	mΑ
locz	Supply current, all outpu	ts off	V _{CC} =5.25V, V _I = 0 V	$V_1 = 4.5V$		64	95.	mA

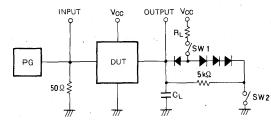
^{* .:} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

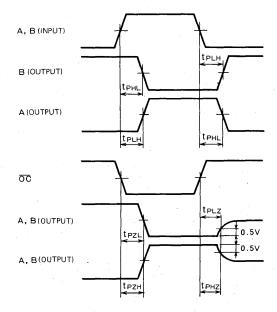
Symbol	D		T		Limits		
Symbol	Par	Parameter Test conditions		Min	Тур	Max	Unit
	Low-to-high-level output	From input A to output B			8	10	
tpLH	propagation time	From input B to output A	C _L =45pF (Note 3)		8	10	ns
	High-to-low level output	From input A to output B			12	15	
t PHL	propagation time	From input B to output A			12	15	ns
	Low-level output enable	From input OC to output A			25	40	
t _{PZL}	time	From input \overline{OC} to output B	D 5570 0 45 F (Note 2)		25	40	ns
	High-level output enable	From input OC to output A	$R_L = 667\Omega$ $C_L = 45pF$ (Note 3)		23	40	ns
t _{PZH}	time	From input $\overline{0C}$ to output B			23	40	"
	Low-level output disable	From input OC to output A			17	25	ns
t _{PLZ}	time	From input OC to output B	R _L =667Ω C _L =5pF (Note 3)		17	25	115
	High-level output disable	From input OC to output A			19	25	ns
t _{PHZ}	time .	From input OC to output B			19	25	118

Note 3: Measurement circuit



Symbol	SW 1	SW2
t PZH	Open	Closed
t _{PZL}	Closed	Open
t PLZ	Closed	Closed
t PHZ	Closed	Closed

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) All diodes are switching diodes (t_{ff} ≤ 4ns).
- (3) C_L includes probe and jig capacitance.



MT4LS644P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS644P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted, non-inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA)
- Wide operating temperature range. $(T_a = -20 \sim +75^{\circ}C)$

APPLICATION

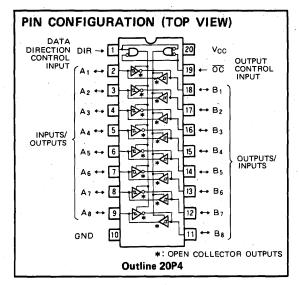
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The inputs and outputs of the buffer circuits with open collector outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

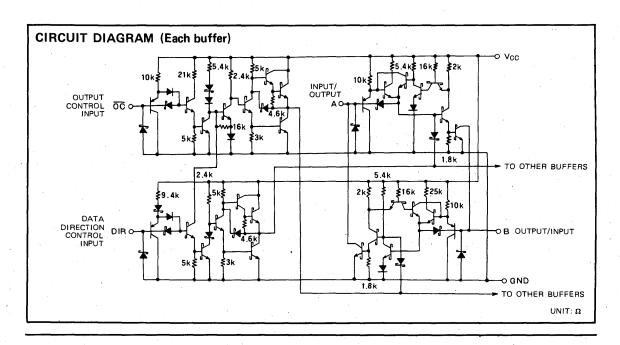
When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin. When output control input \overline{OC} is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.



The functions and pin connections of this IC are identical to those of M74LS643P.

A device, M74LS644-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L	L	0	1
L	H	1	ō
Н	х	н	н

Note 1: 1: Input pin

O: Output (non-inverted output) pin

O: Output (inverted output) pin

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \text{ C}$, unless otherwise noted)

Symbol	Par	ameter	Conditions		Limits	Unit
Voc	Supply voltage				· - 0.5 ~ + 7	V
Vı	Input voltage	A, B			−0.5∼+7	V
VI.	Impat vortage	DIR, OC			-0.5~+15	V
Vo	Output voltage		High-level state		-0.5~+7	, v
Topr	Operating free-air ambi	ent temperature range			−20∼ +75	*C ·
Tstg	Storage temperature ra	nge		1	-65~+150	,c

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Paramete			Limits		Unit
Symbol	yriboti		Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V ₀ =5.5V	0		100	μА
	Low-level output current	V _{OL} ≤0.4V	0		12	mΑ
IOL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 ^{\circ}C$, unless otherwise noted)

Symbol	Paramet	-	Test con-	alia!		Limits		Unit
39111001	raramet	er .	l est con	artions	Min	Typ *	Max	Unit
V _{IH}	High-level output voltage				2			V
VIL	Low-level output voltage						0.6	V
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	-18mA			-1.5	V
Гон	High-level output current		V _{CC} =4.75V, V _I =0.6V,V _I =2V,V _O =5.5V				100	μΑ
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
	Low-level output voltage		$V_1 = 0.6 V, V_1 = 2 V$	I _{OL} =24mA		0.35	0.5	٧
	*	A, B	V 5 05V V 0	7.7			20	μА
	Libe to at the continues.	DIR, ÖÖ	$V_{CC}=5.25V, V_{I}=2.$	''			20	μА
Чн	High-level input current	A, B	V _{CC} =5.25V, V _I =5.	5V			0.1	mA
		DIR, OC	V _{CC} =5.25V, V _I =10	V			0.1	mA
I _{IL}	Low-level input current		V _{CC} =5.25V, V _I =0.	4V			-0.4	mA
Госн	Supply current, all outputs h	igh	V _{CC} =5.25V, V _I =0,V	, V _I =4.5V		48	. 70	mA
IccL	Supply current, all outputs id	ow .	V _{CC} =5.25V, V _I =0V	/, V _I =4.5V		62	90	mA
Iccz	Supply current, all outputs o	ff	V _{CC} =5.25V, V _I =0V	/, V _I =4.5V		64	95	mΑ

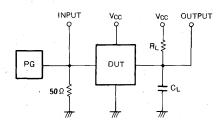
^{* :} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$.

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

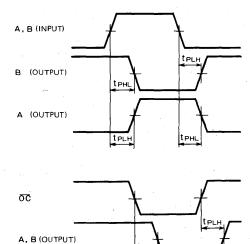
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

		ameter	Test conditions		Limits	-	Unit
Symbol	Par	ameter	rest conditions	Min	Тур	Max	Unit
• _	Low-to-high level output	From input A to output B			16	25	
1 PLH	t PLH propagation time	From input B to output A			20	25	ns
	High-to-low level output	From input A to output B			14	25	
t _{PHL} •	propagation time	From input B to output A	C _L =45pF, R _L =667Ω		15	25	ns
	Low-to-high level output	From input OC to output A	- CL=45βF, NL=667Ω		25	40	
t _{PLH}	propagation time	From input OC to output B	(Note 2)		25	40	ns
	High-to-low level output	From input OC to output A	1		30	60	
t _{PHL}	propagation time	From input OC to output B	•		30	50	ns

Note 2: Measurement circuit



- The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
 C_L includes probe and jig capacitance.



M74LS644-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS644-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with open collector inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output
 A and output/input B
- High fan-out (I_{O L} = 48mA)
- Wide operating temperature range (T_a = −20~+75°C)

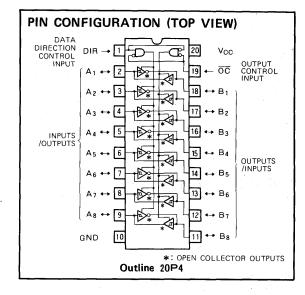
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

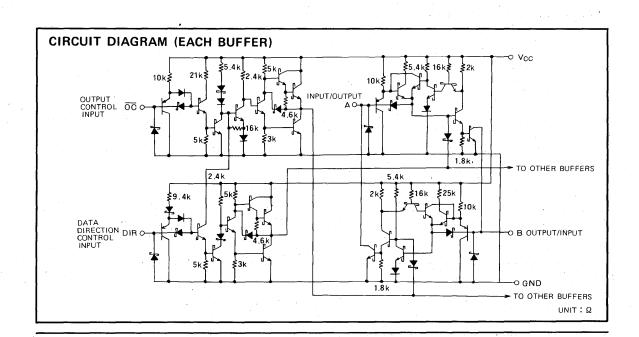
In this device the inputs and outputs are connected mutually and the buffers with open collectors inverted outputs and the buffers with the non-inverted outputs are made two-way buffers, the input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and



A the output pin. When \overline{OC} is high, both A and B are high, and A and B are isolated.

The functions and pin connections of this device are identical to those of M74LS643-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

ōc	DIR	Α	В
L ,	L	0	1
L	Н	1	ō
н .	×	н	Н

Note 1: 1: Input pin

O: Output (non-inverted) pin

O : Output (inverted) pin

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
Voc	Supply voltage			-0.5~+7	٧
V 1	A, B		-0.5~+7	V	
Vi	Input voltage	DIR, OC		-0.5~+15	V
Vo	Output voltage		High-level state	-0.5~+7	. V
Topr	Operating free-air ambie	nt temperature range		-20~+75	°C
Tstg	Storage temperature range			-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75$ °C, unless otherwise noted)

			Limits .			Unit	
Symbol	Parameter		Min	Тур	Max	Oint	
Vcc	Supply voltage		4.75	5	5.25	V	
Іон	High-level output current	V ₀ =5.5V	0		100	μА	
		V _{OL} ,≤0.4V	0		100 μA 12 mA	mA	
loL	Low-level output current	V _{OL} ≦0.5V	0		48	mA	

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75^{\circ}C$, unless otherwise noted)

2.4.				16.2		Limits		Unit	
Symbol	Parameter	•	J est co	nditions	Min	Тур 🗱	Max	Onit	
VIH	High-level input voltage	High-level input voltage			2			٧	
VIL	Low-level input voltage						0.6	V	
V _{T+} -V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		٧	
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =	— 18 mA			-1.5	V	
Joн	High-level output current		V _{CC} =4.75V, V _I =0.	6V, V1=2V, V0=5.5V			100	μА	
			V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4		
VoL	Low-level output voltage		$V_{i}=0.6V, V_{i}=2V$	I _{OL} =24mA		0.35	0.5	٧	
		. 4	VI-0.0V, VI-2V	I _{OL} =48mA		0.4	0.5	V	
		A, B	V _{CC} =5.25V, V _I =2	7\/			20	μА	
1	High-level input current	PIR, OC	V _{CC} =5.25V, V _j =2	./٧			20	μА	
l IH	mgariever impor current	A, B	V _{CC} =5.25V, V _I =5	.5V			0.1	mA	
		DIR, OC	V _{CC} =5.25V, V _I =1	0V	1		0.1	mA	
l ₁ L	Low-level input current		V _{CC} =5.25V, V _I =0	.4V			-0.4	mA	
Icch	Supply current, all outputs high		V _{CC} =5.25V, V _I =0	V, V _I =4.5V		48	70	mA	
I _{COL}	Supply current, all outputs low		$V_{CC} = 5.25V, V_{I} = 0V, V_{I} = 4.5V$			62	90	mA	
I _{CCZ}	Supply current, all outputs off		V _{CC} =5.25V, V _I =0	V, V _I =4.5V		64	95	mA	

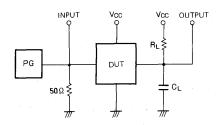
st : All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

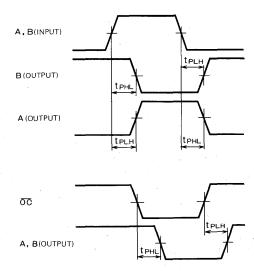
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Paran		Test conditions		Limits		Unit
39111001	l didi	ie (ei	rest conditions	Min	Тур	Max	Unit
+	t PLH Low-to-high-level output propagation time	From input A to output B			16	25	,
' PLH		From input B to output A			20	25	ns
+	High-to-low level output	From input A to output B			14	25	
t _{PHL}	propagation time	From input B to output A	$C_1 = 45 pF$, $R_1 = 667 \Omega$ (Note 2)		15	25	ns
+	Low-to-high level outpout	From input OC to output A	CL=45PF, AL=667 92 (Note 2)		25	40	
t _{PLH}	propagation time	From input OC to output B			25.	40	ns
+	High-to-low-level outpout	From input OC to output A	,		30	60	
t _{PHL}	propagation time	From input OC to output B		,	30	50	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω .
- (2) C_L includes probe and jig capacitance.



DESCRIPTION

The M74LS645P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/ output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

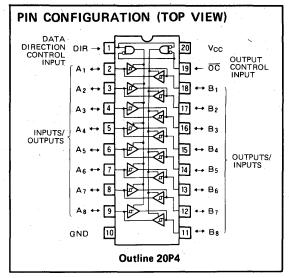
FUNCTIONAL DESCRIPTION

The inputs and outputs of the buffer circuits with 3-state outputs are connected together to form bi-directional buffers.

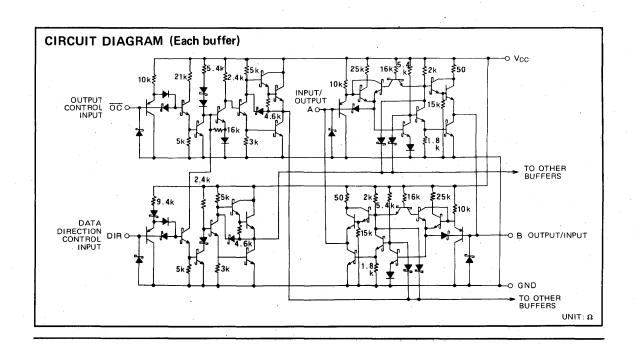
The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin.

When output control input \overline{OC} is high, both A and B are put in the high-impedance state so the buffers are isolated.



A device, M74LS645-1P, having the same pin connections and functions except the value of I_{OL} (=48mA) has been provided.



FUNCTION TABLE (Note 1)

ŌĊ	DIR	Α	В
L	L	0	ł
L	н	t	0
Н	×	Z.	Z

Note 1: 1: Input pin

O: Output (non-inverted output) pin .

Z: High impedance (A, B separated)

X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

Symbol	Parame	eter	Conditions			Limits	Unit
Vcc	Supply voltage	<u> </u>				-0.5~+7	· v
	Input voltage	A, B				$-0.5 \sim +5.5$	V
VI	Input voltage	DIR, OC	-			-0.5~+15	- V
Vo	Output voltage		Off state			-0.5~+5.5	. V
Topr	Operating free-air ambient				−20~+75	င	
Tstg	Storage temperature range					-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

S	P	- '		Limits	Limits	
Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply voltage	•	4.75	5	5.25	V
	High-level output current	V _{OH} ≥ 2.4 V	0		-3	mA
Іон	nigh-level output current	V _{OH} ≧ 2V	0		— 15	mA.
		V _{OL} ≤ 0.4 V	0		12	mΑ
10L	Low-level output current	V _{OL} ≤ 0.5V	0		24	mΑ

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 ^{\circ}$, unless otherwise noted)

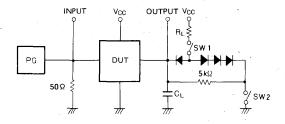
Symbol	Ь	'arameter	Test cond	litions		Limits		Unit
Symbol .	,	arameter	r est conc	ittions	Min	Typ *	Max	OIIII
VIH	High-level input voltag	е			2			V
VIL	Low-level input voltage	е					0.6	٧.
/ _{T+} - V _{T-}	Hysteresis width		V _{CC} = 4.75V		0.2	0.4		٧
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	V
\/	Mark the second		V _{CC} =4.75V	I _{OH} = -3mA	2.4	3.4		V
V _{OH} High-level output voltag	age	$V_1 = 0.6 V, V_1 = 2 V$	I _{OH} = - 15mA	2			V	
V _{OL} Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧	
	19e	$V_1 = 0.6V, V_1 = 2V$	I _{OL} =24mA		0.35	0.5	V	
lozh	Off-state high-level output current		$V_{CC} = 5.25V, V_i = 0.6V$, V _I = 2V , V ₀ = 2.7V		. :	20	μΑ
lozL	Off-state low-level out	put current	$V_{CC} = 5.25V, V_1 = 0.6V$	$V_1 = 2V, V_0 = 0.4V$			- 400	μΑ
		A, B		V _{GG} = 5.25 V, V _I = 2.7 V			20	μА
1	High-level input	DIR, OC	VCC= 5.25V, VI = 2.1	/ V			· 20	V V V V V V µА µА µА mA mA mA
Iн	current	А, В	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	$V_{CC} = 5.25V, V_i = 10^{\circ}$	V			0.1	mΑ
HL	Low-level input currer	nt	V _{CC} =5.25V, V _I =0.4	ıv			-0.4	mA
los	Short-circuit output current (Note 2)		V _{CC} =.5.25V, V _O = 0	v	-40		- 225	mA
Гссн	Supply current, all out	butputs high $V_{CC} = 5.25V$, $V_I = 0 V$, $V_I = 4.5V$			48	70	mA	
ICCL	Supply current, all out	pus low	V _{CC} =5.25V, V _I = 0 V	$V_{CC} = 5.25 \text{V}, \ V_{I} = 0 \text{ V}, \ V_{I} = 4.5 \text{V}$		62	90	mΑ
Iccz	Supply current, all out	puts off	V _{CC} =5.25V, V _I = 0 V	V, V ₁ = 4.5V		64	95	mA

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C. Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, Ta = 25°C, unless otherwise noted)

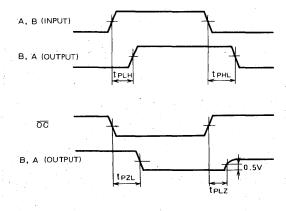
Symbol	00	rameter	Test conditions	-	Limits		
Symbol	, ra	i ameter	rest conditions	Min	Тур	Max	Unit
•	Low-to-high level output	From input A to output B			12	15	1_1
t _{PLH}	propagation time	From input B to output A	$C_1 = 45 pF$ (Note 3)		12	. 15	ns
+_	High-to-low level output	From input A to output B	CL=45pF (Note 3)		12	15	ns
t PHL propagation	propagation time	From input B to output A			12	15	
	Low output enable time	From input OC to output A	itput A		25	40	
t _{PZL}	Low output enable time	From input OC to output B	R _L =667Ω, C _L =45pF		25	40	ns
+_	High outputenable time	From input OC to output A	(Note 3)		23	40	
t _{PZH}	High outputerlable time	From input OC to output B	(Note 3)		23	40	ns
		From input OC to output A			17	25	
t _{PLZ}	Low output disable time	From input OC to output B	R _L =667Ω, C _L =5pF		17	25	ns
•	Lite and distributed	From input OC to output A	(Note 3)		19	25	
t _{PHZ}	High output disable time	From input OC to output B	(Note 3)		19	25	ns

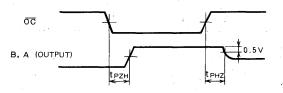
Note 3: Measurement circuit



_			
	Parameter	SW 1	SW2
	t _{PZH}	Open	Closed
	t PZL	Closed	Open
Γ	tPLZ	Closed	Closed
	t _{PHZ}	Closed	Closed

- (1) The pulse generator (PG) has the following the pulse generator (rG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P,P}, Z_O = 50Ω
 All diodes are high speed switching diodes
- (t_{rr} ≤ 4ns).
 (3) C_L includes probe and jig capacitance.





DESCRIPTION

The M74LS645-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

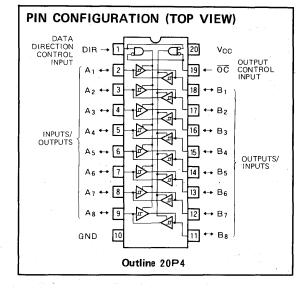
General purpose, for use in industrial and consumer equipment.

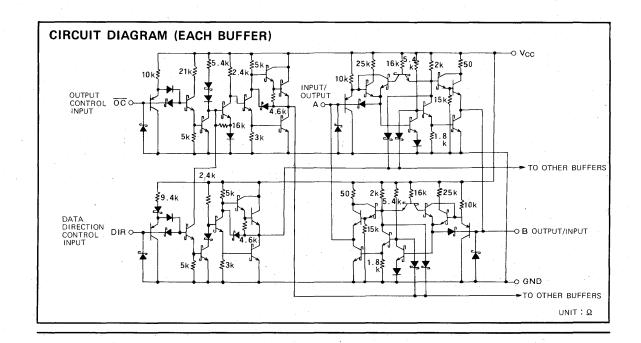
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state non-inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When \overline{OC} is high, both A and B are put in the high-impedance state and A and B are isolated.





FUNCTION TABLE (Note 1)

	ŌC	DIR	A	В
Г	L	· L	0	1-
	L	н	l .	0
	н	X	Z	Z

Note 1: | : Input pin

O: Output (non-inverted output) pin

Z: High impedance (A and B are isolated)

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \,^{\circ}\text{C}$, unless otherwise noted)

Symbol	Para	ameter	Conditions	Limits	Unit	
Vcc	Supply voltage			-0.5~+7	V	
\/.	Input voltage A, B DIR, OC			-0.5~+5.5	.V	
VI				-0.5~+15	V	
Vo	Output voltage		Off-state	-0.5~+5.5	V	
Topr	Operating free-air ambier	nt temperature range		-20~+75	°C	
Tstg	Storage temperature rang	e		−65~ + 150	°C	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ} C$, unless otherwise noted)

	Paramet		Limits			
V _{CC}	Paramet	i aldiletei			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
	High-level output current	V _{OH} ≥ 2.4V	0		-3	mA
ТОН	riigir-level output current	V _{OH} ≧ 2V	.0		-3 -15	mΑ
loL		V _{OL} ≤ 0.4∨	0		12	mA
	Low-level output current	V _{OL} ≤ 0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \, ^{\circ}\text{C}$, unless otherwise noted)

Combal	Parameter		Test conditions		Limits			Unit
Symbol	rarameter		l est congri	tions	Min .	Typ ∗	Max	Onit
VIH	High-level input voltage	: -			2			V
VIL	Low-level input voltage						0.6	· V
V _{T+} - V _{T-}	Hysteresis width		V _{CC} =4.75V		0.2	0.4		V
V _{IC}	Input clamp voltage	4	V _{CC} =4.75V, I _{IC} =-	18mA			- 1.5	٧
	In the second second		V _{CC} =4.75V	I _{OH} = − 3mA	2.4	3.4		V
VoH	High-level output voltage		$V_{I} = 0.6V, V_{I} = 2V$	I _{OH} = - 15mA	2			V
				I _{OL} =12mA		0.25	0.4	٧
VoL	Low-level output voltage		V _{CC} =4.75V	I _{OL} =24mA		0.35	0.5	٧
		*	$V_1=0.6V$, $V_1=2V$	I _{OL} =48mA		0.4	0.5	٧
lozh	Off-state high-level output current		V _{CC} =5.25V, V _I =0.6V, V _I =2V, V _O =2.7V				20	μА
lòzL.	Off-state low-level output current		V _{CC} =5.25V, V _I =0.6V	$V_1 = 2V_1 V_0 = 0.4V$			-400	μΑ
	A, B						20	μΑ
1.	High level in a second	DIR, OC	$V_{CC} = 5.25V, V_{I} = 2.7V$				20	μА
IН	High-level input current	A, B	V _{CC} =5.25V, V _I =5.5	5V			0.1	mA
		DIR, OC	V _{CO} =5.25V, V _I =10V				0.1	mA
l _{IL}	Low-level input current	•	V _{CC} =5.25V, V _I =0.4	4V			-0.4	mA
los	Short-circuit output current (Note 2)	V _{CC} = 5.25V . V _O = 0\	/	40		- 225	mA
Icch	Supply current, all outputs high		V _{CC} =5.25V, V _I =0V	, V _I =4.5V		48	70	mA
IccL	Supply current, all outputs low		V _{CC} =5.25V, V _I =0V	', V _I =4.5V		62	90	mA
locz	Supply current, all outputs off		V _{CC} =5.25V, V _I =0V	', V _I =4.5V		64	95	mA

^{* :} All typical values are at $V_{CC} = 5V$, $Ta = 25^{\circ}C$

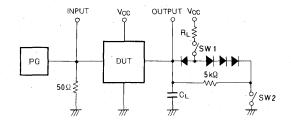
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.



SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

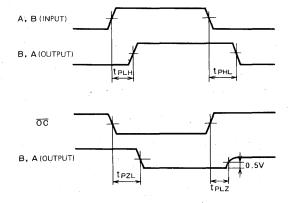
Symbol	Parameter	Total		Limits		11-21	
Symbol	rajanietei		Test conditions	Min	Тур	Max	Unit
	Low-to-high-level output	From input A to output B			12	15	
t _{PLH}	propagation time	From input B to output A	0 - 4575 (Name 2)		12	15	ns
+_	High-to-low level output	From input A to output B	C _L =45pF (Note 3)		12	15	ns
t PHL	propagation time	From input B to output A			12	15	ns
	Low-level output enable	From input OC to output A	ntB		25	40	
tpzL	time	From input OC to output B			25	40	ns
	High-level output enable	From input OC to output A	$R_L=667 \Omega$, $C_L=45 pF$ (Note 3)		23	40	ns
t _{PZH}	time	From input OC to output B			23	40	
+	Low-level output disable	From input OC to output A			17	25	ns
time	time .	From input OC to output B			17	25	
-	High-level outpout disable	From input \overline{OC} to output A	$R_{\perp}=667 \Omega$, $C_{\perp}=5pF$ (Note 3)		19	25	
t _{PHZ} ,	time	From input \overline{OC} to output B	1.		19	25	ns

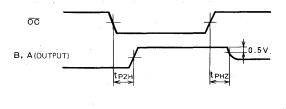
Note 3: Measurement circuit



Symbol	SW 1	SW2		
t _{PZH}	Open	Closed		
t PZL	Closed	Open		
tPLZ	Closed	Closed		
t PHZ	Closed	Closed		

- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}, Z_O = 50\Omega.$ (2) All diodes are switching diodes (t_{rr} ≤ 4ns)
- (3) C_L includes probe and jig capacitance.





M74LS668P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

DESCRIPTION

The M74LS668P is a semiconductor integrated circuit containing a synchronous decade counter function with an up/down control input and preset input.

FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

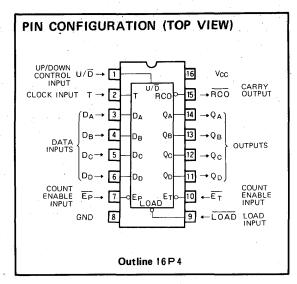
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

Data is also acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D ; and occurs after preset is initiated by dropping load input (LOAD) to a low-level.

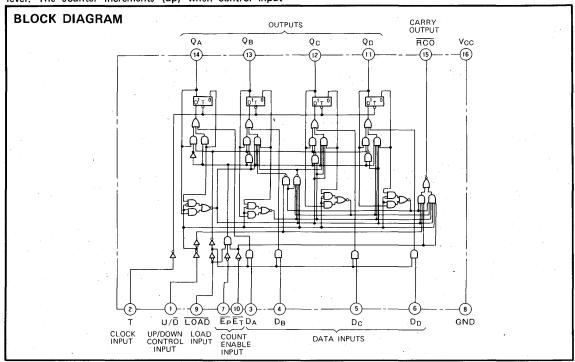
Up/down counter operations are initiated when $\overline{\text{LOAD}}$ is high-level, and the count enable input $(\overline{\text{E}_{P}} \text{ and } \overline{\text{E}_{T}})$ is low-level. The counter increments (up) when control input



 U/\overline{D} is high-level, and decrements (down) at low-level.

Carry output (\overline{RCO}) goes low-level (active) at 9_2 during up counting operations and at O_2 while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a decade counter. (See the application example provided in the back of this specification sheet.)

Counter operations are inhibited when $\overline{\text{LOAD}}$ and $(\overline{\text{E}_{\text{P}}})$ or $\overline{\text{E}_{\text{T}}}$) are all high-level.



FUNCTION TABLE (Note 1)

LOAD	Ε _P	ĒΤ	U/đ	Т	QA	Qв	Qc	QD	RC0 *
L	X	×	X	1	DA	D _B	. D _C	D _D	Н
н	L	L	Н	1		COUNT	UP		н
Н	L	L	L	1		COUNT	DOWN		Н
Н	Н	х	X	X		COUNT	INILIDIT		
Н	×	н .	X	X		COONT	ווסוחוווו		H

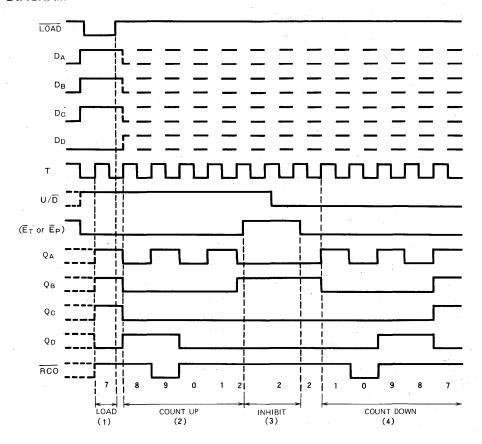
Note 1. 1 : Transition from low to high

X : Irrelevant

Therevant \overline{RCO} is normally at high-level, however, when $\overline{E_T}$ is low and the counter is incrementing, Q_A is high-level, Q_B is center-level, Q_C is low-level, and Q_D is high-level, and \overline{RCO} will go low-level. Also, when the counter is decrementing, Q_A , Q_B , Q_C and Q_D will be low, and \overline{RCO} will also be low.

$$\begin{split} \overline{RCO} &= Q_{A} \cdot Q_{D} \cdot (U/\overline{D}) \cdot \overline{E}_{T} \\ \overline{RCO} &= \overline{Q}_{A} \cdot \overline{Q}_{B} \cdot \overline{Q}_{C} \cdot \overline{Q}_{D} \cdot (\overline{U/\overline{D}}) \cdot \overline{E}_{T} \end{split}$$

TIMING DIAGRAM



Timing diagram notes:

- (1) Preset at 7
- (2) Increment at 8, 9, 0, 1, 2
- (3) Count inhibit
- (4) Decrement at 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 - +75$ °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc .	Supply voltage		0.5~+7	V
Vi	Input voltage '		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Combat	Parameter			Unit		
Symbol	raramet	- arameter			Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
I _{OH}	High-level output current	V _{OH} ≧2.7V	0		-400	μА
loL	Low-level output current	V _{OL} ≤0.4V	0		4	mA
		V _{OL} ≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0	Parameter		Test condition			Limits		Unit
Symbol		rarameter	lest condition	ıs	Min	Тур	Max	Oilit
VIH	High-level input vol	Itage			2			٧
VIL	Low-level input vol	tage					0.8	V
Vic	Input clamp voltag	e	V _{CC} =4.75V, I _{IC} =-18	mA			-1.5	V
VoH	High-level output v	High-level output voltage		$V_{CC} = 4.75V, V_{I} = 0.8V$ $V_{I} = 2V, I_{OH} = -400 \mu A$		3.4		V
\/ -	Low-level output v	eltege	V _{CC} =4.75V	I _{OL} =4 mA		0.25	0.4	V
VOL	Low-level output v	orrage	$V_1 = 0.8V, V_1 = 2V$	I _{OL} =8mA		0.35		٧
		D_A , D_B , D_C , D_D , \overline{E}_P , U/\overline{D}					20	
	High-level input current	T, ET	V _{CC} =5.25V, V _I =2.7V			20	μА	
1		LOAD					40	
LiH .		$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$					0.1	
		T, ET	V _{CC} =5.25V, V _I =10V				0.1	mA
		LOAD	1				0.2	
		D_A , D_B , D_C , D_D , $\overline{E_P}$, U/\overline{D}	`				-0.4	
hi.	Low-level input current	T, ĒT	V _{CC} =5.25V, V _I =0.4V				-0.4	mA
	LOAD	LOAD					-0.8	
108	Short-circuit outpu	t current (Note 2)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
Icc	Supply current		V _{CC} =5.25V (Note 3)			20	34	mA

^{* :} All typical values are at V_{CC} = 5V, T_a = 25°C.



Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. Icc is measured after applying a momentary 4.5V, then ground, to clock input with other inputs grounded and the outputs open.

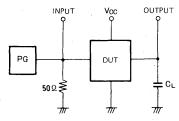
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Constant	D	T		Limits	-	Unit
Symbol fmax tph tph tph tph tph	Parameter	Test conditions	Min	Тур	Max	
fmax	Maximum clock frequency		25	45		MHz
t. _{PLH}	Low-to-high-level, high-to-low-level output propagation			24	40	
t PHL	time, from input T to output RCO			30	60	ns
tpLH	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A , Q_B , Q_C , and Q_D	C _L =15pF (Note 4)		18	27	ns
t _{PHL}				15	27	
tpLH	Low-to-high-level, high-to-low-level output propagation			10	17	ns
t _{PHL}	time, from input E _T to output RCO			24	45	
tpLH	Low-to-high-level, high-to-low-level output propagation			20	35	
t PHL	time, from input U/D to output RCO			20	40	ns

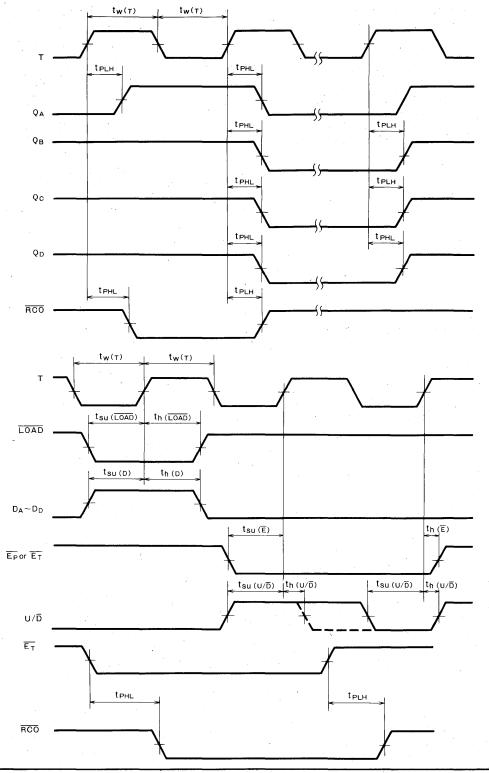
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

C. mah al	Paramatas	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min	Тур	Max	Unit
tw	Clock T pulse width		25	10		ns
tsu(D)	Setup time D _A ∼D _D to T		20	18		ns
t _{su(E)}	Setup time $\overline{E_T}$, $\overline{E_P}$ to T		35	26		ns
tsu(LOAD)	Setup time LOAD to T		25	15		ns
t _{su(U/□)}	Setup time U/D to T		30	20		ns
th	Setup time of all inputs to T		0	-15		ns

Note 4. Measurement circuit

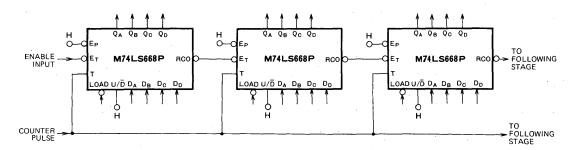


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_t = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P,P}, Z_O = 50Ω.
 (2) C_L includes probe and jig capacitance.



APPLICATION EXAMPLE

10ⁿ counter with cascade connection



M74LS669P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS669P is a semiconductor integrated circuit containing a synchronous 4-bit binary counter function with an up/down control input and preset input.

FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

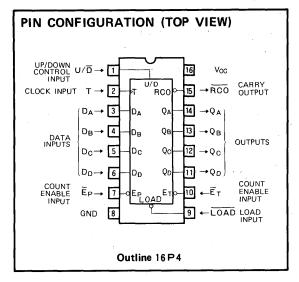
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

Data is acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D ; and occurs after preset is initiated by dropping load input (\overline{LOAD}) to a low-level.

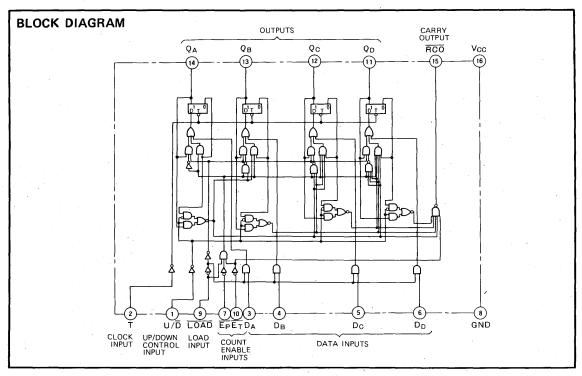
Up/down counter operations are initiated when $\overline{\text{LOAD}}$ is high-level, and the count enable input $(\overline{\text{E}_{P}} \text{ and } \overline{\text{E}_{T}})$ is low-



level. The counter increments (up) when control input U/\overline{D} is high-level, and decrements (down) at low-level.

Carry output (\overline{RCO}) goes low-level (active) at 15₂ during up operations, and at 0₂ while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a binary counter. (See the application example given for M74LS668P.)

Counter operations are inhibited when $\overline{\text{LOAD}}$ and $(\overline{\text{E}_{P}})$ or $\overline{\text{E}_{T}}$) are all high-level.



FUNCTION TABLE (Note 1)

LOAD	ĒР	Ēτ	U/D	Т	QA	QB	Qc	QD	RCO*
,L	Х	×	Х	1	DA	DB	D _C	D _D	Н
Н	L	L	Н	1	COUNT UP			н	
Н	L	L	L	1	COUNT DOWN				Н
Н	· H	х	х	Х		0011117	ALU UDIT		
Н	X	Н	Х	Х	COUNT INHIBIT			"	

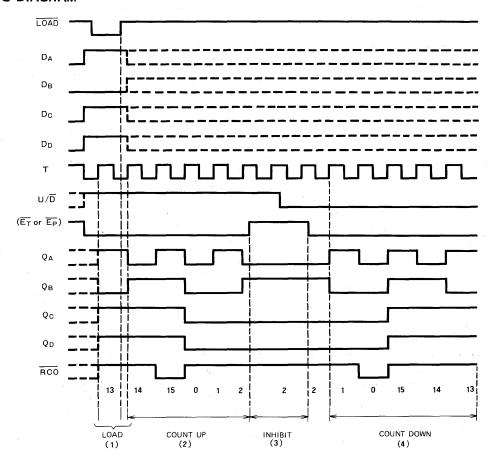
Note 1. 1 Transition from low to high

Irrelevant

Also, when the counter is decrementing, Q_A , Q_B , Q_C and Q_D will be high, and \overline{RCO} will be low. $\overline{RCO} = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot (\underline{U/D} \cdot \overline{E_T})$

 $\overline{RCO} = \overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D (\overline{U/D}) \cdot \overline{E}_T$

TIMING DIAGRAM



Timing diagram notes:

(1) Preset at 13

(2) Increment at 14, 15, 0, 1, 2

(3) Count inhibit

(4) Decrement at 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS ($T_{10} = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V _I	Input voltage		-0.5~+15	V
Vo ·	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Barran	Parameter			Limits			
Symbol	raram	e ter	Min	Тур	Max	Unit		
Vcc	Supply voltage		4.75	5	5.25	V		
Гон	High-level output current	V _{OH} ≧2.7V	- 0		-400	μΑ		
	Low-level output current	V _{OL} ≤0.4V	0		4	mA		
IOL	Low-level output current	0		8	mA			

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test condition			Limits		Unit
39111001		raianicta	. rest conditions	•	Min	Тур	Max	Onit
ViH	High-level input vol	tage			2			V
VIL	Low-level input volt	tage					0.8	٧
Vic	Input clamp voltage		V _{CC} =4.75V, I _{1C} =-18n	ņΑ			-1.5	V
Vон	High-level output vo	oltage	$V_{CC}=4.75V, V_{I}=0.8V$ $V_{I}=2V, I_{OH}=-400\mu A$		2.7	3.4		V
VoL Low-level output vo	altago	V _{CC} =4.75V	IOL=4mA		0.25	0.4	٧	
VOL	Low-level output vo	ntage	V _I =0.8V, V _I =2V	I _{OL} =8mA		0.35	0.5	Ÿ
		D_A , D_B , D_C , D_D , $\overline{E_P}$, U/\overline{D}				-	20	
	High-level input	T, ĒT	$V_{CC}=5.25V, V_{I}=2.7V$			20	μА	
Lie		LOAD				40		
чн	current	D_A , D_B , D_C , D_D , \overline{E}_P , U/\overline{D}					0.1	
		T, ET	$V_{CC}=5.25V, V_I=10V$			0.1	mA	
	,	LOAD					0.2	
		D_A , D_B , D_C , D_D , $\overline{E_P}$, U/\overline{D}					-0.4	
1	Low-level input current	T, ET	$V_{CC}=5.25V, V_{I}=0.4V$	•			-0.4	mA
		LOAD					-0.8	
los	Short-circuit output	Short-circuit output current (Note 2)			-20		—100	mA
loc	Supply current		V _{CC} =5.25V (Note 3)			20	34	mA ·

All typical values are at V_{CC} = 5V, T_B = 25°C.
 Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.
 3. I_{CC} is measured after applying a momentary 4.5V, then ground, to the clock input with all other inputs grounded.

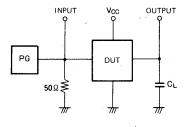
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	. Farameter	l'est conditions	Min	Тур	Max	Unit
f _{max}	Maximum clock frequency		25	30		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output			24	40	
t _{PHL}	propagation time, from input T to output RCO			32	60	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	- -		20	27	
t _{PHL}	time, from input T to outputs Q_A , Q_B , Q_C , and Q_D	C _L = 15pF (Note 4)		15	27	ns
telh	Low-to-high-level, high-to-low-level output			10	17	
t _{PHL}	propagation time, from input $\overline{E_T}$ to output \overline{RCO}			28	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	· .		25	35	
t _{PHL}	time, from input U/D to output RCO		-	20	40	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Unit		
Symbol	r al ametei	rest conditions	Min	Тур	Max	Unit
tw	Clock T pulse width		25	12		ns
tsu(D)	Setup time D _A ~D _D to T		20	18		ns
t _{su(E)}	Setup time $\overline{E_T}$, $\overline{E_P}$ to T		35	26		ns
t su (LOAD)	Setup time LOAD to T		25	15		ns
t _{su (U/D)}	Setup time U/D̄ to T		30	20		ns
th	Setup time of all inputs to T	*	0	- 15		ns

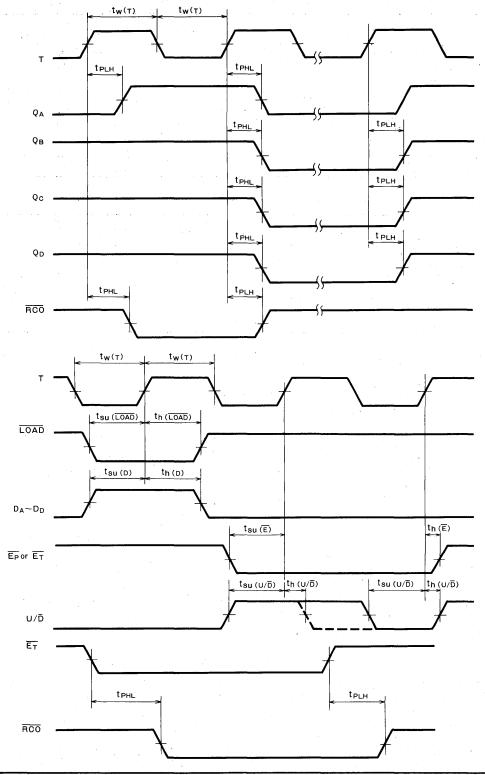
Note 4. Measurement Circuit



- The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_t = 6ns, t_t = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
 C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

· 文山本市新文 [[] () 表现的时间 \$P\$1986



4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS670P is a semiconductor integrated circuit containing a 4 word x 4 bit register file circuit with 3-state outputs.

FEATURES

- Since read address and write address are independent, simultaneous writing and reading of data is possible.
- Provided with read enable input and output control inputs
- Storage capacity can be easily expanded with the aid of the enable input.
- AND-tie may be used (With 3-state output)
 Wide operating temperature range (T_a = -20 ~ +75°C)

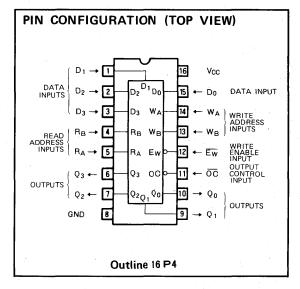
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

16 flip-flops are used as storage devices, and a discrete enable input, address input, and output controlling input are provided for reading and writing. Accordingly, during writing, the contents of other words can be read, and during reading, other words can be written, thereby enhansing to high-speed operation.

The 3-state output permits 128-output AND-tie even in the worst condition. Expansion of up to 512 words is possible. possible.

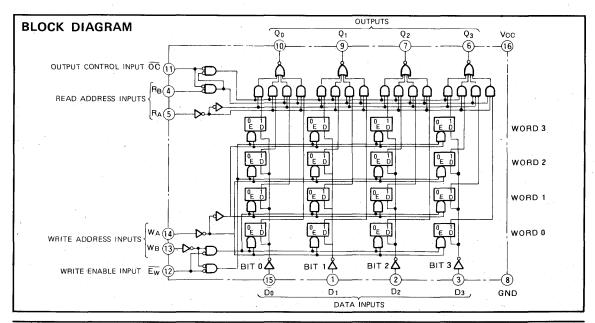


Writing Method

By designating a word using write address inputs W_A and W_B and applying data to the data inputs D_0 , D_1 , D_2 , and D_3 , writing into each bit is performed. For writing the write enable input $\overline{E_W}$ is held low (Writing will not be performed if $\overline{E_W}$ is high)

Readout Method

When a word is designated by read address inputs R_A and R_B , the contents of each bit appear in the outputs Q_0 , Q_1 , Q_2 , and Q_3 . For reading the output control input \overline{OC} is held low. (when \overline{OC} is high, all the outputs are in the high-impedance state).



4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Writing Method

Г.,,	14/	Ēw		W	ord	•
WA	WB	EW	0	1 '	2	3
Х	X	Н	Q ⁰	Q ⁰	Q ⁰	Q ⁰
L	L	L	Q=D	Q0	Q ⁰	Q ⁰
н	L	L	Q ⁰	Q=D	Q0	Q ⁰
L	Н	L	Q ⁰	Q ₀	Q≕D	Q ⁰
Н	Н	L	Q0 . •	Q ⁰	Q0	Q=D

Readout Method

RA	RB	ōc	Q ₀	Q1	Q ₂	Q ₃
X	Х	Н	Z	Z	Z	Z
L	١	L	W ₀ B ₀	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃
Н	L	L.	W ₁ B ₀	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃
L	Ŧ	L	W ₂ B ₀	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃
Н	Н	L	W ₃ B ₀	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃

Note 1: Q0: The level of Q before the indicated steady-state input conditions were established.

 $Q = D : \mbox{ The four selected internal latch outputs will assume the states applied to the four external data inputs. } $W_XB_Y: \mbox{ The Yth bit of word X. } X: \mbox{ irrelevant } Z: \mbox{ high-impedance} $Z: \mbox{ high-impeda$

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^{\circ}C$,)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
Vı	Input voltage		-0.5~+15	V
Vo	Output voltage	Off-state	$-0.5 \sim +5.5$	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
Tstg	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^{\circ}C$, unless otherwise noted)

0				Limits		Unit
Symbol	Parame	ter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
Іон	High-level output current	V _{OH} ≧2.4V	0		-2.6	mA
		V _{OL} ≦0.4V	0		4	mA
loL	Low-level output current	0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +70^{\circ}C$, unless otherwise noted)

					Limits			Unit
Symbol	Paramete	•	Test condi	tions	Min	Тур*	Max	Unit
VIH	High-level input voltage				2			V
VIL	Low-level input voltage			-			0.8	. V
Vic	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-1	8mA			-1,5	V
V _{OH}	High-level output voltage		V _{CC} =4.75V, V _I =0.8 V _I =2V, I _{OH} =-2.6mA	2.4	3.1		٧	
	1 1		V _{CC} =4.75V	I _{OL} = 4mA		0.25	0.4	٧
VoL	Low-level output voltage		V _I =0.8V, V _I =2V	I _{OL} = 8mA		0.35	0.5	V
lozh	Off-state high-level output cur	rrent	V _{CC} =5.25V, V _I =2V, V _I =2.7V				20	μА
lozL	Off-state low-level output curr	rent	V _{CC} =5.25V. V _I =2V. V _I =0.4V				-20	μA
		Ew					40	
		ŌĊ	V _{CC} =5.25V, V _I =2.7V				60	μA
hн	High-level input current	Other input	7	·			20	
'IH	riigii-iever iriput current	Ew					0.2	
		ŌC	V _{CC} =5.25V, V _I =10V				0.3	mA
		Other input					0.1	
		Ew					-0.8	
l _{IL}	Low-level input current	ŌĊ	V _{CC} =5.25V, V _I =0.4V	v .			-1.2	. mA
		Other input					-0.4	
los	Short-circuit output current	(Note 2)	V _{CC} =5.25V, V _O =0V	, , , , , , , , , , , , , , , , , , , ,	-30		- 130	mA
loo	Supply current		V _{CC} =5.25V (Note 3)			30	50	mA

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

^{3:} Icc is measured with W_A, W_B, R_A, R_B inputs grounded and D₀ \sim D₃, $\overline{E_W}$, \overline{OC} inputs at 4.5V.



Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

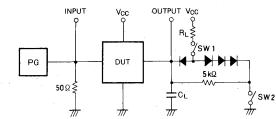
M74LS670P

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

0	Parameter	Test conditions		Unio		
Symbol	Farameter	rest conditions	, Min	Тур	Max	Unit
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	40	ns
t _{PHL}	time, from input RA, RB to output Q0,Q1,Q2,Q3	•		14	45	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation	C ₁ = 15pF (Note 4)		-11	45	. ns
t _{PHL}	time, from input \overline{E}_W to output Q_0 , Q_1 , Q_2 , Q_3	CL = 13DF (Note 4)		16	50	ns
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time	e,		9	45	ns .
t _{PHL}	from input D_0 , D_1 , D_2 , D_3 to output Q_0 , Q_1 , Q_2 , Q_3			14	40	ns
t _{PZH}	Output enable time to high-level	$R_L=2k\Omega$, $C_L=15pF$ (Note 4)		6	35	ns
t _{PZL}	Output enable time to low-level	$R_L = 2k\Omega$, $C_L = 15pF$ (Note 4)		10	40	ns
t _{PHZ}	Output disable time from high-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 4)		16	50	ns
t _{P⊾Z}	Output disable time from low-level	$R_L=2k\Omega$, $C_L=5pF$ (Note 4)		7	35	ns

Note 4: Measurement circuit



Symbol	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

- The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
 - PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) All diodes are switching diodes (t_{rr} ≤ 4ns)
 (3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $Ta=25^{\circ}C$, unless otherwise noted)

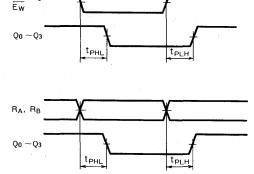
Symbol	Parameter	Test conditions	1	Limits		
		l est conditions	Min	Тур	Max	Unit
tw(Ew)	Write enable input Ew pulse width		25	9		ns
tw(oc)	Output control input OC pulse width		25	9		ns
t _{SU(D)}	Setup time D ₀ ~D ₃ to $\overline{E_W}$	·	10	5		ns
t _{SU(W)}	Setup time W _A , W _B to E _W		15	-2		ns
t _{h(D)}	Hold time D ₀ ∼D ₃ to E _W	,	15	1		ns
t _{h(W)}	Hold time WA, WB to EW		5	0		ns
tlatch	Latch time for new date (Note 5)		25	5		ns

Note 5: Latch time is the time allowed for the internal output of the latch to assume the state of new data.

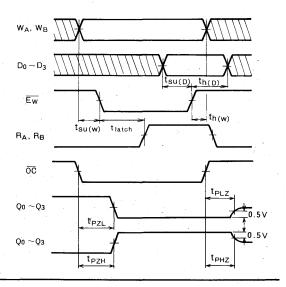
TIMING DIAGRAM (Reference level = 1.3V)

tw(Ew)

 $\underline{D_0} \sim D_3$



Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.



NEW PRODUCT

MITSUBISHI LSTTL

8-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS682P is a semiconductor integrated circuit containing two 8-bit words comparator functions.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Internal 24kΩ pull-up resistors on the Q inputs
- Active pull-up outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

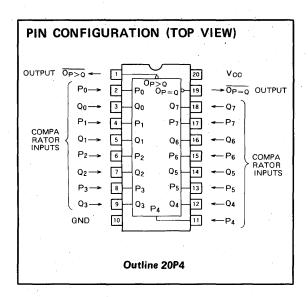
FUNCTIONAL DESCRIPTION

Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

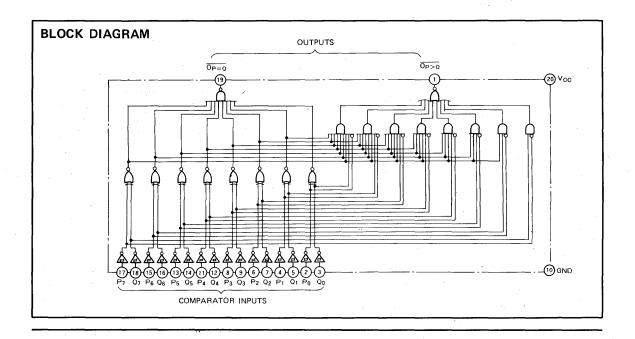
 ${\bf Q}_0\sim {\bf Q}_7$ have internal pull-up resistors (=24k Ω), so that misoperation due to noise is reduced on condition that ${\bf Q}_0\sim {\bf Q}_7$ are open.

Beside the IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	O _{P=0}	0 _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No.	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	



8-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE

P, Q	Op≕Q	O _{P>Q}
P=Q	L	н
P>Q	Н	L'
P <q< td=""><td>Н</td><td>Н.,</td></q<>	Н	Н.,

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \%$, unless otherwise noted)

,					
Symbol	Parameter	Conditions	Limits	Unit	
Vcc	Supply voltage		-0.5~+7	V	
	V _I Input voltage	Inputs P		-0.5~+15	V
VI		Inputs Q	-0.5~V _{CC} +0.5	V	
Vo	Output voltage	High-level state	-0.5~V _{CC}	V	
Topr	Operating free-air ambient temperature range		-20~+75	င	
T _{stg}	Storage temperature range		−65~+150	င	

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \circ$, unless otherwise noted)

Completed	Parameter			Limits			
Symbol			Min	Тур	Max	Unit	
Vcc	Supply voltage	4.75	5	5.25	٧		
Гон	High-level output current	V _{OH} ≥2.7V	0		-400	μΑ	
	Low-level output current	V _{OL} ≤0.4V	0		12	mA	
loL		V _{OL} ≦0.5V	0		24	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

Cumple at	Parameter		Test conditions -			Limits		l lain
Symbol	, rarameter				Min	Тур*	Max	Unit
V _{IH}	High-level input voltage				2			, , , V
VIL	Low-level input voltage						0.8	V
V _{T+} — V _{T-}	Hysteresis width		V _{CC} =4.75V			0.4		V
V _{IC}	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA				-1.5	V
Voн	High-level output voltage		$V_{CC} = 4.75V$, $V_1 = 2V$, $V_1 = 0.8V$, $I_{OH} = -400\mu A$		2.7			V
	Low-level output voltage		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	V
VoL			$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	V
		P, Q	V _{CC} =5.25V, V	1=2.7V			20	μΑ
lін	High-level input current	P	V _{CC} =5.25V, V	=10V				
	. Q		V _{CC} =5.25V, V _I =5.5V]		0.1	· mA
	Low lovel input sussent	Р	V - 5 05V V	0.4)/			-0.2	. mA
lic.	Low-level input current Q		$V_{CC} = 5.25V, V_1 = 0.4V$				-0.4	mA
los	Short-circuit output current (N	Note 1)	V _{CC} =5.25V, V _O =0V		-20		-100	mA
Icc -	Supply current		V _{CC} = 5.25V (Note 2)			42	70	m A

^{*:} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$. Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

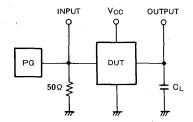
^{2:} ICC is measured with all inputs at value of 4.5V.

8-BIT MAGNITUDE COMPARATOR

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

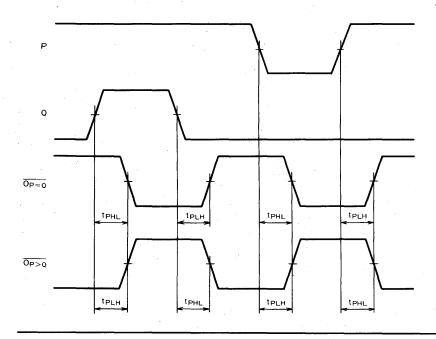
0		-	Limits			
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
t PLH	Low-to-high level, high-to-low level output			13	30	
t PHL	propagation time from inputs P to output Op=Q			16	30	ns
tpLH	Low-to-high level, high-to-low level output			12	30	
t PHL	propagation time from inputs Q to output $\overline{O_{P=Q}}$	C _L =45pF (Note 3) All other input pins in low-state		17	30	ns
t PLH	Low-to-high level, high-to-low level output propagation time from inputs P to output OP>Q			24	30	
t _{PHL}				21	30	ns
t PLH	Low-to-high level, high-to-low level output			26	30	
t PHL	propagation time from inputs Q to output $\overline{O}_{P>Q}$			27	30	ns

Note 3: Measurement circuit

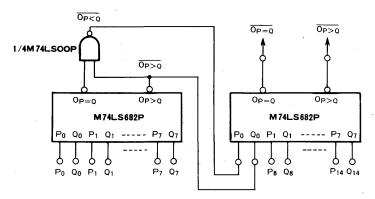


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_0 = 50Ω
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE Example of 15-bit comparator



DESCRIPITON

The M74LS683P is a semiconductor integrated circuit containing two 8-bit words comparator functions with open collector outputs.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Internal $24k\Omega$ pull-up resistors on the Q inputs
- Open collector outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

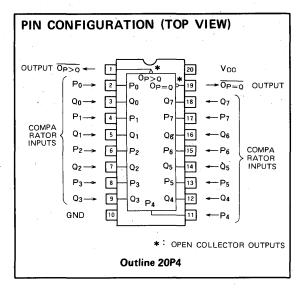
FUNCTIONAL DESCRIPTION

Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

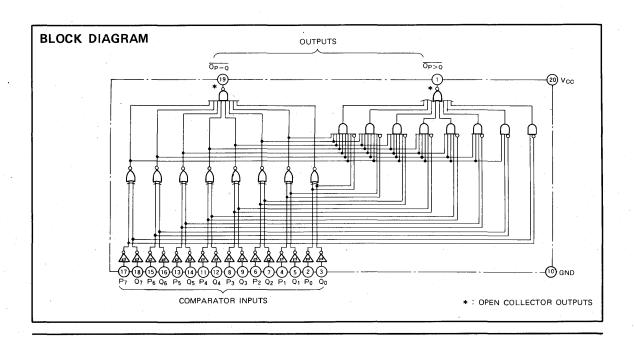
 $\mathbf{Q}_0\sim\mathbf{Q}_7$ have internal pull-up resistors (=24k Ω), so that misoperation due to noise is reduced on condition that $\mathbf{Q}_0\sim\mathbf{Q}_7$ are open.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	O _{P=0}	O _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	





FUNCTION TABLE

. P, Q	Op=Q	O _{P>Q}
P=Q	L.	Н
P>Q	H	L
P<0	H	Н

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Parameter Conditions		Unit
Vcc	Supply voltage		-0.5~+7	٧
V _I Input voltage	Inputs P	-0.5~+15	٧	
	Input voltage	Inputs Q	-0.5~V _{CC} +0.5	٧
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	~ ℃.
Tstg	Storage temperature range		-65~+150	ဗ

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter			Unit		
Symbol			Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V ₀ =5.5V	0		100	μΑ
	Low-level output current	V _{OL} ≤0.4V	0		12	mA
IOL		V _{OL} ≤0.5V	0		24	mΑ

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 ^{\circ}C$, unless otherwise noted)

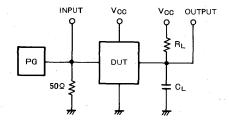
Symbol	Paramatas		Took	conditions	·	Limits		Unit
Symbol	Parameter	*	. lest	conditions	Min Typ★ I		Max	Unit
V _{IH}	High-level input voltage				2			V
VIL	Low-level input voltage		-	V _{CC} =4.75V			0.8	V
V _{T+} V _{T-}	Hysteresis width		V _{CC} =4.75V			0.4		٧
Vic	Input clamp voltage	Input clamp voltage		V _{CC} =4.75V, I _{IC} =-18mA			-1.5	٧
Гон	High-level output current		$V_{CC} = 4.75V$, $V_1 = 2V$, $V_1 = 0.8V$, $V_0 = 5.5V$				100	μΑ
	Low-level output voltage		$V_{CC} = 4.75V$ $V_{I} = 2V$ $V_{I} = 0.8V$ $I_{OL} = 12mA$ $I_{OL} = 24mA$			0.25	0.4	٧
VoL	Low-level output voltage					0.35	0.5	V +
		P, Q	V _{CC} =5.25V, V _I	=2.7V			20	μΑ
Lin	High-level input current	Р	V _{CC} =5.25V, V _I	=10V				
		Q	V _{CC} =5.25V, V _I =5.5V				0.1	mA
l	Low-level input current	Р	V _{CC} =5.25V, V _I =0.4V V _{CC} =5.25V (Note 1)				-0.2	mA
111	Low lover input current	Q					-0.4	mA
Icc	Supply current					42	70	mA

*: All typical values are at V_{CC} = 5V, $T_a \approx 25^{\circ}C$. Note 1: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

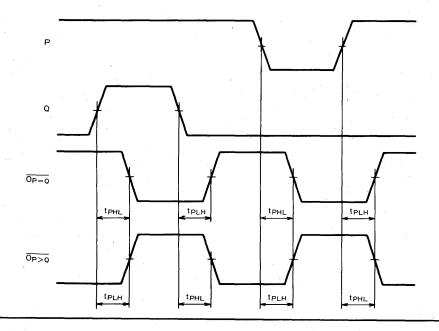
Symbol	Parameter	Test conditions	Limits			Unit
Symbol	raiametei	l est conditions	Min	Тур	Max	Onit
tpLH	Low-to-high level, high-to-low level output	·		23	45	
tpHL	propagation time from inputs P to output Op=Q			20	30	ns
tpLH	Low-to-high level, high-to-low level output			21	40	
tpHL	propagation time from inputs Q to output Op=Q	B -6670 0 -4555 (Note 2)		20	35	ns
tpLH	Low-to-high level, high-to-low level output	$R_L = 667\Omega$, $C_L = 45pF$ (Note 2) All other input pins in low-state.		26	45	
t _{PHL}	propagation time from inputs P to output OP>Q			22	30	ns
t PLH	Low-to-high level high-to-low level output			28	45	
t _{PHL}	propagation time from inputs Q to output Op>Q			26	30	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_P.P, Z_O = 50Ω
 (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



NEW PRODUCT

M74LS684P

8-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS684P is a semiconductor integrated circuit containing two 8-bit words comparator functions.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Active pull-up outputs.
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

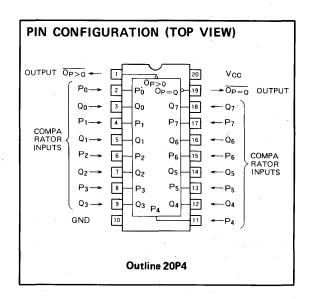
FUNCTIONAL DESCRIPTION

Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

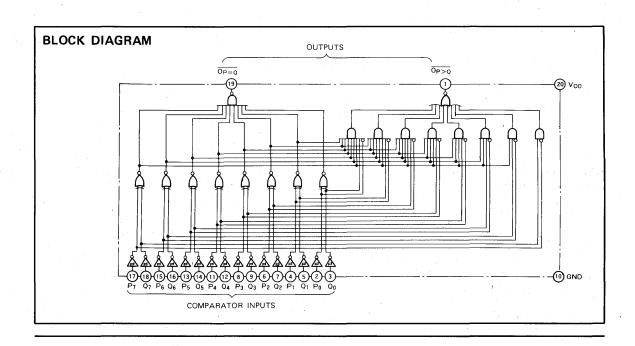
Note that this IC, in comparison to M74LS682P, does not have internal pull-up resistors on its inputs $Q_0\sim Q_7$.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.



Туре	Inputs		Outputs				
designation	Q 24kΩ pull-up	E	O _{P=0}	0 _{P>0}	Format		
M74LS682P	Yes	Νo	Yes	Yes	Active pull-up		
M74LS683P	Yes	No	Yes	Yes	Open collector		
M74LS684P	No	No	Yes	Yes	Active pull-up		
M74LS685P	No	No	Yes	Yes	Open collector		
M74LS688P	No	Yes	Yes	No	Active pull-up		
M74LS689P	No	Yes	Yes	No	Open collector		



8-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE

P, Q	O _{P=Q}	O _{P>Q}
P=Q	L	Н
P>Q	Н	L .
P <q< td=""><td>н</td><td>Н</td></q<>	н	Н

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
V _I	Input voltage		-0.5~+15	, V
Vo	Output voltage	High-level state	-0.5~V _{CC}	V
Topr	Operating free-air ambient temperature range		-20~+75	r
Tstg	Storage temperature range		− <u>65</u> ~+150	τ

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

0						
Symbol	Parar	neter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	V
1он	High-level output current	V _{OH} ≥2.7V	0		-400	μΑ
	IOL Low-level output current	V _{OL} ≦0.4∨	0		12	mA
IOL.		V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75 \text{ C}$, unless otherwise noted)

Symbol			11.1		Limits		Unit
Symbol	Parameter	lest	Test conditions			Max	Unit
VIH	High-level input voltage			· 2			V
VIL	Low-level input voltage					0.8	
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V			0.4		٧
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC}	= - 18mA			-1.5	V
Vон	High-level output voltage	$V_{CC} = 4.75V, V_1 = 2V,$	$V_1 = 0.8V, I_{OH} = -400 \mu A$	2.7			· V
.,		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	Ý
VoL	Low-level output voltage	$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	V
	High level in the second	V _{CC} =5.25V, V _I	=2.7V			20	μΑ
lин	High-level input current	V _{CC} =5.25V, V _I	=10V			0.1	mA
HL .	Low-level input current	V _{CC} =5.25V, V _I	=0.4V			-0.2	mA
los	Short-circuit output current (Note 1)	V _{CC} =5.25V, V _C	=0V	-20		-100	mA
Icc	Supply current	V _{CC} =5.25V (No	te 2)		40	65	mA

^{*:} All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

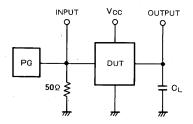
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			
	Farameter	l est conditions	Min	Тур	Max	Unit
t PLH	Low-to-high level, high-to-low level output			13	30	
t PHL	propagation time from inputs P to output Op=Q			16	30	ns
t PLH	Low-to-high level, high-to-low level output			12	30	
t PHL	propagation time from inputs Q to output Op=Q	0 45-5 (1) 0		17	30	ns
tpLH	Low-to-high level, high-to-low level output	CL=45pF (Note 3) All other input pins in low-state		24	30	
t PHL	propagation time from inputs P to output Op>Q			21	30	ns
t PLH	Low-to-high level, high-to-low level output			26	. 30	
t PHL	propagation time from inputs Q to output Op>Q			27	30	ns

^{2:} ICC is measured with all inputs at value of 4.5V.

8-BIT MAGNITUDE COMPARATOR

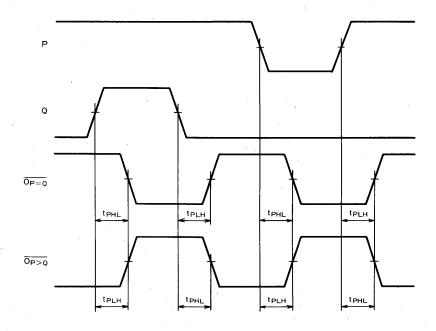
Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P,P}, Z_O = 50Ω

 (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



NEW PRODUCT

MT4LS685P

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS685P is a semiconductor integrated circuit containing two 8-bit words comparator functions with open collector outputs.

FEATURES

- Hysteresis at inputs (width = 400mW typical)
- Open collector outputs
- Wide operating temperature range ($T_a = -20 \sim +75^{\circ}$ C)

APPLICATION

General purpose, for use in for industrial and consumer equipment.

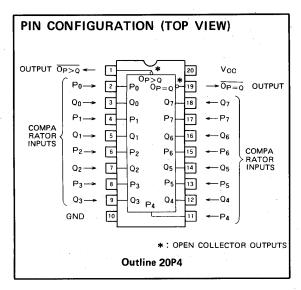
FUNCTIONAL DESCRIPTION

The eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

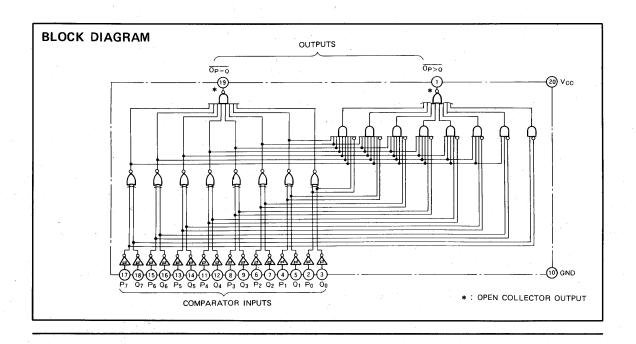
Note that this IC, in comparison to M74LS683P, does not have internal pull-up resistors on its inputs $Q_0 \sim Q_7$.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.



Туре	Inputs		Outputs				
designation	Q 24kΩ pull-up	Ē	Op=Q	O _{P>Q}	Format		
M74LS682P	Yes	No	Yes	Yes	Active pull-up		
M74LS683P	Yes	No	Yes	Yes	Open collector		
M74LS684P	No	No	Yes.	Yes	Active pull-up		
M74LS685P	No	No	Yes	Yes	Open collector		
M74LS688P	No	Yes	Yes	No	Active pull-up		
M74LS689P	No	Yes	Yes	No	Open collector		



FUNCTION TABLE

P, Q	Op=Q	O _{P>Q}
P=Q	L	Н
P>Q	Н	L
P <q< td=""><td>Н</td><td>Н</td></q<>	Н	Н

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75 \, ^{\circ} \text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°C.
Tstg	Storage temperature range		−65 ~ +150	r

RECOMMENDED OPERATING CONDITIONS (Ta = -20~ +75°C, unless otherwise noted)

ſ	Committee	Parameter					
ı	Symbol	Parami	eter .	Min	Тур	Max	Unit
ſ	Vcc	Supply voltage		4.75	5	5.25	٧
-	Гон	High-level output current	V _O =5.5V	. 0		100	μΑ
Ī		Low-level output current	V _{OL} ≦0.4V	0		12	mΑ
ı	IOL	Low-level output current	V _{OL} ≦0.5V	. 0		24	mΑ

ELECTRICAL CHARACTERISTICS (Ta = -20~ +75°C, unless otherwise noted)

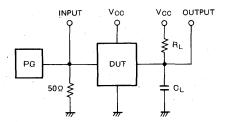
0 1	Parameter	To-t-	Test conditions		Limits		
Symbol	Farameter	i est c			Typ *	Max	Unit
VIH	High-level input voltage				-		V
VIL	Low-level input voltage					0.8	V
V _{T+} V _{T-}	Hysteresis width	V _{CC} =4.75V	V _{CC} =4.75V		0.4		>
Vic	Input clamp voltage	V _{CC} =4.75V, I _{IC}	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	V
Гон	High-level output current	V _{CC} =4.75V, V _I =2V,	$V_{CC} = 4.75V, V_1 = 2V, V_1 = 0.8V, V_0 = 5.5V$			100	μΑ
		V _{CC} =4.75V	I _{OL} =12mA		0.25	0.4	٧
VoL	Low-level output voltage	$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	>
	High Investment of the Control of th	V _{CC} =5.25V, V _I	=2.7V			20	μΑ
I _{IH}	High-level input current	$V_{CC} = 5.25V, V_1 = 10V$	=10V			0.1	mA
IIL	Low-level input current	V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =0.4V			-0.2	mA
lcc	Supply current	V _{CC} =5.25V (Not	te 1)		40	65	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C. Note 1: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

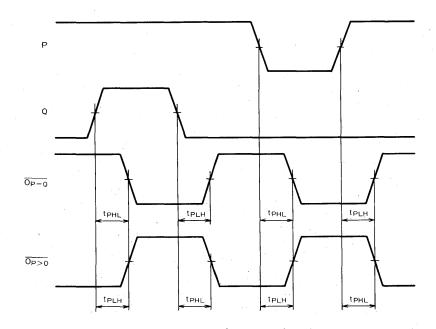
Symbol	Parameter	T	Limits			11-14
Farameter	Test conditions	Min	Тур	Max	Unit	
tpLH	Low-to-high level, high-to-low level output			23	45	
tpHL	propagation time from inputs P to output Op=Q			20	35	ns
tpLH	Low-to-high level, high-to-low level output			21	45	
t _{PHL}	propagation time from inputs Q to output Op=Q	D 0070 0 45 5 (V) 0)		20	35	ns
tpLH	Low-to-high level, high-to-low level output	$R_L = 667 \Omega$, $C_L = 45 pF$ (Note 2) All other input pins in low-state		26	45	
tpHL	propagation time from inputs P to output $\overline{O}_{P>Q}$			22	35	ns
tpLH	Low-to-high level, high-to-low level output			28	45	
tphL	propagation time from inputs Q to output $\overline{OP>Q}$			26	35	ns

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3 V_P , V_Q = 50 V_Q (2) V_Q = 1 includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



NEW PRODUCT

MITSUBISHI LSTTLS M74LS688P

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

DESCRIPTION

The M74LS688P is a semiconductor integrated circuit containing two 8-bit words comparator functions with enable input.

FEATURES

- Hysteresis at inputs P and Q (width = 400mV typical)
- Provided with enable input (E)
- Active pull-up output
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

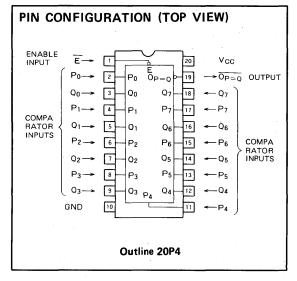
FUNCTIONAL DESCRIPTION

When enable input \overline{E} is low, two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at output $\overline{O_{P=0}}$.

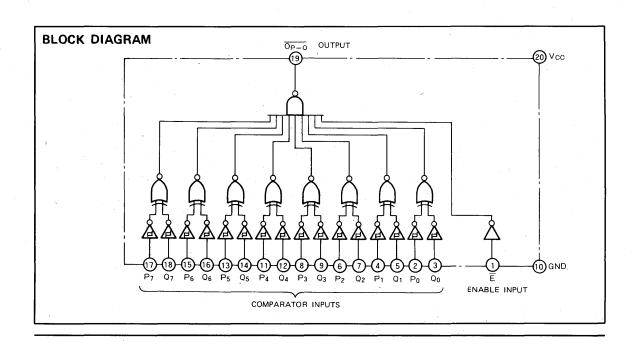
When E is high, $\overline{O_{P=Q}}$ is high in spite of $P_0 \sim P_7$ and $Q_0 \sim Q_7.$

. Beside this IC, there are eight-bit digital comparators varing input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	E	0p=0	0 _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	



8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

FUNCTION TABLE (Note 1)

P, Q	Ē	O _{P=Q}
P=Q	L	L
P>Q	L	н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
X	н	Н

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc ·	Supply voltage		-0.5~+7	V
Vı ·	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~ Vcc	V
Topr	Operating free-air ambient temperature range		-20~+75	°C
T _{stg}	Storage temperature range		−65∼+150	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75 \, ^{\circ}$ C, unless otherwise noted)

	Parameter					
Symbol	raran	ieter	Min	Тур	Max	Unit
Vcc	Supply voltage		4.75	5	5.25	٧
Гон	High-level output current	V _{OH} ≧2.7V	0		400	μΑ
		V _{OL} ≦0.4V	0		12	mΑ
loL	Low-level output current	V _{OL} ≤0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 - +75 \, \text{C}$, unless otherwise noted)

Symbol			Test conditions		Limits		
Symbol	Parameter	lest			Typ *	Max	Unit
V _{IH}	High-level input voltage						٧
VIL .	Low-level input voltage					0.8	٧
V _{T+} -V _{T-}	Hysteresis width	V _{CC} =4.75V	V _{CC} =4.75V		0.4		V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC}	V _{CC} =4.75V, I _{IC} =-18mA			-1.5	· V
Voн	High-level output voltage	V _{CC} =4.75V, V _I =2V,	$V_{CC} = 4.75V$, $V_1 = 2V$, $V_1 = 0.8V$, $I_{OH} = -400\mu A$				V
	Low-level output voltage	V _{CC} =4.75V	1 _{OL} =12mA		0.25	0.4	V
VoL	Low-level output voltage	$V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =24mA		0.35	0.5	V
	High lovel inside acceptance	V _{CC} =5.25V, V _I	=2.7V			20	μΑ
ін	High-level input current	V _{CC} =5.25V, V _I	=10V			0.1	mA
l _{IL}	Low-level input current	V _{CC} =5.25V, V _I	V _{CC} =5.25V, V _I =0.4V		,	-0.2	mA
los	Short-circuit output current	V _{CC} =5.25V, V _C	V _{CC} =5.25V, V _O =0V			-100	mA
loc	Supply current	V _{CC} =5.25V (No	te 2)		40	65	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.

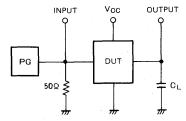
Note 2: I_{CC} is measured with all other inputs at value of 4.5V.

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

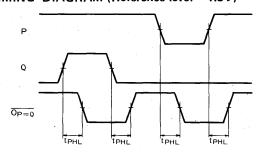
Symbol	Parameter	Test conditions		Limits		
Symbol	Faranteter			Тур	Max	Unit
t PLH	Low-to-high level, high-to-low level output			12	23	
t PHL	propagation time from inputs P to output Op=Q	·		18	28	ns
tPLH	Low-to-high level, high-to-low level output	0 -4555 (11 0)		11	23	
t PHL	propagation time from inputs Q to output Op=Q	C _L =45pF (Note 3) All other input pins in low-state		19	28	ns
tpLH	Low-to-high level, high-to-low level output			10	18	
t PHL	propagation time from input \(\overline{E} \) to output \(\overline{Op=Q} \)			16	20	ns

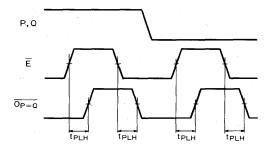
Note 3: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3 V_P . P_t , Z_0 = 50 Ω (2) C_L includes probe and jig capacitance.

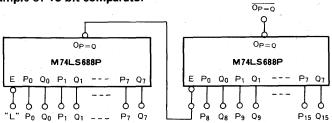
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Example of 16-bit comparator



NEW PRODUCT

M74LS689P

S-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS689P is a semiconductor integrated circuit containing two 8-bit words comparator functions with enable input and open collector output.

FEATURES

- Hysteresis at inputs P and Q (width = 400mV typical)
- Provided with enable input (E)
- Open collector output
- Operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

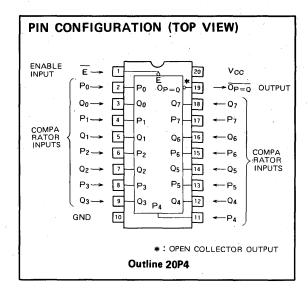
FUNCTIONAL DESCRIPTION

When enable input \overline{E} is low, two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at output $\overline{O_{P=0}}$.

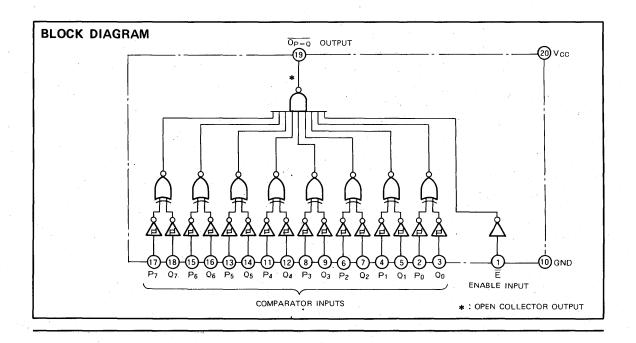
When E is high, $\overline{O_{P=Q}}$ is high in spite of $P_0 \sim P_7$ and $Q_0 \sim Q_2$.

Beside this IC, there are eight-bit digital comparators varing input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application in M74LS688P.



Туре	Inputs		Outputs			
designation	Q 24kΩ pull-up	Ē	OP=0	O _{P>0}	Format	
M74LS682P	Yes	No	Yes	Yes	Active pull-up	
M74LS683P	. Yes	No	Yes	Yes	Open collector	
M74LS684P	No	No	Yes	Yes	Active pull-up	
M74LS685P	No	No	Yes	Yes	Open collector	
M74LS688P	No	Yes	Yes	No	Active pull-up	
M74LS689P	No	Yes	Yes	No	Open collector	



8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

P, Q	Ē	0 _{P=0}
P=Q	L	L
P>Q	L	н
P <q< td=""><td>, r</td><td>H</td></q<>	, r	H
X	н	н

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = -20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc ·	Supply voltage		-0.5~+7	V
Vi	Input voltage		-0.5~+15	V
Vo	Output voltage	High-level state	-0.5~+7	V
Topr	Operating free-air ambient temperature range		-20~+75	°
T _{stg}	Storage temperature range	,	-65~+150	r

RECOMMENDED OPERATING CONDITIONS (Ta=-20~+75°C, unless otherwise noted)

Symbol	Parameter			Limits			
Symbol	Paran	neter	Min	Тур	Max	Unit	
Vcc	Supply voltage		4.75	5	5.25	V	
Гон	High-level output current	V ₀ =5.5V	0		100	μΑ	
	Low-level output current	V _{OL} ≤0.4V	0		12	mA	
JOL	LOW-level output current	V _{OL} ≦0.5V	0		. 24	mA	

ELECTRICAL CHARACTERISTICS (Ta = -20~+75°C, unless otherwise noted)

Symbol	Parameter High-level input voltage	Test conditions		Limits			11-21
				Min	Typ *	Max	Unit
V _{IH}				2			V
VIL	Low-level input voltage					0.8	٧
V _T +-V _T -	Hysteresis width	V _{CC} =4.75V			0.4		٧
Vic	Input clamp voltage	V _{CC} =4.75V, 1 _{IC} =-18mA				←1.5	٧
lон	High-level output current	$V_{CC} = 4.75V, V_1 = 2V, V_1 = 0.8V, V_0 = 5.5V$				100	μΑ
VoL	Low-level output voltage	$V_{CC} = 4.75V$ $V_1 = 2V$ $V_1 = 0.8V$	I _{OL} =12mA		0.25	0.4	٧
			IOL=24mA		0.35	0.5	٧
Ιн	High-level input current	V _{CC} =5.25V, V _I	=2.7V		,	20	μΑ
		V _{CC} =5.25V, V _I =10V				0.1	mA
lıL	Low-level input current	V _{CC} =5.25V, V _I =0.4V				-0.2	mΑ
Icc	Supply current	V _{CC} =5.25V (Note 2)			40	65	mA

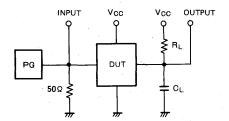
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25 \,^{\circ}C$, unless otherwise noted)

Symbol	Parameter	T	Limits			
		Test conditions	Min	Typ^	Max	Unit
tpLH	Low-to-high level, high-to-low level output propagation time from inputs P to output OP=O	R _L =667 Ω , C _L =45pF (Note 3) All other input pins in low-state.		23	40	ns
t _{PHL}				21	35	
t PLH	Low-to-high level, high-to-low level output propagation time from inputs Q to output Op≃Q			23	40	ns
t PHL				21	35	
t PLH	Low-to-high level high-to-low level output propagation time from input E to output $\overline{Op}=Q$			22	35	ns
t PHL				20	30	

^{*:} All typical values are at $V_{CC} = 5V$, $T_a = 25^{\circ}C$. Note 2: I_{CC} is measured with all inputs at value of 4.5V.

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

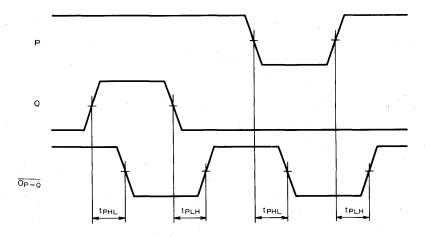
Note 3: Measurement circuit

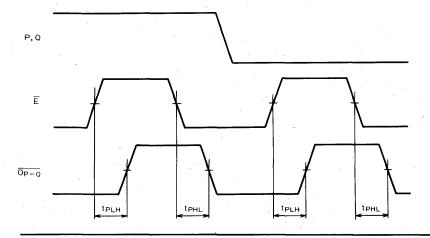


- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_T = 6ns, t_T = 6ns, t_T = 50ns, t_T = 9 = 3V_P, p, Z_O = 50Ω.

 (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





CONTACT ADDRESSES FOR FURTHER INFORMATION

Semiconductor Marketing Division Mitsubishi Electric Corporation 2-3, Marunouchi 2-chome

Chiyoda-ku, Tokyo 100, Japan 24532 MELCO J Telex: Telephone:

(03) 218-3473 (03) 218-3499

(03) 214-5570 Facsimile:

Overseas Marketing Manager Kita-Itami Works 4-1, Mizuhara, Itami-shi, Hyogo-ken 664, Japan

526408 KMELCO J Telex: Telephone: (0727) 82-5131

(0727) 72-2329 Facsimile:

HONG KONG =

Ryoden Electric Engineering Co., Ltd. 22nd fl., Leighton Centre 77, Leighton Road

Causeway Bay, Hong Kong 73411 RYODEN HX Telex:

Telephone: (5) 7907021 (852) 123-4344 Facsimile:

SINGAPORE =

MELCO SALES SINGAPORE PTE. LTD. 230 Upper Bukit Timah Road

#03-01/15

Hock Soon Industrial Complex

Singapore 2158

RS 20845 MELCO Telex: Telephone: 4695255

Facsimile: 4695347

TAIWAN =

MELCO-TAIWAN CO., LTD. 1st fl., Chung-Ling Bldg., 363, Sec. 2, Fu-Hsing S Road, Taipei, R.O.C.

25433 CHURYO Telex. "MELCO-TAIWAN"

(02) 735-3030 Telephone: (02) 735-6771 Facsimile:

U.S.A. =

NORTHWEST

Mitsubishi Electronics America, Inc. 1050 East Argues Avenue Sunnyvale, CA 94086, U.S.A. 172296 MELA SUVL Telex:

910-339-9549 Twx: Telephone: (408) 730-5900 Facsimile: (408) 730-4972

SOUTHWEST

Mitsubishi Electronics America, Inc. 991 Knox Street

Torrance, CA 90502, U.S.A. **664787 MELA TRNC** Telex:

(213) 515-3993 Telephone: Facsimile: (213) 324-6578

SOUTH CENTRAL

Mitsubishi Electronics America, Inc. 2105 Luna Road, Suite 320 Carrollton, TX 75006, U.S.A.

(214) 484-1919 Telephone: Facsimile: (214) 243-0207

NORTHERN

Mitsubishi Electronics America, Inc. 15612 Highway 7 #243 Minnetonka, MN 55345, U.S.A.

291115 MELA MTKA Telex: Telephone: (612) 938-7779 Facsimile: (612) 938-5125

NORTH CENTRAL

Mitsubishi Electronics America, Inc. 800 N. Bierman Circle Mt. Prospect, IL 60056, U.S.A.

Telex: 270636 MESA CHIMPCT Telephone: (312) 298-9223

(312) 298-0567

NORTHEAST

Facsimile:

Mitsubishi Electronics America, Inc. 200 Unicorn Park Drive

Woburn, MA 01801, U.S.A. Telex: 951796 MELA WOBN

Twx: 710-348-1229 (617) 938-1220 Telephone: Facsimile: (617) 938-1075

MID ATLANTIC

Mitsubishi Electronics America, Inc.

Two University Plaza

Hackensack, NJ 07601, U.S.A. 132205 MELA HAKI Telex:

Twx: 710-991-0080 Telephone: (201) 488-1001 Facsimile: (201) 488-0059

SOUTH ATLANTIC

Mitsubishi Electronics America, Inc. 6575 The Corners Parkway

Suite 100

Norcross, GA 30092, U.S.A. 910-380-9555 Twx: Telephone: (404) 662-0813

Facsimile: (404) 662-5208

SOUTHEAST

Mitsubishi Electronics America, Inc. Town Executive Center 6100 Glades Road #210

Boca Raton, FL 33433, U.S.A. Twx. 510-953-7608 Telephone: (305) 487-7747

Facsimile: (305) 487-2046 **WEST GERMANY** =

Mitsubishi Electric Europe GmbH

Headquarters: Gothear Str. 6

4030 Ratingen 1, West Germany Telex: 8585070 MED D Telephone: (02102) 4860 Facsimile: (02102) 486-115

Munich Office: Arabellastraße 31

8000 München 81, West Germany

Telex: 5214820 Telephone: (089) 919006-09 Facsimile: (089) 9101399

FRANCE-

Mitsubishi Electric Europe GmbH 65 Avenue de Colmar Tour Albert 1er F-92507 Rueil Malmaison Cedex,

France 202267 (MELCAM F) Telex: (01) 7329234 Telephone:

(01) 7080405 Facsimile:

ITALY ==

Mitsubishi Electric Europe GmbH Centro Direzionale Colleoni

Palazzo Cassiopea 1

20041 Agrate Brianza I-Milano Telephone: (039) 636011

Facsimile: (039) 6360120

SWEDEN =

Mitsubishi Electric Europe GmbH Lastbilsvägen 6B 5-19149 Sollentuna, Sweden

10877 (meab S) Telex: Telephone: (08) 960468 Facsimile: (08) 966877

U.K.=

Mitsubishi Electric (U.K.) Ltd. Hertford Place, Denham Way, Maple Cross, Rickmanworth, Herts, WD3 2BJ, England, U.K.

Telex: 916756 MEUKG (923) 770000 Telephone: Facsimile: (923) 775282

AUSTRALIA =

Mitsubishi Electric Australia Pty. Ltd. 73-75, Epping Road, North Ryde, P.O. Box 1567, Macquarie Centre, N.S.W., 2113, Australia

Telex: **MESYD AA 26614** (02) (888) 5777 Telephone: (02) (887) 3635 Facsimile:

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